# A New Scan-BIST Structures to Test delay Faults in Sequential Circuits

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**Abstract.** Delay testing that requires the application of consecutive two-pattern tests is not an easy task in a scan-based environment. This paper proposes a novel approach to the delay fault testing problem in scan-based sequential circuits. This solution is based on the combination of a BIST structure with a scan-based design to apply delay test pairs to the circuit under test.

**Keywords:** delay faults, scan design, BIST

## 1. Introduction

Delay fault test generation has been the subject of extensive investigations [1–5]. Concerning sequential circuits, various issues are illustrated in [6–9]. For such circuits, the use of scan design rather than non-scan design is generally recommended. Scan techniques reduce test generation complexity of these circuits [10] by improving testability of the CUTs. However, a remaining important barrier to the practical use of delay testing in scan environment is the application of two-pattern tests to the combinational logic portion of the circuit. Actually, in a standard scan design, it is not possible to apply a pre-determined test pattern pair by scan shifting the bits of the test patterns.

Despite the fact that many different solutions have been investigated until now to generate tests for delay faults in a scan environment [11–17], the application of two-pattern test remains a problem due to the poor delay fault coverage or the prohibitive area overhead it induces. A solution to solve this problem can be to associate a BIST structure with a scan-based design [18, 19]. In this case, the scan design removes the sequentiality problem by reducing the test generation complexity while BIST allows to directly apply the desired test pair without the need to load scan registers by shifting bits. Moreover, BIST allows to apply the test sequence at the system clock speed that is needed to test delay faults.

In recent papers [20, 21], we presented a new BIST test pattern generator (TPG) for delay testing in combinational circuits. Here, we propose to combine the BIST structure with a scan-based design to test delay faults in sequential circuits. The main contribution of this paper is first to present the new scan-BIST TPG (Section 2), and then to give comparative results with a pure scan implementation and the double-strobe flip-flop structure proposed in [12] in terms of robust delay fault coverage, test sequence length and area overhead (Section 3).

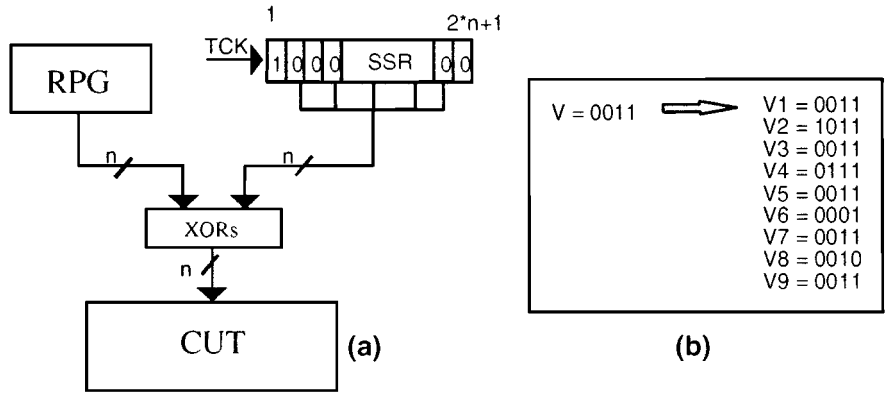



*Fig. 1.* The SIC TPG design (a) and the associated subsequence (b).

## 2. Delay Fault-Oriented BIST Test Pattern Generator

### *2.1. Principle of BIST Test Pattern Generator*

For the reader's convenience, we briefly remind the principle of the BIST TPG we propose in [20, 21] (see Fig. 1). The even parallel outputs of a Scan Shift Register (SSR) with $2 * n + 1$ stages are combined with the $n$ outputs of a Random Pattern Generator (RPG) using $n$ XOR gates. The RPG produces a sequence of random patterns of $n$ bits ($n$ being the number of primary inputs of the CUT). By initializing the SSR with (10...0) and activating its clock, a walking one is obtained. For each random pattern outputed by the RPG, this walking one produces on the XOR outputs the complete Single Input Change (SIC) sequence of $n$ patterns. This SIC sequence is sufficient to detect all robustly testable path delay faults [5, 22]. For the whole sequence of $Nr$ random patterns generated by the RPG, this structure produces a sequence of $(2 * n + 1) \cdot Nr$ patterns.

For example, Fig. 1(b) presents the sequence obtained from an initial vector $V$ provided by a 4 bits RPG ($V = 0011$). Each bit of the initial pattern is shifted once from 0 to 1 and once from 1 to 0. So, if a path delay fault is tested with a subsequence of SIC patterns, it is tested for both rising and falling transitions on its inputs.

### *2.2. SSR Optimization*

The structure of the TPG design described in the previous section can be optimized in order to reduce the area overhead. For this purpose, a first solution consists in replacing the SSR by a state machine or a counter/decoder based structure. Such a counter/decoder based structure works as follows: the counter produces $2 * n + 1$ states with $n$ being the number of circuit inputs. The decoder composed of $n + 1$ AND gates produces the walking one that allows to generate the required SIC test sequence. As shown in Fig. 2, this structure can be optimized still further. The number of counter states can be divided by 2 and then reduced to $n + 1$ by injecting the clock signal into the AND gates. Then, when the clock is low, the state machine composed of the counter and the decoder produces a vector of 0's and the vector provided by the RPG is transferred through the XOR network to the circuit inputs. When the clock is high, the outputs of the AND gates produce

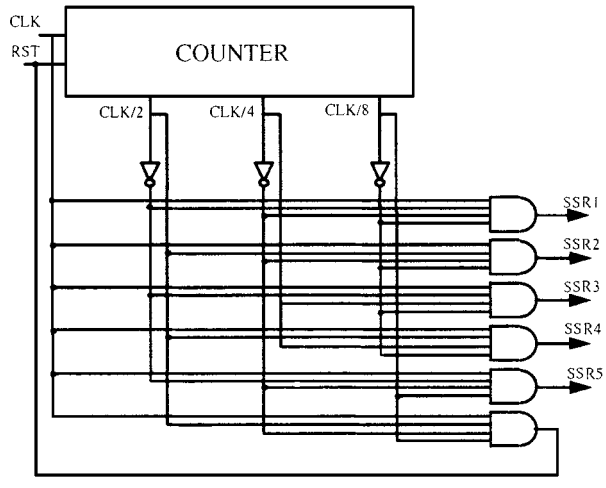



*Fig. 2.* The counter/decoder.

a vector with a 1 in only one bit position. A transition is then produced through the XOR network on the corresponding input of the circuit. Note that a signal RST is generated on the state $n+1$, and that this signal is used to reset the counter and to increment the RPG.

Due to the reduced number of flip-flops ($\log_2(n+1)$) required to implement the function, this counter/decoder reduces the area overhead of the TPG design. For example, consider a circuit with five inputs. Eleven flip-flops are necessary to generate the robust test sequence with the basic SSR structure, while only three flip-flops are needed with the counter. Even if six AND gates have to be added to decode the counter outputs, the area overhead is always reduced compared with the SSR structure. Table 1 presents results obtained on ISCAS'89 benchmark circuits. The third column gives the number of flip-flops of the basic SSR structure and the fourth column gives the number of flip-flops used by the counter/decoder. The area reduction ($Ar_1$) between the basic SSR structure and the counter/decoder is given in the fifth column. The evaluation of the area reduction has been done using the ES2 standard cell library with process ECPD10 [23]. For the counter-based structure, this evaluation takes into account the flip-flops and the AND gates of the decoder. An average of 40.7% area reduction has been obtained on the set of benchmark circuits compared with the basic SSR structure.

### *2.3. Optimization Related to the CUT Structure*

By considering the structural characteristics of the CUT, the area overhead of the TPG structure can be reduced still further. Assume a CUT with $n$ inputs and $m$ outputs. As it has been verified on a number of circuits, all the $n$ inputs do not always influence all the $m$ outputs [20]. In this case, inputs that do not belong to the same input cone of logic can be changed simultaneously without modifying the robust delay fault coverage. In the following, such inputs are called "compatible" inputs. Conversely, inputs that belong to a same cone of logic are called "incompatible" inputs.

Because compatible inputs can be switched simultaneously without modifying the robust delay fault coverage, the TPG design can hence be optimized. More formally, when $k$ inputs of the circuit are compatibles, only one SSR (or counter) stage is needed to switch simultaneously these $k$ inputs. Hence, the total number of SRR (or counter) stages is reduced. This reduction implies a reduction in the number of flip-flops

*Table 1.* Area reduction provided by SSR optimization on ISCAS'89 benchmark circuits.

| | | SSR replaced by counter/decoder | | Optimization related to the CUT | |
|---|---|---|---|---|---|
| Circuit | No. of flip-flops Basic SSR | No. of flip-flops Counter/Decoder | ($Ar_1$%) Area reduction | No. of flip-flops Counter/Decoder | ($Ar_2$%) Area reduction |
| s382 | 49 | 5 | 47 | 4 | 68 |
| s386 | 27 | 4 | 45 | 4 | 48 |
| s420 | 71 | 6 | 46 | 6 | 48 |
| s510 | 51 | 5 | 48 | 5 | 56 |
| s526 | 49 | 5 | 47 | 4 | 68 |
| s713 | 109 | 6 | 50 | 5 | 74 |
| s838 | 135 | 7 | 36 | 7 | 37 |
| s953 | 91 | 6 | 49 | 5 | 77 |
| s1238 | 65 | 6 | 45 | 5 | 61 |
| s1494 | 29 | 4 | 47 | 4 | 47 |
| s5378 | 429 | 8 | 36 | 6 | 86 |
| s9234 | 495 | 8 | 36 | 7 | 79 |
| s13207 | 1401 | 10 | 20 | 8 | 81 |
| s15850 | 1223 | 10 | 20 | 8 | 81 |
| s35932 | 3527 | 11 | 16 | 4 | 99 |
| s38417 | 3329 | 11 | 16 | 7 | 96 |
| s38584 | 2929 | 11 | 16 | 8 | 93 |

for the SSR-based structure or may imply a reduction in the number of flip-flops for the counter/decoder based structure ($N$ flip-flop $= \log_2(N$ states)). For the counter/decoder, the reduction in the number of states also implies a reduction in the number of AND gates in the decoder. All these reductions directly influence the area overhead but also involve a reduction in the number of test vectors to achieve the desired fault coverage.

This optimization that related to the CUT structure has been validated on ISCAS'89 benchmark circuits. Table 1 presents the area reduction obtained by associating the optimization related to the CUT structure with the use of the counter/decoder presented in the previous section. The sixth column shows the final number of flip-flops required by the counter/decoder based structure. The seventh column shows the complete area reduction ($Ar_2$) with respect to the basic SSR structure. An average of 66.43% area overhead reduction has been obtained compared with the basic SSR structure. The difference between $Ar_2$ and $Ar_1$ represents the effect of the optimization related to the CUT structure.

## 3. Insertion of the BIST TPG Structure in a Scan Environment

From a general point of view, scan-design techniques reduce test generation complexity of sequential circuits [10] by improving the testability of the CUT. The basic element of any scan-design technology is a scanable flip-flop, and the simplest form of a scan chain is based on flip-flops connection via a multiplexor with normal mode and test mode. In normal mode, the scan chain operates in its normal parallel load mode. In test mode, it operates as a shift register with a scan input. For stuck-at faults, only single test patterns have to be considered during test generation, and traditionally, this is correctly taken into account by standard scan designs.

Concerning delay faults, the problem is quite different because two pattern tests have to be considered during test. Unfortunately, in a standard scan design, it is not possible to apply a pre-determined two-pattern test by classically scan-shifting the two patterns into the scan chain. It is therefore not possible to get a high delay fault coverage with such a standard scan design. Hence, the only way to improve the delay fault testability of sequential circuits is to modify the scan structure to allow applying dedicated tests for delay faults.

The solution we propose is to associate the BIST structure proposed in [20, 21] with the scan-based design. Such an association has been considered before in an other context (stuck-at fault testing) and for other purposes like partial scan [14, 19]. In the context of delay testing, scan design removes the sequentiality problem by reducing the test generation complexity while BIST allows to directly apply delay fault oriented tests without the need to load scan registers by shifting bits. In fact, the idea is to add some delay fault detection capabilities to a given stuck-at fault oriented test sequence injected to the circuit through the scan chain. These delay fault detection capabilities can be provided by the BIST structure presented previously. From each test vector loaded into the input scan chain, a robust SIC test subsequence is generated by the SIC test pattern generator. As seen previously, the robust SIC test subsequence is generated from an SSR or a counter/decoder, and an XOR network. Thus, the scan chain replaces the RPG part of the TPG design shown in the previous section. Note that with such an approach, the circuit responses cannot be injected directly into the output scan chain. A signature analyzer (SA) is necessary to compress the test output data from each SIC subsequence. At the end of each SIC subsequence, a new vector is loaded in the scan-in chain and the signature that corresponds to the subsequense is shifted-out.

Note that scan-based sequential circuits are not only composed by an input scan chain and an output scan chain (case illustrated in Fig. 3(a)). In state machines, the register which transmits data to the combinational part of the circuit is the same than the one that receives data from this part of the circuit. In this case, the scan chain has to fill the functions of an input scan chain and of an output scan chain. The Scan-BIST structure adapted to deal with state machines is presented in Fig. 3(b). The scan path IN/OUT represents both the input scan chain and the output scan chain as well as a compressor function (SA) distributed into each scan cell.

According to the considered scan structure, different types of scan cells can be used in the scan chain. In particular, scan cells are different depending on whether they are connected to the CUT inputs only (scan path IN), to the CUT outputs only (scan path OUT) or both to the CUT inputs and outputs (scan path IN/OUT). The three different types of scan cells are represented in Fig. 4. Figure 4(a) shows the scan cell used in an IN scan path. This cell allows to configure the circuit in its normal operation mode (C0C1 = 10) to serially shift a test vector (C0C1 = 01) or to generate the robust test sequence using the walking one generated by the

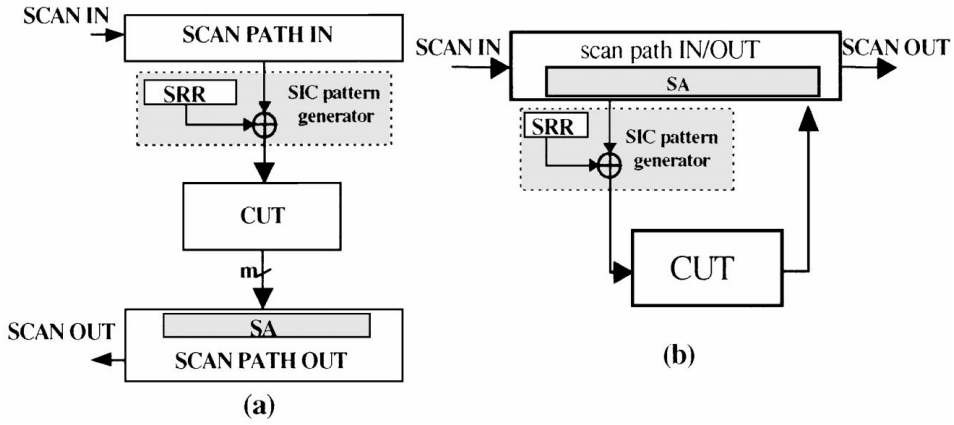
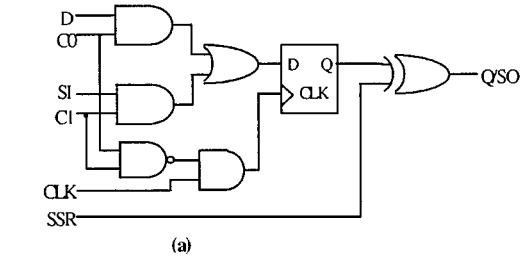
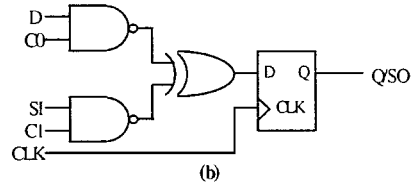


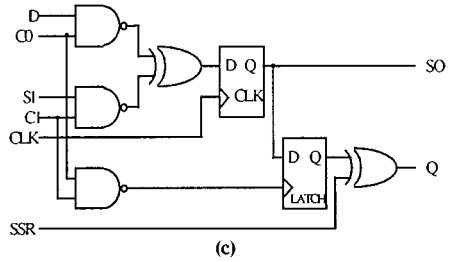

*Fig. 3.* Combination of scan and BIST.




| C0 | C1 | Configuration modes |
|---|---|---|
| 0 | 0 | Reset |
| 0 | 1 | Shift register |
| 1 | 0 | Normal function |
| 1 | 1 | Delay test - Clock inhibited |




| C0 | C1 | Configuration modes |
|---|---|---|
| 0 | 0 | Reset |
| 0 | 1 | Shift register |
| 1 | 0 | Normal function |
| 1 | 1 | Signature analyser |




| C0 | C1 | Configuration modes |
|---|---|---|
| 0 | 0 | Reset |
| 0 | 1 | Shift register |
| 1 | 0 | Normal function |
| 1 | 1 | Signature analyser - Delay |

*Fig. 4.* Scan cell used in: (a) input scan chain, (b) output scan chain and (c) input/output scan chain.

SSR (C0C1 = 11). When (C0C1 = 11), the clock is inhibited and the SIC test sequence can be generated by the SSR from the test pattern stored into the flip-flop. The scan cell used in an OUT scan path (Fig. 4(b)) is the standard cell allowing the normal operation mode (C0C1 = 10), the response compaction mode (C0C1 = 11) or the serial shift out mode (C0C1 = 01). The scan cell used in the IN/OUT scan chain (Fig. 4(c)) can be configured as both: register that transmit data to the CUT or register that receive data from the CUT. The test pattern injected in the IN/OUT scan path is stored in the latch during the SIC test sequence generation and the circuit response is captured in the D flip-flop configured for data compaction.

## 4. Experimental Results

The method we propose in this paper has been validated on ISCAS'89 benchmark circuits. A set of experiments has been performed to compare the Scan-BIST structure with (i) a pure scan implementation and (ii) the double-strobe flip-flop scan-based structure proposed in [12]. The main characteristic of this double-scan structure is that it allows to apply deterministic two pattern tests to the CUT, and hence, to reach the maximum robust path delay fault coverage.

Results of the comparison between the proposed Scan-BIST structure and the standard pure scan implementation are summarized in Table 2. Column 2 gives the robust path delay fault coverage achieved with a 100% stuck-at fault coverage deterministic test sequence generated by [24] and applied through the standard scan implementation. Note that each intermediate vector produced during the scan shifting process is considered also as a test vector. Column 3 gives the robust path delay fault coverage achieved with the proposed Scan-BIST structure with a SIC sequence generation activated from the same deterministic stuck-at fault test sequence. As can be seen, the delay fault coverage obtained with the scan-BIST structure is almost always very much higher than the one obtained with a standard scan chain (which is always very low). Note that results in terms of delay fault coverage are not provided for biggest benchmark circuits due to the limitation of the delay fault simulator used for these experiments because of the high number of path delay faults to be considered.

*Table 2.* Comparison with a pure scan implementation (NA = not available).

| Circuit | FC (%) | | Area overhead Scan-BIST/Pure scan (%) |
|---|---|---|---|
| | Pure scan | Scan-BIST | |
| s382 | 25 | 61.13 | 77.99 |
| s386 | 10.14 | 99.03 | 52.51 |
| s420 | 12.61 | 87.98 | 116.98 |
| s510 | 18.66 | 95.19 | 70.94 |
| s526 | 22.56 | 82.68 | 63.57 |
| s713 | 6.07 | 13.10 | 73.72 |
| s838 | 13.03 | 82.81 | 124.03 |
| s953 | 5.19 | 95.70 | 62.8 |
| s1238 | 5.70 | 43.82 | 41.35 |
| s1494 | 12.06 | 94.06 | 15.23 |
| s5378 | 6.74 | 52 | 49.14 |
| s9234 | NA | NA | 37.5 |
| s13207 | NA | NA | 60.93 |
| s15850 | NA | NA | 49.13 |
| s35932 | NA | NA | 54.6 |

Column 4 reports the results of the area comparison between the two structures. The area of the scan chain has been estimated from data coming from the ES2 standard cell library with the CMOS ECPD10 process [23]. Note that only the cells of the scan chain have been considered in the estimation of the scan area (routing area has not been considered). These results show an average area overhead of the test structures of 50% for the biggest ISCAS'89 circuits. But on the other side, this area overhead has to be considered with a target fault coverage in mind (the robust delay fault coverage increases from 15 to 90% in average).

Results of the second comparison between the proposed Scan-BIST structure and the double-strobe flip-flop scan-based structure [12] are listed in Table 3. Two groups of results are first reported for each structure: the number of test patterns loaded in each structure (column 3 and 6), the number of clock cycles required to apply the given test patterns (columns 4 and 7) and the obtained robust delay fault coverage (columns 5 and 8). The values of the last column represents the area comparison between the proposed scan-BIST structure and the double-strobe flip-flop structure. Note that $(-)$ means that our structure requires less area than the double-strobe flip-flop implementation.

The first comment concerning these results is that the area overhead obtained with the proposed Scan-BIST structure is comparable to that obtained with the double flip-flop structure. For the biggest benchmark circuits, it is even more efficient with our solution. A second comment is that the scan-BIST structure requires a drastically shorter test application time. Indeed, the number of clock cycles necessary to apply the complete test sequence by using the double flip-flop implementation is very high even if, on the other hand, the robust delay fault coverage achieved is maximal. Note that deterministic delay test pairs have been used with the double strobe structure while the delay fault coverage achieved by using the scan BIST structure has been obtained by loading the scan-BIST structure with a stuck-at fault test sequence.

A last and important comment concerning these results is that the double scan implementation is not applicable for large circuits (NA = not applicable). Actually, because of the number of path delay faults

*Table 3.* Fault coverage and test time obtained for ISCAS'89 benchmark circuits (NA = not available).

| Circuit | No. of inputs | Scan-BIST | | | Double flip-flop | | | Area overhead (%) |
|---|---|---|---|---|---|---|---|---|
| | | No. of stuck-at test patterns | Test time (No. of clock cycles) | Fault coverage (%) | No. of delay test patterns | Test time (No. of clock cycles) | Fault coverage (%) | |
| s382 | 3 | 33 | 1209 | 61.13 | 664 | 28509 | 86 | 5.33 |
| s386 | 7 | 77 | 1469 | 99.03 | 456 | 5915 | 100 | 20.63 |
| s420 | 19 | 64 | 3280 | 87.98 | 1124 | 37059 | 100 | 36.56 |
| s510 | 19 | 70 | 1896 | 95.19 | 804 | 10439 | 100 | 37.97 |
| s526 | 3 | 71 | 2577 | 82.68 | 752 | 32293 | 84.39 | 4.7 |
| s713 | 35 | 45 | 2134 | 13.10 | 1522 | 59319 | 19.97 | 22.66 |
| s838 | 35 | 106 | 10526 | 82.81 | 2466 | 160225 | 100 | 41.1 |
| s953 | 16 | 107 | 5272 | 95.70 | 2218 | 130803 | 100 | 7.06 |
| s1238 | 14 | 188 | 7914 | 43.82 | 2584 | 95571 | 53.59 | 11.18 |
| s1494 | 8 | 159 | 3345 | 94.06 | 16684 | 21203 | 97.67 | 7.5 |
| s5378 | 35 | 140 | 33919 | 52 | 9754 | 3501327 | 69.29 | −0.75 |
| s9234 | 19 | 299 | 142552 | NA | NA | NA | NA | 0.16 |
| s13207 | 31 | 270 | 370569 | NA | NA | NA | NA | −0.88 |
| s15850 | 14 | 152 | 184365 | NA | NA | NA | NA | −1.08 |
| s35932 | 35 | 70 | 246168 | NA | NA | NA | NA | −7.73 |

to consider during the ATPG process, it is not possible to derive a deterministic robust test sequence for path delay faults for such large circuits. By using the scan-BIST structure, we can generate the test sequence to test large circuits even if the delay fault coverage cannot be provided for biggest circuits. This is due to the limitations of the delay simulator (not the ATPG process).

## 5. Conclusion

One problem in delay fault testing for sequential circuits using a standard-scan methodology is the inability to provide an acceptable robust delay fault coverage. In this paper, we propose a new structure that allows to apply two-pattern test sequences to a circuit designed with scan. This structure is based on the combination of BIST and Scan. The Scan design removes the sequentiality problem by reducing the test generation complexity while BIST allows to directly apply the desired test pattern pair to the circuit under test.

Experimental results obtained from ISCAS'89 benchmark circuits indicate that our structure allows to achieve a high robust delay fault coverage from a deterministic stuck-at fault test sequence in a short application time. The comparison with the double scan implementation have shown that the scan BIST structure is comparable in terms of area overhead and it presents an advantage for large circuits for which generating deterministic test sequences is increasingly difficult.

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