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Research Article

ADC Production Test Technique Using Low-Resolution Arbitrary Waveform Generator

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Standard production test techniques for ADC require an ATE with an arbitrary waveform generator (AWG) with a resolution at least 2 bits higher than the ADC under test resolution. This requirement is a real issue for the new high-performance ADCs. This paper proposes a test solution that relaxes this constraint. The technique allows the test of ADC harmonic distortions using only low-cost ATE. The method involves two steps. The first step, called the learning phase, consists in extracting the harmonic contributions from the AWG. These characteristics are then used during the second step, called the production test, to discriminate the harmonic distortions induced by the ADC under test from the ones created by the generator. Hardware experimentations are presented to validate the proposed approach.

1. INTRODUCTION

Analog-to-digital converters (ADCs) are nowadays part of complex systems developed for diverse domains such as medical applications, telecommunications, and consumer applications. The increasing performances of such systems induce the need of developing high-speed and high-resolution ADCs. In addition to developing high-resolution ADCs, a relevant challenge is to have test instrument performances higher than ADC under test performances.

Indeed, the common way to test ADCs in production is the DSP-based method [1]. In order to achieve such a test, there is a need of an arbitrary waveform generator (AWG), and a capture memory, combined with a processing unit in the tester. The accuracy of such a test depends on the instrument performances. The most critical instrument is the AWG. As a rule of thumb, the signal delivered by the generator must be 10 dB better than the specification limits of the ADC, to ensure acceptable test conditions. Consequently, it is commonly admitted that the generator resolution should be at least 2-bit higher than the tested ADC resolution.

In this context, it is clear that there is a great interest in developing new test solutions that relax the constraints on the test instrument performances.

Digital-to-analog converters (DACs) are the main components of AWGs. In [2–5], solutions for the compensation of DACs nonlinearity are proposed. These solutions are based on hardware modifications. Unfortunately, in our context, the DACs are already embedded in test instruments. In [6], a digital processing technique is proposed to compensate for DAC nonlinearity without any hardware modification. This technique could be suitable for the compensation of AWGs, but the technique needs high-performance instruments to implement the calibration routine. As a consequence, if there is a need of a high-performance instrument for calibration, the interest in using a low-performance AWG is reduced.

Some publications address another approach [7–9]. This approach consists in relaxing constraints on AWG performances by discriminating the sources of errors in the test path or by virtually improving the performances of the test instrument.

Two techniques deal directly with low-performance stimuli for converter testing. The first technique; the SEIR [7], is a histogram-based technique dedicated to the test of ADC linearity using low-linearity stimuli. The second one is the 2-ADC method [8] that permits to estimate noise parameters from ADCs under test. Both methods overcome the performance issue of the stimuli by discriminating the

errors of the DUT from the errors of the setup. However, these methods are dedicated to the measurement of linearity or noise of an ADC under test. None of them address the measurement of harmonics in order to compute some dynamic parameters.

Finally, another method, the wobbling technique, is proposed in [9] that reduces the effect of rounding from the converter in order to accurately estimate its dynamic parameters. In particular, the wobbling-based technique improves the repeatability of the harmonic distortion measurements. Although this method proved to be efficient, the level of the harmonics of the AWG still needs to be lower than those of the ADC under test to avoid any fault masking. Consequently, this solution does not solve the problem for most of the current ADCs.

A conventional solution to reduce the AWG nonlinearities is to use a filter centred on the test frequency. However, this solution is quite expensive as a new filter is required for each test frequency, involving a complex test board with costly calibration phase.

In this context, the objective of this paper is to propose a method to test ADC harmonic distortions using only a low-cost ATE. This method relies on an initial learning phase, in which the AWG characteristics are estimated. These AWG characteristics are subsequently used to discriminate the harmonic distortions induced by the ADC under test from the ones induced by the AWG.

The paper is organized as follows. The first section presents the usual ADC test parameters and the instrumental constraints in order to achieve a correct test. The theoretical developments of the proposed method and its application for low-cost mass production test are described in Section 3. Several experimental validations are presented in Section 4. Finally, Section 5 gives some concluding remarks.

2. ADC TEST

2.1. Conventional ADC test

Real-life ADCs are affected by errors, usually classified in two types [1, 10, 11]:

(a) stochastic errors: noise, aperture uncertainty (jitter), and coupling between analog and digital part;
(b) deterministic errors: nonlinearities, distortion.

Several parameters are defined in order to characterize and test ADCs [12, 13]. The traditional dynamic parameters are total harmonic distortion (THD), spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SINAD). The critical static parameter is the integral nonlinearity (INL). The above set of parameters can be derived [11, 14, 15] or computed [1] from the harmonic values and/or the noise value. A very common way to evaluate these harmonic and noise values of a given converter relies on spectral analysis, that is, to apply a single-tone sine wave to the converter input and compute the FFT on the output signal.

DSP-based method is usually used in order to measure these parameters. The typical DSP-based test architecture is described in Figure 1. The analog stimulus is usually generated by an AWG, and the output signal is captured and stored in a logic analyzer.

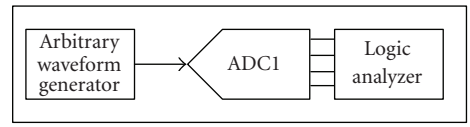

Figure 1: DSP-based test architecture.

Table 1: Common H2 amplitude versus converter resolution.

Converter resolution	Common H2 (dB)
12	−88
10	−73
8	−55

In order to achieve a correct evaluation of the ADC parameters, there are some constraints concerning the instrument performances and in particular for the AWG. Indeed, an ideal test signal is a pure sine wave, but a real-life signal applied to the converter input is obviously deteriorated by the noise and the harmonics induced by the AWG. Clearly, the noise and the harmonic levels of the test signal should be low enough to be negligible in front of the noise and harmonics induced by the converter under test. The condition for an accurate evaluation of the ADC parameters is therefore the use of an AWG with better performances than the ADC under test. Sections 3 and 4 detail this condition regarding the noise and the harmonic distortions induced by the AWG.

2.2. Harmonic distortions induced by the AWG

We only focus on harmonic estimation. Indeed, the method developed in [16] can be used to estimate noise features in a similar test configuration to the one proposed in this paper. This method uses one generator to supply the same test signal simultaneously for two ADCs under test. These two ADCs share the same sampling clock. Using the properties of correlated noise sources disturbing both ADCs, by simple postprocessing calculations, it is possible to discriminate the noise provided by each ADC under test from the one induced by external sources.

To illustrate the influence of the AWG on harmonics measurements, we only consider the second-order harmonic, H2, but similar behavior could be obtained with other harmonics. Table 1 gives an idea of H2 amplitude that could be induced by converters according to practical experiments and datasheets.

As previously explained, AWG consists of a DAC with harmonic distortions. Consequently, if we consider a sine wave generated by an AWG and converted by an ADC, the digital signal at the output of the ADC is deteriorated by both components. In the worst case, the H2 amplitude induced by both sources can be summed. Table 2 gives the true H2 amplitude of the tested ADC, and the measured H2 amplitude considering the influence of the AWG.

Table 2: H2 measurement, ADC versus DAC/ADC setup.

Test configuration	True H2 (dB)	Measured H2 (dB)
8-bit ADC tested using 8-bit DAC	−55.0	−49.0
8-bit ADC tested using 10-bit DAC	−55.0	−54.0
8-bit ADC tested using 12-bit DAC	−55.0	−54.8

It can be seen that the correct estimation of the ADC harmonics requires the use of an AWG with a resolution at least 2 bits higher than the resolution of the ADC under test.

3. METHODOLOGY

Section 2 has demonstrated that there are strong constraints on the test instrument performances to be able to perform conventional ADC test applying the DSP-based method.

This section presents a test method for mass-production testing of ADC harmonic distortions using low-cost testers. A low-cost tester may be defined as a tester embedding low-end AWGs that would not be efficient enough to apply a conventional DSP-based test. As a rule of thumb, the price of a time slot for a tester that embeds some high-performance analog instruments is commonly twice the price of a time slot for a tester composed of digital channels and low-performance analog instruments. The theoretical fundamentals are given in the first part. Section 4 describes the first step of the method that consists in estimating the AWG-harmonic contribution. Section 5 is dedicated to the production test stage in which ADCs are tested using a postprocessing correction of the AWG errors.

3.1. Theoretical fundamentals

Let us consider a sine wave applied to an ADC. Using a Fourier series expansion, the output signal can be expressed by (1). In this equation, we distinguish the quantized sine-wave $x(n)$ that would be obtained if the ADC was ideal and the sum of all the harmonic values introduced by static and dynamic nonlinearity of the converter [11]

$$s(n) = x(n) + \sum_{k\geq 0} H\mathrm{conv}_k^{\mathrm{Amp}} \cos(k(\theta_n + \theta_0) + \theta_k), \qquad (1)$$

where n is the sample index, θ_0 the initial phase shift, θ_k the phase shift induced by dynamic nonlinearity, $H\mathrm{conv}_k^{\mathrm{Amp}}$ the amplitude of the kth harmonic H, induced by the converter, named conv, and θ_n is the nominal sampling phase given by

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n, \qquad (2)$$

where P is the number of cycles (i.e., signal periods) and M the number of samples in the test record.

In Section 4, we will restrict our study to static nonlinearity contributions, which are dominant in most of ADC architectures, especially for those using a sample-and-hold in the input circuitry. The effects of the other contributions, mainly due to parasitic elements, will be evaluated in further studies.

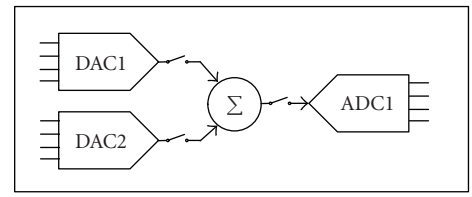

Figure 2: Hardware setup for test development.

Equation (3) is the simplification of (1) considering only static nonlinearities

$$s(n) = x(n) + \sum_{k\geq 0} H\mathrm{conv}_k^{\mathrm{Amp}} \cos(k(\theta_n + \theta_0)). \qquad (3)$$

Equation (3) may also apply to a DAC and can thus be used to express the signal generated by an AWG.

3.2. Learning AWG harmonic contribution for postprocessing

According to [16] and considering a system of two DACs and one ADC connected by a set of switches and a combiner as illustrated in Figure 2, it is possible to discriminate the harmonic contribution of the three converters. The idea is to exploit different configurations and test conditions in order to separate the harmonic contribution of each converter.

Let us consider a test configuration in which the output of DAC1 is directly connected to the ADC1 input. The spectrum of the output signal can be computed and we can extract the values of the harmonics H_k. Obviously, the output signal is impacted by errors of both converters. In other words, the measured spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of ADC1. According to (4), setting a zero initial phase shift, we can write the following:

$$H\mathrm{meas}_k = H_k^m = (H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{adc1}_k^{\mathrm{FS}}). \qquad (4)$$

In this equation, we assume that amplitudes of harmonics created by the DAC are negligible with respect to the fundamental amplitude of the signal. In this way, we can consider that the ADC is driven by a single-tone signal.

Equation (4) establishes a relation between the harmonic contributions of the two converters involved in the test configuration. In this equation, the left member is known and corresponds to the amplitude of the kth spectral bin measured at the output of the ADC, while the right member represents the unknowns. This relation is possible because at first we fix the initial to zero ($\theta_0 = 0$), and there is no dynamic nonlinearity ($\theta_k = 0$).

This example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the new test method. By using different configurations—DAC1/ADC1, DAC2/ADC1, or DAC1+DAC2/ADC1—we are able to obtain a set of different equations. So, with an adequate set of configurations

(i.e., system of five independent (5)), we are able to discriminate the harmonic contribution of each converter

$$\begin{aligned} H_k^{m,a} &= H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{adc1}_k^{\mathrm{FS}}, \\ H_k^{m,b} &= H\mathrm{dac2}_k^{\mathrm{FS}} + H\mathrm{adc1}_k^{\mathrm{FS}}, \\ H_k^{m,c} &= H\mathrm{dac2}_k^{\mathrm{FS/2}} + H\mathrm{adc1}_k^{\mathrm{FS/2}}, \\ H_k^{m,d} &= H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{dac2}_k^{\mathrm{FS/2}}\cos(k\pi) + H\mathrm{adc1}_k^{\mathrm{FS/2}}, \\ H_k^{m,e} &= H\mathrm{dac1}_k^{\mathrm{FS}} + H\mathrm{dac2}_k^{\mathrm{FS/2}}\cos(k\varphi_1) + H\mathrm{adc1}_k^{\mathrm{FS}}\cos(k\varphi_2) \end{aligned} \tag{5}$$

with $\varphi_1 = \pi - 2arcos(1/4)$, $\varphi_2 = \pi - arcos(1/4)$.

Note that the combiner influence is neglected in the development of this method. Indeed, the combiner used for further experimentations is a fully resistive element. As a consequence, noise should be the main contribution of this element. This assumption has been verified during practical experimentation.

A system of a two-channel AWG has two DACs. If we connect this system to an ADC by set of switches and a combiner, we obtain the setup required for our method. Therefore, it is possible to apply this method to estimate the harmonic contribution of the AWG in the objective to perform a postprocessing correction of this AWG to test ADCs.

3.3. Mass production test using postprocessing correction

The method described in Section 2 permits to estimate the harmonic contributions of the AWG and the tested ADC. Five test configurations are required to achieve this estimation.

After one application of the whole method, if we change the ADC and repeat the complete procedure, we will have a new test result for the ADC under test, but still the same AWG contribution. In fact, once the AWG is characterized, there is only one unknown in (4). Solving this equation, it is therefore possible to determine the harmonic contribution of every new ADC using only one test.

In summary, considering mass production test, we need to apply the five required test configurations in order to estimate the AWG harmonic contribution. Then we only need one additional test per ADC under test and the ADC harmonic contribution is estimated by performing a postprocessing correction of the AWG contribution. As a consequence for mass production test, the test time required to extract the AWG contribution with the five test configurations is negligible compared to total testing time. In other words, the test time required to apply our method is completely comparable to the test time required to apply a conventional ADC test. However, there is no need of AWGs with higher performances than the ADC under test.

4. EXPERIMENTAL VALIDATIONS

Large sets of hardware measurements have been performed to validate the proposed approach. The purpose of the experimentation is to evaluate the efficiency of our method to accurately test an ADC using an AWG of the same resolution. The experimental setup is first introduced, then the protocol is described, and finally results are presented. The performance of the proposed test strategy is evaluated by comparing the THD and SFDR [12, 13].

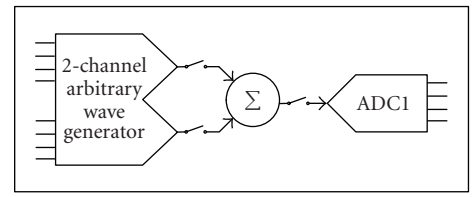

Figure 3: Experimental test setup.

Table 3: Test results for the standard test using low-resolution AWG versus reference test setup.

	THD (dB)	SFDR (dB)
Standard test with AWG2021	−51.6	52.5
Reference test	−68.4	63.5

4.1. Experimental setup

In order to experiment the test strategy, we use a two-channel AWG Sony/Tektronix AWG2021 containing two 12-bit DACs, a resistive splitter/combiner, and a 10-bit ADC, as presented in Figure 3.

Moreover, to compare the results of our method to a conventional ADC test, some reference measurements have been performed using a standard test setup with high-performance analog generator.

Finally, to demonstrate that the AWG is not efficient enough to accurately characterize the ADC dynamic performances without the proposed method, the conventional DSP-based method has been implemented by directly connecting one output of the AWG to the input of the ADC. Table 3 presents the results of this test in comparison with the reference measurements regarding THD and SFDR test parameters.

An error of more than 16 dB is observed on the estimation of the THD, and more than 11 dB on the estimation of the SFDR. This clearly demonstrates that despite the AWG has a resolution 2 bits higher than the ADC under test, it is not efficient enough to set up an accurate DSP-based test. It has been demonstrated in Section 2.2 that a test instrument must have a resolution at least 2 bits higher than the ADC under test resolution to get reliable results. Nevertheless, we observed that a 12-bit resolution for the AWG is not high enough to accurately test a 10-bit ADC because it exhibits worse performances than common 12-bit converters in terms of THD and SFDR.

4.2. Experimental protocol

In order to validate the method, four ADCs of the same batch have been tested. These four samples were chosen in order to

Table 4: Estimated values of the AWG harmonic components using the 5-test procedure.

	Estimation of AWG harmonics				
	Using ADC#1	Using ADC#2	Using ADC#3	Using ADC#4	σ
H2 (dB)	−59.5	−60.1	−58.7	−58.1	0.9
H3 (dB)	−52.0	−52.1	−52.2	−52.3	0.1
H4 (dB)	−79.7	−77.1	−86.4	−90.6	6.2
H5 (dB)	−84.1	−87.5	−90.7	−94.0	4.2
H6 (dB)	−88.7	−82.9	−84.4	−83.6	2.6
H7 (dB)	−94.5	−108.8	−107.6	−120.9	10.8
H8 (dB)	−93.5	−97.2	−87.9	−85.0	5.5
H9 (dB)	−94.9	−84.3	−91.3	−88.3	4.5
H10 (dB)	−93.7	−105.3	−87.3	−82.7	9.8

Table 5: Average THD measurements reference test versus 1-test procedure.

	THD reference (dB)	THD estimation (dB)	Measurement difference (dB)
ADC#1	−66.6	−67.3	0.7
ADC#2	−68.1	−66.7	−1.4
ADC#3	−62.6	−62.4	−0.2
ADC#4	−60.5	−60.6	0.1

Table 6: Average SFDR measurements reference test versus 1-test procedure.

	SFDR reference (dB)	SFDR estimation (dB)	Measurement difference (dB)
ADC#1	68.7	67.9	0.8
ADC#2	70.1	70.0	0.1
ADC#3	67.0	66.7	0.3
ADC#4	63.3	62.1	1.2

represent a significant population of converters considering the SDFR and THD variations. Indeed, these samples have THD varying from −60.5 dB to −68.3 dB and SFDR varying from 63.3 dB to 70.3 dB.

Each of these four ADCs has been tested with a conventional ADC test procedure to obtain reference measurements. The test has been performed ten times to estimate the repeatability of the technique. The evaluated dynamic parameters are the THD and the SFDR.

Then the proposed method has been applied considering both the 5-test procedure used in the preliminary learning phase and the 1-test procedure used during production test. As for the conventional ADC test, the THD and the SFDR parameters are computed from the estimated values of the harmonic components. Again, the test has been performed ten times on each ADC.

4.3. Experimental results of the full test procedure

4.3.1. Learning phase validation

In order to validate the learning phase that permits to characterize the AWG, the 5-test procedure described in Section 3.2 has been applied to the four-sampled ADCs. Results are presented in Table 4 that gives the estimated values of the harmonic components induced by the AWG for 2nd to the 10th harmonics. The last column gives the standard deviation for each harmonic considering the four estimations using the 5-test procedure with 4 different ADCs.

Analyzing these results, it appears that the amplitude of the most significant harmonic components is well estimated when taking into account the different converters used during the 5-test procedure. More precisely in this experiment, the major contributors to the AWG harmonic distortion are the H2 and H3 components. Similar values are obtained for the amplitude of these components whatever the converter used during the procedure (around −59 dB for the H2 harmonic and −52 dB for the H3 harmonic, with a standard deviation of less than 1 dB). For harmonic components with lower amplitude, results show a larger spread depending on the converter used during the procedure. In fact, these harmonics are nearby or below the noise floor and they are not relevant. As a consequence, even a rough estimation of these harmonics will not strongly impact the test-procedure efficiency.

In summary, these results demonstrate that the 5-test procedure allows the extraction of the amplitude of the most significant harmonic components induced by the AWG with a good accuracy, whatever the converter used during the procedure.

4.3.2. Production test validation

Using the AWG harmonic distortion estimated during the learning 5-test procedure, we defined a postprocessing on the response of the ADC under test. The objective of this section is to validate the effectiveness of this postprocessing correction of AWG errors in order to accurately test subsequent ADCs with only a 1-test procedure per ADC.

Table 7: THD estimation accuracy versus AWG resolution.

	AWG resolution	THD reference (dB)	THD estimation (dB)	Measurement difference (dB)
ADC#1	12	−61.8	−61.7	−0.1
	10	−61.8	−62.0	0.2
	8	−61.8	−62.4	0.6
	6	−61.8	−61.7	−0.1
ADC#2	12	−59.8	−59.1	−0.7
	10	−59.8	−58.8	−1.0
	8	−59.8	−58.9	−0.9
	6	−59.8	−59.1	−0.8

Table 8: SFDR estimation accuracy versus AWG resolution.

	AWG resolution	SFDR reference (dB)	SFDR estimation (dB)	Measurement difference (dB)
ADC#1	12	63,9	65,1	−1,2
	10	63,9	64,7	−0,8
	8	63,9	65,4	−1,5
	6	63,9	66,0	−2,1
ADC#2	12	63,0	62,8	0,2
	10	63,0	62,6	0,4
	8	63,0	61,8	1,2
	6	63,0	62,1	0,9

To this aim, we consider the amplitude of the AWG harmonic components extracted with the 5-test procedure using ADC#1. Then the 4 samples of ADCs are tested ten times using the 1-test procedure described in Section 3.3, and postprocessing correction on the response of the DUT is performed to remove the AWG contribution. Results are presented hereafter in comparison with the reference measurements obtained using a conventional ADC test setup and a high-performance AWG.

Table 5 gives the average THD measurements for the four ADC samples tested ten times, using either a conventional ADC test (2nd column) or the 1-test procedure with postprocessing correction (3rd column). Each result is the average of ten measurements. The last column gives the difference between the two measurements.

Table 5 shows that the maximal difference between the proposed method and a conventional ADC test is less than 1.5 dB. This result is very interesting especially when we consider the repeatability of the measurement for the same product on ATE that is around 1 dB.

Results for the SFDR estimation are given in Table 6. As for the THD measurements, we have good estimations. The estimation uncertainty (1.2 dB) is in the same range of the test production scattering (1.3 dB) on the SFDR measurement for the same ADC.

All these results demonstrate that once the harmonic contribution of the AWG has been extracted in the initial learning phase, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and postprocessing correction.

4.4. Test production validation versus AWG resolution

4.4.1. Introduction

The conclusion of the first experiments is twofold. At first, the 5-test procedure, also called learning phase, gives a stable estimation of the amplitudes of the most significant harmonic components induced by the AWG whatever the ADC used. This conclusion leads to the second experimentation. Indeed the second experimentation allows us to conclude that once the harmonic contribution of the AWG has been extracted in the initial learning phase, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and a postprocessing correction. These two first experiments were performed with a 12-bit AWG. It has been demonstrated (cf. Table 3) that this AWG is not efficient enough to accurately characterize the ADC dynamic performances using the standard DSP-based method. To go further, a third experiment has been carried out in order to estimate the lowest resolution acceptable for the AWG relatively to the accuracy of the new production test results.

4.4.2. Experimental protocol

The test setup is similar to the previous one, that is, made of a Sony/Tektronix AWG2021, a resistive combiner, and a 10-bit ADC.

Two ADCs were tested, each converter being tested four times, each test being performed with a different AWG

resolution (from 12 bits to 6 bits, by steps of 2 bits). We reduced the AWG resolution by increasing its quantization noise.

4.4.3. Experimental results

Table 7 presents the results of THD measurements for the two ADCs. Three different results are given

(i) reference measurement made with a high-performance AWG in a conventional test setup;
(ii) estimation with our method;
(iii) estimation error.

Table 8 gives the same kind of results as Table 7, but for a different dynamic parameter: SFDR.

Production test repeatability usually shows variations of dynamic parameter estimations of around 1.5 dB. Considering this limit of acceptance for dynamic parameter estimations, Tables 7 and 8 give positive results. Indeed, considering THD estimation for both ADCs, whatever the AWG resolution between 12 bits and 6 bits, there is no estimation error over 1.5 dB. Considering SFDR parameter estimation, there is only one error estimation over this limit; this is for the ADC#1 tested with a 6-bit AWG.

The fact that the limit has not been exceeded for the test of ADC#2 can be explained by the difference between the two ADCs reference measurements. Indeed, the SFDR reference of ADC#1 is better than the one of ADC#2. In other words, for ADC#1 the highest spurious harmonic is closer to the noise level than for ADC#2. As a consequence, the noise contribution to this spurious harmonic is higher. As the noise contribution is random, it induces some measurement variations and errors higher for ADC#1 than for ADC#2.

From the experimental results, we can conclude that the harmonic distortion generated by the AWG is not anymore a limiting factor for most ADCs testing. For example, let us consider a 10-bit ADC. In order to set up a conventional test, the AWG resolution must be at least of 12 or 13 bits. Using the proposed new approach, the constraints on AWG resolution can be considerably relaxed.

5. CONCLUSION

In this paper, we propose an ADC test solution based on the estimation of ADC harmonics and a postprocessing correction of AWG errors on the test response. The method relies on a preliminary learning phase in which the AWG harmonic contribution is estimated. The AWG characteristics are then used during production test with a postprocessing correction of the test data in order to remove the AWG contribution.

Thanks to the proposed method, it is possible to accurately measure ADC harmonics using an ATE with standard-performance AWG, whereas a conventional DSP-based test requires an AWG with a resolution at least 2 bits higher than the ADC under test. This method can be associated to the 2-ADC method [8], that is suited to noise measurements in a test setup similar to the one required to apply the novel method. Indeed, using these two methods we can test all the ADC dynamic test parameters. As a consequence, one of the main benefits of the method is that it allows the test of a wide range of converters with the same standard test equipment, and without the need of customising the test board for every new product. Moreover, after the learning phase, there is no additional test time compared with a conventional ADC test procedure. To go further, it has been proven that using this new approach the constraints on AWG resolution can be considerably relaxed. The validation has been achieved with some 10-bit ADCs. From an industrial point of view, this method is interesting for high-resolution converters. As a consequence, the next experimental validation would be done on higher resolution converters. The same type of ADCs is used for the learning step and the industrial test step of the validations. The approach should still be valid if the two steps were made with different types of converters, at the condition that the AWG settings (frequency and amplitude of the sine wave) are kept both steps.

The theoretical developments have been made under the assumptions that the combiner has no distortion influence and that the ADC is not influenced by dynamic nonlinearity. The combiner influence has been verified during practical experimentations. The ADC used for practical experimentations was not influenced by dynamic nonlinearity. Further theoretical developments would be done in order to take into account ADC architectures that do not prevent dynamic nonlinearity.

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