



**HAL**  
open science

# High Launch Switching Activity Reduction in At-Speed Scan Testing using CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme

Kohli Miyase, Hideo Furukawa, Patrick Girard, Xiaoqing Wen, Yuta Yamato, Seiji Kajihara, Laung-Terng Wang, Mohammad Tehranipoor

► **To cite this version:**

Kohli Miyase, Hideo Furukawa, Patrick Girard, Xiaoqing Wen, Yuta Yamato, et al.. High Launch Switching Activity Reduction in At-Speed Scan Testing using CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme. IEICE Transactions on Information and Systems, 2010, E93-D (1), pp.2-9. 10.1587/transinf.E93.D.2 . lirmm-00406963

**HAL Id: lirmm-00406963**

**<https://hal-lirmm.ccsd.cnrs.fr/lirmm-00406963>**

Submitted on 17 Jul 2020

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# High Launch Switching Activity Reduction in At-Speed Scan Testing Using CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme\*

Kohei MIYASE<sup>†</sup>, Xiaoqing WEN<sup>†</sup>, Members, Hiroshi FURUKAWA<sup>†</sup>, Nonmember, Yuta YAMATO<sup>†</sup>, Student Member, Seiji KAJIHARA<sup>†</sup>, Member, Patrick GIRARD<sup>††</sup>, Laung-Terng WANG<sup>†††</sup>, and Mohammad TEHRANIPOOR<sup>††††</sup>, Nonmembers

**SUMMARY** At-speed scan testing is susceptible to yield loss risk due to power supply noise caused by excessive launch switching activity. This paper proposes a novel two-stage scheme, namely CTX (Clock-Gating-Based Test Relaxation and X-Filling), for reducing switching activity when a test stimulus is launched. Test relaxation and X-filling are conducted (1) to make as many FFs as possible inactive by disabling corresponding clock control signals of clock-gating circuitry in Stage-1 (Clock-Disabling), and (2) to equalize the input and output values in Stage-2 of as many remaining active FFs as possible (FF-Silencing). CTX effectively reduces launch switching activity and thus yield loss risk even when only a small number of don't care (X) bits are present (as in test compression) without any impact on test data volume, fault coverage, performance, or circuit design.

**key words:** power supply noise, test relaxation, X-filling, clock-gating, test compaction

## 1. Introduction

At-speed scan testing is necessary to improve timing-related test quality [1]. It is realized by *launching* a transition at the start-point of a path and *capturing* its response at the end-point of said path at the system speed. In practice, the *launch-on-capture (LOC)* clocking scheme is widely used for at-speed scan testing [1].

Figure 1 shows the essence of the LOC clocking scheme: After a test vector is loaded through a series of shift clock pulses of which  $S_L$  is the last (where  $L$ : the length of the longest scan chain), transitions are launched by the first capture clock pulse,  $C_1$ , at the corresponding scan FFs. Transitions are caused by the difference between the values shifted-in by  $S_L$  and the values captured by  $C_1$ . The *test cycle* between the transitions launch ( $C_1$ ) and the response capture ( $C_2$ ) is the rated system clock period.

Although at-speed scan testing is indispensable for improving timing-related test quality [1], its applicability is severely limited by *test-induced yield loss*, which occurs

when functionally good chips fail only during at-speed scan testing [2]–[4]. The major causes of this problem are power supply noise (i.e. IR-drop and ground bounce), which are caused by excessive *launch switching activity* at  $C_1$  and result in an increase in delay. A 10% drop in power supply voltage has been shown to be capable of increasing path delay by 30% [5]. Obviously, this may result in capture failures at  $C_2$  [4], thus leading to test-induced yield loss [6]–[8]. This problem is worsening rapidly amongst deep-submicron and low-power chips [6]. Therefore, there is an urgent need to reduce the yield loss risk induced by excessive power supply noise.

Previous techniques for reducing launch switching activity are based on the following three approaches:

- (1) **Hardware Limitation:** The number of capturing-FFs at  $C_1$  (Fig. 1) can be reduced via circuit modification [9], one-hot clocking [1], or capture clock staggering [1]. However, this approach may cause significant ATPG change, test data inflation, and even fault coverage loss to be incurred.
- (2) **Low-Capture-Power ATPG:** 0's and 1's in test vectors can be carefully generated through such techniques as input-output equalizing at FFs [10], clock-gating, etc. to reduce launch switching activity. However, this approach may cause significant test data inflation and/or take a long amount of CPU time.
- (3) **Test Relaxation & X-Filling:** *Test relaxation* is to identify don't-care bits (X-bits) from a set of fully-specified test vectors while maintaining fault coverage [11], [12]. Once this has been done, *X-filling* is conducted on the resulting partially-specified test cubes

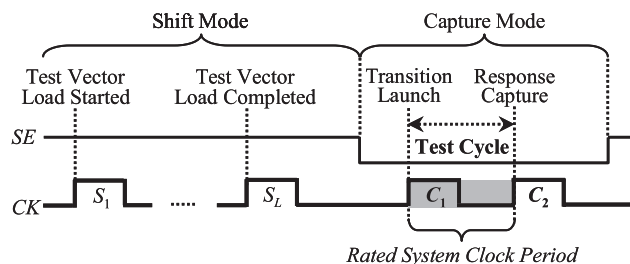


Fig. 1 LOC-based at-speed scan testing.

Manuscript received February 6, 2009.

Manuscript revised May 29, 2009.

<sup>†</sup>The authors are with Kyushu Institute of Technology, Iizuka-shi, 820–8502 Japan.

<sup>††</sup>The author is with LIRMM, France.

<sup>†††</sup>The author is with SynTest, USA.

<sup>††††</sup>The author is with University of Connecticut, USA.

\*A previous version of this paper has been published at Asian Test Symposium 2008.

DOI: 10.1587/transinf.E93.D.2

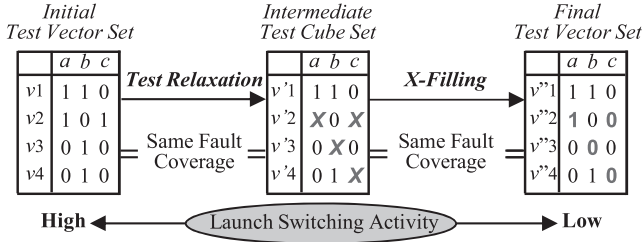


Fig. 2 Concept of test relaxation and X-filling.

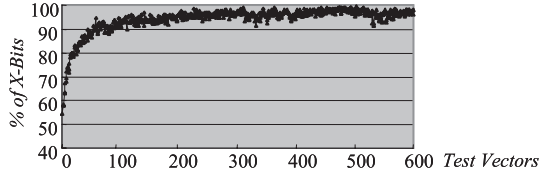


Fig. 3 X-bit distribution for an industrial circuit.

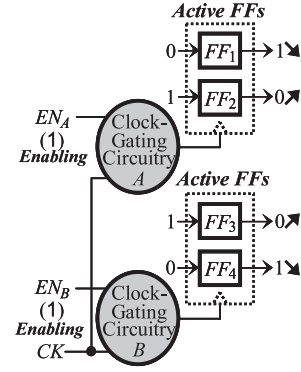
to equalize the input and output values of as many FFs as possible [13]–[15]. Launch switching activity is reduced in this way. The concept of this approach is illustrated in Fig. 2.

The test relaxation & X-filling approach is practical as a simple post-ATPG processing method since it reduces launch switching activity without affecting test data volume, fault coverage, performance, or circuit design. However, this approach has one major limitation: if the number of X-bits identified from a test set is small, its reducing effect on launch switching activity may be insufficient. Such an X-bit shortage may be caused by test compaction or test compression. Figure 3 shows an example of an industrial circuit (600 K gates and 600 transition delay test vectors) for which test vectors obtained at the early stages of test generation have few (60% or less) X-bits.

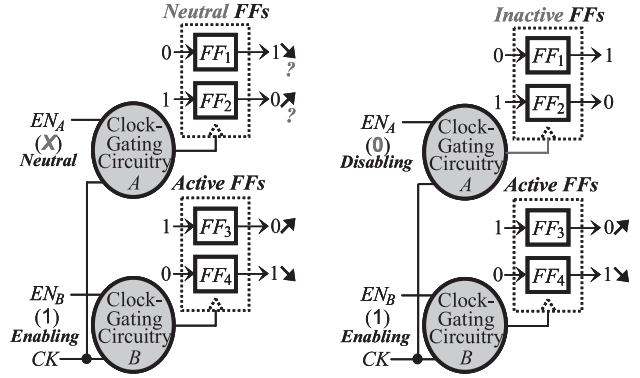
Therefore, there is an urgent need to improve the test relaxation & X-filling approach so as to effectively reduce launch switching activity even when only a small number of X-bits are available, as in test compaction and test compression. This paper outlines the achievement of this goal through the implementation of a novel two-stage scheme: *CTX* (*Clock-Gating-Based Test Relaxation and X-Filling*). The basic idea of this approach is to make sophisticated use of clock-gating in test relaxation & X-filling, as illustrated in Fig. 4.

Figure 4 (a) illustrates four FFs controlled by two clock control signals,  $EN_A$  and  $EN_B$ , whose values are 1 for the initial test vector. This means that all of the FFs are *active* (i.e. capturing) at  $C_1$  (Fig. 1), resulting in four initial launch transitions. CTX consists of the following two stages:

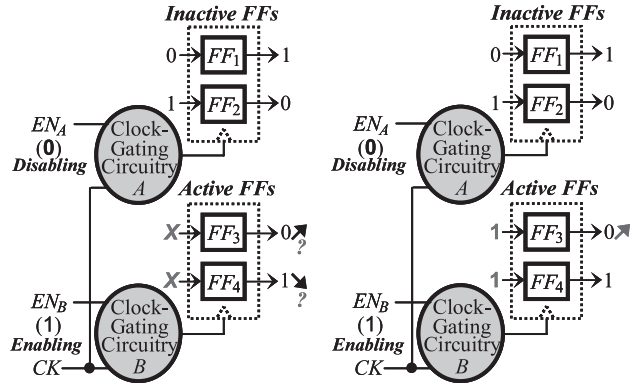
- **Stage-1 (Clock-Disabling):** Test relaxation is first conducted to turn as many enabling clock control signals (value = 1) as possible into *neutral* ones (with = X), as shown in Fig. 4 (b); X-filling is then conducted to turn as many neutral clock control signals as possible into disabling ones (value = 0), as shown in Fig. 4 (c).



(a) State for Initial Test Vector



(b) After Test Relaxation in Stage-1 (c) After X-Filling in Stage-1



(d) After Test Relaxation in Stage-2 (e) After X-Filling in Stage-2

Fig. 4 Basic flow of CTX.

Since all FFs controlled by a disabling clock control signal (e.g.,  $FF_1$  and  $FF_2$ , in Fig. 4 (c)) are *inactive*, launch transitions are efficiently reduced in a collective manner.

- **Stage-2 (FF-Silencing):** Test relaxation is then conducted to turn as many active transition-FFs (input  $\neq$  output, e.g.  $FF_3$  and  $FF_4$  in Fig. 4 (c)) as possible into neutral-FFs (input or output = X, e.g.  $FF_3$  and  $FF_4$  in Fig. 4 (d)), after which X-filling (which attempts to equalize the input and output of a neutral-FF) is conducted to turn as many neutral-FFs as possible into non-transition-FFs (input = output, e.g.  $FF_4$  in

Fig. 4 (e)) by attempting to equalize the input and the output of a neutral-FF. In this way, the number of launch transitions at individual FFs is reduced.

The following are the major contributions of the CTX scheme:

- (1) *Clock-Disabling-Based Test Relaxation & X-Filling*: CTX fully explores the collective power-saving capability of clock-gating in at-speed scan testing.
- (2) *FF-Silencing-Based Test Relaxation & X-Filling*: CTX attempts to equalize the input and output values of the remaining active FFs to further reduce launch transitions at individual FFs.
- (3) *Non-Intrusive Use of Clock-Gating*: By using clock-gating throughout test data manipulation, CTX avoids causing any ATPG change, test data inflation, or fault coverage loss.
- (4) *X-Bit-Efficiency*: With clock-disabling and FF-Silencing, CTX significantly reduces launch switching activity even when only a small number of X-bits are available.

## 2. Background

### 2.1 Test Relaxation

As illustrated in Fig. 2, *test relaxation* is the process of identifying don't-care bits (X-bits) from a fully-specified test vector set,  $V$ , to create a partially-specified test cube set,  $C$ , while guaranteeing that some properties of  $V$  are preserved by  $C$ . Such properties include stuck-at fault coverage [11], transition delay fault coverage [12], and even all sensitized paths for transition delay fault detection [15].

X-bits can also be obtained directly from test generation by disabling random-fill. However, this increases ATPG time and test data volume. For example, the test vector count increased by 144.8% when random-fill was disabled to leave X-bits for low-power X-filling [13]. Thus, it is preferable to apply maximum test compaction with random-fill to generate an initial *fully-specified* compacted test set, and then use test relaxation to create *partially-specified* test cubes. Compaction followed by relaxation results in a compact final test set with additional benefits after X-filling is conducted [13]–[15].

### 2.2 X-Filling

As illustrated in Fig. 2, *X-filling* is the process of assigning logic values to the X-bits in a test cube for a specific purpose. In this paper, X-filling is used to reduce *launch switching activity (LSA)*, which occurs at  $C_1$  (Fig. 1). Many *low-LSA X-filling* techniques have been proposed [13]–[15], and Fig. 5 illustrates one of them, called *JP-fill* [15].

**JP-Fill:** In Fig. 5, the test cube is  $c = \langle 10XX \rangle$  and the logic function of the combinational portion is  $F$ . Thus,  $\langle c: PPI \rangle = \langle 0XX \rangle$  and  $\langle F(c): PPO \rangle = \langle XXX \rangle$ . First, **justification** (①) is conducted in an attempt to assign 0 to  $p_2$ ,

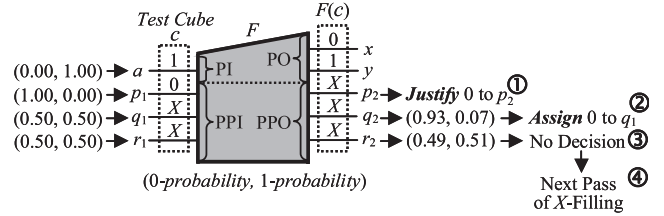


Fig. 5 Concept of JP-Fill.

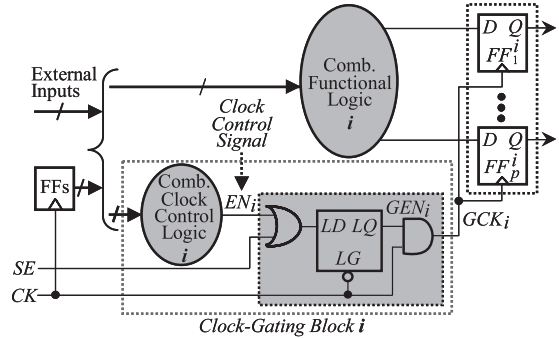


Fig. 6 Example scheme of clock-gating.

since  $p_1$  is 0. Then, the 0 and 1 probabilities of each PPO X-bit for bit-pairs  $q_1$ - $q_2$  and  $r_1$ - $r_2$  of the form X-X are calculated by setting the 0 and 1 probabilities for each input X-bit to 0.50, after which *probability propagation* is conducted. Since the 0-probability (0.93) of  $q_2$  is significantly larger than its 1-probability (0.07), it is reasonable to assign 0 to  $q_1$  (②). However, since the 0-probability (0.49) of  $r_2$  is nearly equivalent to its 1-probability (0.51), no decision is made for  $r_1$  (③). In this case, 3-valued logic simulation is performed, and one more pass of JP-Fill (④) is conducted with justification and/or probability propagation.

In essence, JP-fill uses justification and multiple passes to improve the effectiveness of X-filling, while its scalability is improved through probability propagation. In this way, JP-fill achieves effectiveness and scalability in a balanced manner.

### 2.3 Clock-Gating

*Clock-gating* is the most widely used power management mechanism in practice. Figure 6 shows an example scheme.

A circuit may contain multiple clock-gating blocks. Figure 6 shows the  $i$ -th such block, which is enhanced for scan testing. In shift mode ( $SE = 1$ ), all FFs are constantly driven by the clock  $CK$  so that the shift operation is properly conducted. The *clock control signal* ( $EN_i$ ) is generated at the rising edge of  $CK$  and takes over control of  $GEN_i$  in capture mode ( $SE = 0$ ).  $GEN_i$  is then ANDed with  $CK$  to create the *gated clock*  $GCK_i$  that is directly connected to the FFs.

Clock-gating can be used to reduce launch switching activity in capture mode. This is achieved by setting  $EN_i$  to 0 at the last shift pulse,  $S_L$ . This way, the launch capture

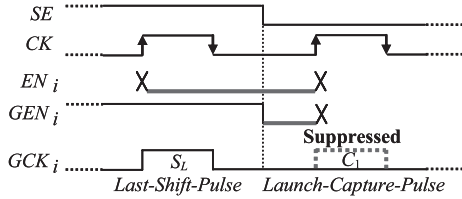


Fig. 7 Clock-gating for reducing launch switching activity.

clock pulse ( $C_1$  in Fig. 1) is suppressed as shown in Fig. 7, and no FFs controlled by  $GCK_i$  (i.e.  $FF_1^i \sim FF_p^i$  as shown in Fig. 6) will capture. In other words, launch transitions at the FFs are reduced in a *collective* manner.

**Definition 1:** If the clock of a FF is a gated clock, the FF is called a *clock-gated FF*; otherwise, the FF is called a *non-clock-gated FF*. A group of FFs controlled by the same gated clock is called a *clock-gated FF group*. For example, Fig. 4 shows two clock-gated FF groups:  $\{FF_1, FF_2\}$  and  $\{FF_3, FF_4\}$ . Note that all FFs connected through one clock tree are considered one clock-gated FF group.

The capability of clock-gating to collectively reduce launch switching activity by disabling the clock for a group of FFs makes it a highly effective technique in terms of reducing yield loss risk in at-speed scan testing, especially when the percentage of available X-bits in a test cube is low (such as in test compaction and test compression, where the effect of conventional X-filling on LSA reduction is often limited).

From an ATPG point of view, clock-gating can be utilized by implementing either of the following two basic approaches:

**Approach-1 (Detection-Oriented):** Test generation is conducted in a manner that activates as many clocks for FFs as possible (i.e. disabling clock-gating) in order to make more FFs available for launch and capture in transition fault detection. Most commercial ATPG systems use this approach explicitly or implicitly. This leads to a smaller test set, higher fault coverage, and shorter CPU time, at the cost of higher launch switching activity.

**Approach-2 (Reduction-Oriented):** In test generation, clock-gating can be used aggressively to reduce launch switching activity. However, this reduces the number of FFs available for launch and capture in transition fault detection, leading to test vector count inflation, a longer CPU time, and even fault coverage loss under certain conditions.

In practice, it is preferable to use the detection-oriented approach (Approach-1) to generate a compact initial test set, and then convert it into a final test set with reduced launch switching activity by using CTX, the basic idea of which is illustrated in Fig. 4. The details of CTX are described in the following section.

### 3. The CTX Scheme

#### 3.1 Problem Formalization

The following is a problem regarding clock-gating-based

reduction of launch switching activity in at-speed scan testing:

Suppose that  $V_{initial}$  is a set of test vectors. Find a new set of test vectors,  $V_{final}$ , under the following conditions:

- (1) The fault coverage of  $V_{final}$  may not be less than that of  $V_{initial}$ .
- (2) The size of  $V_{final}$  must be equal to that of  $V_{initial}$ .
- (3) The peak launch switching activity of  $V_{final}$  must be lowered from that of  $V_{initial}$  to the greatest extent possible utilizing clock-disabling and FF-silencing.

#### 3.2 Basic Concept

This paper proposes a novel two-stage scheme, namely *CTX (Clock-Gating-Based Test Relaxation and X-Filling)*, to solve the preceding problem. The following are useful terms in describing the procedure of CTX:

**Definition 2:** If the value of a clock control signal,  $EN$ , under an input vector is logic 1 (0),  $EN$  is said to be *enabling (disabling)*. If the value is X,  $EN$  is said to be *neutral*. For example,  $EN_A$  in Fig. 4 (a), (b), and (c) are enabling, neutral, and disabling clock control signals, respectively.

**Definition 3:** If the clock for a FF or a clock-gated FF group is enabled (disabled), the FF or the clock-gated FF group is said to be *active (inactive)*. For example,  $FF_1$  and  $FF_2$  ( $FF_3$  and  $FF_4$ ) in Fig. 4 (c) are inactive (active) FFs. It can also be said that the clock-gated FF group  $\{FF_1, FF_2\}$  ( $\{FF_3, FF_4\}$ ) is inactive (active).

**Definition 4:** If the input and output of a FF have the *same (different)* logic value, the FF is said to be a *non-transition-FF (transition-FF)*. If the input or output of a FF is X, the FF is said to be a *neutral-FF*. For example, both  $FF_3$  and  $FF_4$  in Fig. 4 (d) are neutral-FFs. In Fig. 4 (e),  $FF_3$  is a transition-FF,  $FF_4$  is a non-transition-FF, and both of them are active.

CTX is based on the following two observations:

**Observation-1:** Not all enabling clock control signals necessarily need to be enabling. This exception occurs when a clock control signal is enabled to detect a fault in a test vector, but said fault is later detected by another test vector that does not require the clock control signal to be enabling.

**Observation-2:** Even if only one FF needs to be active for fault detection, all other FFs in the same clock-gated FF group also have to be active since they share the same clock control signal. This results in redundant transitions, especially when clock-gating is coarse-grained.

The basic concept of CTX is summarized in Fig. 8.

The first observation leads to Stage-1 (*Clock-Disabling*) of CTX, as shown in Fig. 8. Test relaxation is conducted to turn as many enabling clock control signals as possible into neutral ones, after which X-filling is conducted to convert as many neutral clock control signals as possible into disabling ones. In this way, launch switching activity can be reduced efficiently at the clock-gated FF group level

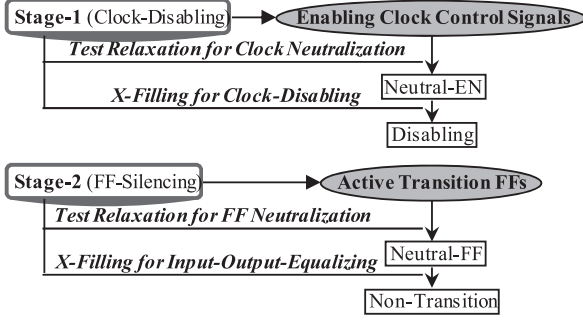


Fig. 8 Basic concept of CTX.

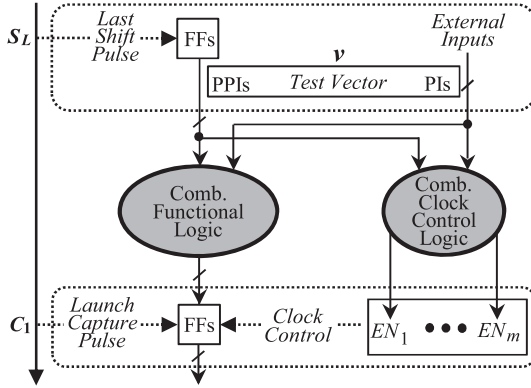


Fig. 9 Circuit model for CTX.

due to the collective reduction capability of clock gating.

The second observation leads to Stage-2 (*Input-Silencing*) of CTX, as shown in Fig. 8. Test relaxation is conducted to turn as many active transition-FFs as possible into neutral-FFs, after which *X*-filling is conducted to convert as many neutral-FFs as possible into non-transition-FFs. Subsequently, launch switching activity can be further reduced at the individual FF level.

An example of the basic flow of CTX when applied has been demonstrated in Fig. 4. In the following sections, the details of the CTX procedure are presented.

### 3.3 Circuit Model

Figure 9 shows a model of a circuit containing  $m$  clock-gating blocks, for the purpose of test generation in CTX.

In Fig. 9, signals related to the last shift pulse and launch capture pulse are surrounded by the dotted line, respectively. As shown in Fig. 9, a fully-specified test vector,  $v$ , is loaded at the rising edge of the last shift pulse,  $S_L$ .  $v$  consists of the PPI part ( $v$ : PPI) (which corresponds to the outputs of FFs) and the PI part ( $v$ : PI) (which corresponds to primary inputs). The combinational clock control logic circuitry produces  $m$  clock control signals,  $EN_1, EN_2, \dots, EN_m$ , which correspond to the  $m$  clock-gating blocks, as shown in Fig. 6. Each of the clock control signals may be disabling or enabling, and determines whether the corresponding clock-gated FF group is active

or not at launch capture pulse  $C_1$ . In the figure, the signals related to the clock activation are surrounded by the solid rectangles and the logic circuits are surrounded by the solid circles, respectively.

### 3.4 CTX Procedure

Based on the fundamental concept of CTX shown in Fig. 8, the CTX procedure can be described as follows. Note that the list of clock control signal line EN as shown in Fig. 6 can be obtained by a synthesis tool which inserts clock gating circuit.

#### Procedure of CTX:

**Input:**  $V^0 = \{v_i^0 \mid i = 1, 2, \dots, n\}$  // initial test set  
**Output:**  $V^2 = \{v_i^2 \mid i = 1, 2, \dots, n\}$  // final test set

#### Stage-1 (Clock-Disabling):

- (1-1) Obtain  $RS(v_i^0) = \{\text{bits in } v_i^0 \text{ that are reachable from at least one enabling clock control signal under } v_i^0\}$  for  $i = 1, 2, \dots, n$ .
- (1-2) Obtain  $T^1 = RS(v_1^0) \cup RS(v_2^0) \dots \cup RS(v_n^0)$ .
- (1-3) Conduct constrained test relaxation on  $V^0$  to turn as many bits in  $T^1$  into *X*-bits as possible while preserving the fault coverage of  $V^0$ . Denote the set of resulting partially-specified test cubes as  $C^1 = \{c_i^1 \mid i = 1, 2, \dots, n\}$ .
- (1-4) Try to justify 0 on each neutral clock control signal under  $c_i^1$  by assigning appropriate logic values to some *X*-bits in  $c_i^1$  for  $i = 1, 2, \dots, n$ .
- (1-5) Conduct low-LSA *X*-filling for the remaining *X*-bits in  $c_i^1$  for  $i = 1, 2, \dots, n$ . Denote the set of resulting fully-specified test vectors as  $V^1 = \{v_i^1 \mid i = 1, 2, \dots, n\}$ .

#### Stage-2 (FF-Silencing):

- (2-1) Obtain  $RF(v_i^1) = \{\text{bits in } v_i^1 \text{ that correspond to active transition-FFs under } v_i^1\}$  for  $i = 1, 2, \dots, n$ .
- (2-2) Obtain  $T^2 = RF(v_1^1) \cup RF(v_2^1) \dots \cup RF(v_n^1)$ .
- (2-3) Conduct constrained test relaxation on  $V^1$  to turn as many bits in  $T^2$  into *X*-bits as possible while preserving (1) the fault coverage of  $V^1$  and (2) the logic value of any clock control signal. Denote the set of resulting partially-specified test cubes as  $C^2 = \{c_i^2 \mid i = 1, 2, \dots, n\}$ .
- (2-4) Conduct low-LSA *X*-filling for the *X*-bits in  $c_i^2$  for  $i = 1, 2, \dots, n$ . Denote the set of resulting fully-specified test vectors as  $V^2 = \{v_i^2 \mid i = 1, 2, \dots, n\}$ .

### 3.5 Constrained Test Relaxation

The key operation within CTX procedure described above is *constrained test relaxation*, conducted on a fully-specified test set,  $V$ , to turn as many target bits in  $T$  into *X*-bits as possible while preserving (1) the fault coverage of  $V$  and (2) the logic values of target lines in  $S$ . The result is  $C$ , a set

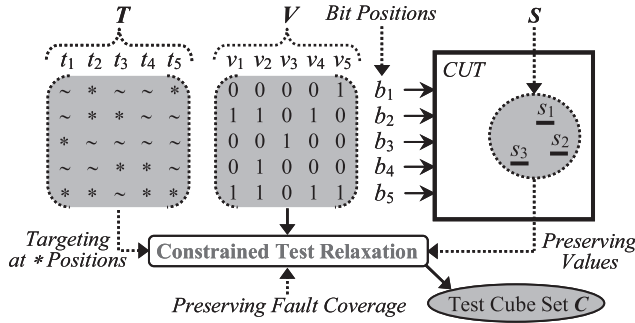


Fig. 10 Basic concept of constrained test relaxation.

of partially-specified test cubes. This process is illustrated in Fig. 10, where \* indicates a target bit position. Note that only fault coverage needs to be preserved in constrained test relaxation (S1-S3), where  $S = \emptyset$  can be assumed.

Constrained test relaxation is conducted via the following procedure, obtained by applying a basic, non-constrained test relaxation procedure that has previously been proposed [12].

#### Procedure of Constrained Test Relaxation:

**Input**  $V$ : set of fully-specified test vectors

$T$ : set of target bits

$S$ : set of target lines ( $= \emptyset$  in (1-3) of CTX)

**Output**  $C$ : set of resulting partially-specified test cubes

**S-1:** Identify all essential faults of  $V$  (each of which can only be detected by one test vector in  $V$ ) through an efficient procedure based on two passes of fault simulation.

**S-2:** Identify all bits in  $V$  whose logic values are necessary to (1) detect all essential faults and (2) preserve logic values of all target lines in  $S$ , in such a manner that bits in  $T$  are avoided to the greatest extent possible (such bits can be readily found by making use of the justification operation also widely used in ATPG). Then, convert the identified bits in  $V$  into X-bits, which results in an intermediate test cube set,  $C'$ .

**S-3:** Perform a 3-valued fault simulation on  $C'$  against all the non-essential faults of  $V$ . For all undetected, non-essential faults, identify the X-bits whose logic values in  $V$  are necessary to detect said faults in such a manner that bits in  $T$  are avoided to the greatest extent possible. Finally, in  $V$ , restore to the identified X-bits their original logic values. This results in the final test cube set,  $C$ .

The time complexity of the constrained test relaxation procedure is  $O(M \times N)$ , where  $M$  and  $N$  represent the number of faults and the number of test vectors, respectively.

## 4. Experimental Results

The CTX test generation scheme was implemented in C language and applied it two industrial circuits for evaluation experiments. The computer used in these experiments

Table 1 Basic information of industrial circuits.

Circuit	# Gates	# FFs	# Clock Gating Elements	# Gated FFs (%)	# Vec.	Test Cov. (%)
cir1	50k	1077	66	99.4	319	95.3
cir2	600k	35566	984	82.9	991	90.0

Table 2 Reduction ratio.

Circuit	Reduction Ratio of Launch Switching Activity		
	XID + Preferred	XID + JP	CTX
cir1	29.7	33.9	35.9
cir2	48.1	55.7	59.2

Table 3 CPU time.

Circuit	CPU Time (s)		
	XID + Preferred	XID + JP	CTX
cir1	85.84	96.98	149.31
cir2	3287.13	7033.69	11729.48

has a 2.8 GHz CPU and 32 GB memory. Transition LOC delay test vectors were generated using the ATPG tool ‘‘TetraMAX<sup>TM</sup>’’ from Synopsys. Table 1 shows the details of the circuits.

Three experiments were conducted using (1) XID with Preferred-Fill [13], (2) XID with JP-Fill [15], and (3) the proposed CTX scheme, where XID is a test relaxation system developed based on [12]. The results are summarized in Table 2. The reduction ratios of launch switching activity (w.r.t.; measured by the WSA metric [13]) for the original test sets are shown under ‘‘XID+Preferred’’, ‘‘XID+JP’’, and ‘‘CTX’’, respectively. It should be noted that none of the three method increases test vector counts.

Table 2 shows that the CTX scheme is more effective than the previous schemes when compared to conventional test relaxation [12] and X-filling [13], [15] results. It also shows that CTX is especially effective for low-power devices, in which the clock-gating mechanism is frequently used. Particularly notable is the reduction ratio for ‘‘cir2’’, which decreased launch switching activity by almost 60%. Moreover, while WSA metric does not represent IR-drop value exactly, given the 60% of WSA reduction ratio, we can expect a significant reduction in IR-drop.

Table 3 shows the amount of CPU time required after a given initial test set has been generated. While CTX require a greater computational cost than the other methods, this increase seems acceptable.

### Discussions

(1) CTX is *non-intrusive* in reducing yield loss risk for at-speed scan testing, in that CTX causes no test data inflation, fault coverage loss, circuit/clocking modification, or circuit performance degradation. This makes CTX a preferred part of any power-safe test generation flow.

(2) CTX is *applicable to test compaction and test compression* where the number of X-bits in a test cube is limited. CTX makes up for such X-bit shortages by making

full use of clock-gating in a sophisticated manner (in that the original test vector count does not change).

## 5. Conclusions

This paper proposed a novel two-stage scheme, namely *CTX* (*Clock-Gating-Based Test Relaxation and X-Filling*) for effectively reducing launch switching activity that may cause yield loss in at-speed scan testing. The basic idea is to use clock-gating to disable as many FFs that do not contribute to fault detection as possible. *CTX* is the first of technique its kind that makes full use of clock-gating in test relaxation and *X*-filling. *CTX* reduces yield loss risk without any impact on test size, fault coverage, ATPG, circuit and clock design, or functional performance. Furthermore, *CTX* is applicable to any test compression schemes where *X*-bits are limited.

Future work includes: (1) conducting more evaluation experiments on more industrial circuits with gated clocks, (2) evaluating *CTX* in a test compression flow, and (3) conducting IR-drop and timing analysis to further demonstrate the effectiveness of the *CTX* scheme.

## Acknowledgments

The authors would like to thank STARC for providing industrial circuits.

## References

- [1] L.-T. Wang, C.-W. Wu, and X. Wen ed., *VLSI Test Principles and Architectures: Design for Testability*, Morgan Kaufmann, 2006.
- [2] J. Saxena, K.M. Butler, V.B. Jayaram, S. Kundu, N.V. Arvind, P. Sreepakash and M. Hachinger, "A case study of IR-drop in structured at-speed testing," Proc. Int'l Test Conf., pp.1098–1104, 2003.
- [3] P. Girard, "Survey of low-power testing of VLSI circuits," IEEE Des. Test Comput., vol.19, no.3, pp.82–92, May/June 2002.
- [4] N. Nicolici and B. Al Hashimi, *Power-Constrained Testing of VLSI Circuits*, Kluwer Academic Publishers, 2003.
- [5] J. Wang, D.M.H. Walker, A. Majhi, B. Kruseman, G. Grontboud, L.E. Villagra, P. Wiel, and S. Eichenberger, "Power supply noise in delay testing," Proc. Int'l Test Conf., Paper 17.3, 2006.
- [6] S. Ravi, "Power-aware test: Challenges and solutions," Proc. Int'l Test Conf., Lecture 2.2, 2007.
- [7] N. Ahmed, M. Tehranipoor, and V. Jayaram, "Transition delay fault test pattern generation considering supply voltage noise in a SOC design," Proc. Design Automation Conf., pp.533–538, 2007.
- [8] V.R. Devanathan, C.P. Ravikumar, and V. Kamakoti, "A stochastic pattern generation and optimization framework for variation-tolerant, power-safe scan test," Proc. Intl. Test Conf., Paper 13.1, 2007.
- [9] S. Wang and W. Wei, "A technique to reduce peak current and average power dissipation in scan designs by limited capture," Proc. Asian S. Pacific Design Automation Conf., pp.810–816, 2007.
- [10] X. Wen, S. Kajihara, K. Miyase, T. Suzuki, K.K. Saluja, L.-T. Wang, K.S. Abdel-Hafez, and K. Kinoshita, "A new ATPG method for efficient capture power reduction during scan testing," Proc. VLSI Test Symp., pp.58–63, 2006.
- [11] A.H. El-Maleh and K. Al-Utaibi, "An efficient test relaxation technique for synchronous sequential circuits," IEEE Trans. Comput. Aided Des., vol.23, no.6, pp.933–940, June 2004.
- [12] K. Miyase and S. Kajihara, "XID: Don't care identification of test patterns for combinational circuits," IEEE Trans. Comput. Aided Des., vol.23, no.2, pp.321–326, Feb. 2004.
- [13] S. Remersaro, X. Lin, Z. Zhang, S.M. Reddy, I. Pomeranz, and J. Rajski, "Preferred fill: A scalable method to reduce capture power for scan based designs," Proc. Int'l Test Conf., Paper 32.2, 2006.
- [14] X. Wen, K. Miyase, T. Suzuki, S. Kajihara, Y. Ohsumi, and K.K. Saluja, "Critical-path-aware X-filling for effective IR-drop reduction in at-speed scan testing," Proc. Design Automation Conf., pp.527–532, 2007.
- [15] X. Wen, K. Miyase, S. Kajihara, T. Suzuki, Y. Yamato, P. Girard, Y. Ohsumi, and L.-T. Wang, "A novel scheme to reduce power supply noise for high-quality at-speed scan testing," Proc. Int'l Test Conf., Paper 25.1, 2007.



**Kohei Miyase** received Ph.D. degrees in Computer Science and Systems Engineering from Kyushu Institute of Technology, Japan 2005. In 2007, he joined the Department of Computer Science and Electronics of Kyushu Institute of Technology, Japan, where he is an Assistant Professor currently. His research interests include test compression, design for testability, low power test, and fault diagnosis. He is a member of the IEEE.



**Xiaoqing Wen** received the B.E. degree from Tsinghua University, Beijing China, in 1986, the M.E. degree from Hiroshima University, Hiroshima, Japan, in 1990, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1993. From 1993 to 1997, he was a Lecturer at Akita University. He was a Visiting Researcher at University of Wisconsin, Madison, U.S.A., from Oct. 1995 to March 1996. He joined SynTest Technologies, Inc., U.S.A., in 1998, and served as its CTO until 2003. In 2004,

he joined the Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor. His research interests include VLSI test, diagnosis, and testable design. He is a senior member of the IEEE, and a member of the REAJ.



**Hiroshi Furukawa** received the B.E. from Kumamoto University, Japan, in 1992, He joined NEC Micro Systems in 1992. He is studying towards his Ph.D. degree in the Creation Informatics Program at Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Japan. His research interests include VLSI test.



**Yuta Yamato** received his B.E. and M.E. degrees in Computer Sciences and Electronics from Kyushu Institute of Technology, Japan, in 2005 and 2007 respectively. Currently, he is studying towards his Ph.D. degree in the Creation Informatics Program at Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Japan. His research interests include VLSI test and diagnosis.





**Seiji Kajihara** received the B.S. and M.S. degrees from Hiroshima University, Japan, and the Ph.D. degree from Osaka University, Japan, in 1987, 1989, and 1992, respectively. From 1992 to 1995, he worked with the Department of Applied Physics, Osaka University, as an Assistant Professor. In 1996, he joined the Department of Computer Science and Electronics of Kyushu Institute of Technology, Japan, where he is a Professor currently. His research interest

includes test generation, delay testing, and design for testability. He received the Young Engineer Award from IEICE in 1997, the Yamashita SIG Research Award from IPSJ in 2002, and the Best Paper Award from IEICE in 2005. Dr. Kajihara is a member of the IEEE and the IPSJ. He serves on the editorial board of the *Journal of Electronic Testing: Theory and Applications*.



**Patrick Girard** received a M.S. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research), and works in the Microelectronics Department of the LIRMM (Laboratory of Informatics, Robotics and Microelectronics of Montpellier – France). Patrick Girard is the Vice-Chair of the European Test Technology

Technical Council (ETTC) of the IEEE Computer Society. He is currently the Editor-in-Chief of the *ASP Journal of Low Power Electronics (JOLPE)* and an Associate Editor of the *IEEE Transactions on VLSI Systems* and the *Journal of Electronic Testing – Theory and Applications (JETTA – Springer)*. From 2005 to 2009, he was an Associate Editor of the *IEEE Transactions on Computers*. He has served as technical program committee member of the *ACM/IEEE Design Automation Conference (DAC)*, *ACM/IEEE Design Automation and Test in Europe (DATE)*, *IEEE International Test Conference (ITC)*, *IEEE International Conference on Computer Design (ICCD)*, *IEEE International Conference on Design & Test of Integrated Systems (DTIS)*, *IFIP International Conference on VLSI-SOC*, *IEEE VLSI Test Symposium (VTS)*, *IEEE European Test Symposium (ETS)*, *IEEE International On-Line Testing Symposium (IOLTS)*, *IEEE Asian Test Symposium (ATS)*, *ACM/IEEE International Symposium on Low Power Electronic Design (ISLPED)*, *IEEE International Symposium on Electronic Design, Test & Applications (DELTA)* and *IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*. He has served as Test Track Chair for *DAC 2007*, *DATE 2007*, *DATE 2008*, *ICCD 2008* and *DATE 2009*. He has also served as Program Chair for *DELTA 2006*, *DTIS 2006*, *DDECS 2007* and *ETS 2008*. Patrick Girard has been involved in several European research projects (*ESPRIT III ATSEC*, *EUREKA MEDEA*, *MEDEA+ ASSOCIATE*, *IST MARLOW*, *MEDEA+ NanoTEST*, *CATRENE TOETS*) and has managed industrial research contracts with major companies like *Infineon Technologies*, *Atmel*, *STMicroelectronics*, etc. His research interests include the various aspects of digital testing and memory testing, with special emphasis on *DFT*, *BIST*, diagnosis, delay testing, and power-aware testing. He has supervised 20 PhD dissertations and has published 6 books or book chapters, 30 journal papers, and more than 110 conference and symposium papers on these fields. He received the Best Paper Award at *ETS 2004* and at *DDECS 2005*.



**Laung-Terng (L.-T.) Wang** is chairman and chief executive officer (CEO) of SynTest Technologies (Sunnyvale, CA). He received his BSEE and MSEE degrees from National Taiwan University in 1975 and 1977, respectively, and his MSEE and EE Ph.D. degrees from Stanford University in 1982 and 1987, respectively. He founded SynTest Technologies (Sunnyvale, CA), a design-for-test (DFT) company, in January 1990. He currently holds 20 U.S. Patents and 15 European Patents. He has

also co-authored and co-edited three internationally used *DFT/EDA* textbooks — *VLSI Test Principles and Architectures* (2006), *System-on-Chip Test Architectures* (2007), and *Electronic Design Automation* (2009). A member of Sigma Xi, Dr. Wang received a 2007 Meritorious Service Award from the IEEE Computer Society and is a co-recipient of the 2009 IEICE Information and Systems Society Excellent Paper Award for an excellent series of papers that appeared in *IEICE Transactions on Information and Systems* during a period of five years. He is a Fellow of the IEEE and an IEEE Computer Society Golden Core Member.



**Mohammad Tehranipoor** (S'02-M'04-SM'07) received the B.Sc. degree from Amirkabir University of Technology (Tehran Polytechnic University), the M.Sc. degree from the University of Tehran, and the Ph.D. degree the University of Texas at Dallas in 1997, 2000, and 2004, respectively all in electrical engineering. He is currently an Assistant Professor of Electrical and Computer Engineering at the University of Connecticut. His current research projects include: computer-aided design and test for

CMOS VLSI designs, design-for-testability, at-speed test, secure design and IC trust. Dr. Tehranipoor has published over 85 journal articles and refereed conference papers in the area of VLSI design, test, and hardware security and trust. He has published two books entitled “*Nanometer Technology Designs – High-Quality Delay Tests*” and “*Emerging Nanotechnologies – Test, Defect Tolerance and Reliability*” in addition to three book chapters. He is a recipient of a *best paper award* at the 2005 VLSI Test Symposium (VTS), *best paper award* at the 2008 North Atlantic Test Workshop (NATW), *best paper award* at NATW'2009, *honorable mention for best paper award* at NATW'2008, *best paper candidate* at the 2006 Design Automation Conference (DAC), *best paper candidate* at the 2005 Texas Instrument Symposium on Test, *best panel award* at VTS'2006, and *top ten paper recognition* at the 2005 International Test Conference (ITC). Dr. Tehranipoor is also a recipient of the 2008 *IEEE Computer Society Meritorious Service Award* and the 2009 *NSF CAREER award*. He serves on the program committee of several conferences and workshops. Dr. Tehranipoor served as the guest editor for *Journal of Electronic Testing: Theory and Applications (JETTA)* on “Test and Defect Tolerance for Nanoscale Devices” and guest editor for *IEEE Design and Test of Computers* on “IR-drop and Power Supply Noise Effects on Very Deep-submicron Designs”. He served as *Program Chair* of the 2007 IEEE Defect-Based Testing (DBT) workshop, *Program Chair* of the 2008 IEEE Defect and Data Driven Testing (D3T), *Co-program Chair* of the 2008 International Defect and Fault Tolerance in VLSI Systems (DFT). He initiated a new workshop called IEEE International Workshop on Hardware-Oriented Security and Trust (HOST) and served as *HOST-2008 General Chair and Chair of Steering Committee*. He is currently serving as the *General Chair* for *D3T-2009*, *DFT-2009*, and *HOST-2009*. He is also currently serving as an Associate Editor for *JETTA* and Editor for *TTTC Newsletter*. Dr. Tehranipoor is a term member of Graduate Faculty of ECE Department at Duke University. Dr. Tehranipoor is a Senior Member of the IEEE and Member of ACM and ACM SIGDA.