Product On-Chip Process Compensation for Low Power and Yield Enhancement

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Abstract. This paper aims at introducing a reliable on-chip process compensation flow for industrial integrated systems. Among the integrated process compensation techniques, the main one aims at reducing the supply voltage of fast circuits in order to reduce their power consumption while maintaining the specified operating frequency. The proposed design flow includes efficient methodologies to gather/sort on-chip process data but also post-silicon tuning strategies and validation methods at both design and test steps. Concrete results are introduced in this paper to demonstrate the added value of such a methodology. More precisely, it is shown that its application leads to an overall energy reduction ranging from 10% to 20% on fast chips.

Keywords: Variability, voltage scaling, sensors, process compensation.

1 Introduction

Energy consumption, not only the one of integrated systems, has become one of the most widely discussed topics in recent years because of the global warming effects. Since semiconductor electronic devices are increasingly used, designing products with the environmental impacts in mind through their entire life cycle becomes a necessity and technology development is now not only driven by a desire to improve circuit density and speed.

More precisely, the management of the power consumption of IC and its associated variability while warranting their functionality is now one of the major challenges in integrated system design.

Within this context, the process induced variability, which is a matter of a few atoms or less, appears as an important additional issue that cannot be neglected.

Indeed, leakage power varies now exponentially with key process parameters such as gate length, oxide thickness, threshold voltage[1], in addition to the variability related to local transistor environment and wires including circuit layout, pattern dependency and density[2].

J. Monteiro and R. van Leuken (Eds.): PATMOS 2009, LNCS 5953, pp. 247–255, 2010.

Up to now, this increasing variability has led designers to introduce additional design margins which increases pessimism and thus reduces both timing and power performances. To overcome the variability issue, a close cooperation between system design and technology development teams is required for the future technology nodes as technological solutions can no longer compensate for all the effects of scaling.

As a result, good process control techniques combined with on-chip performance monitoring and compensation techniques appears as an interesting solution for reducing both power and spread power consumption, maintaining a reasonable margins and maximizing the number of chips that will meet power and delay constraints.

If several Process Voltage Temperature (PVT) sensors have been proposed in the literature for variability compensation [3, 4 ,5, 6], no work related to the design and test flow of circuits integrating process compensation technique has been published up to now and to the best of our knowledge. This paper addresses this point.

The remainder of the paper is organized as follows. Section II describes some on-chip sensors used to gather and sort on-chip process data. Section III gives an overall view of the proposed process compensation flow and associated techniques related to design, manufacturing, test, speed binning, fuse coding, and the post-silicon tuning. Concrete results related to energy savings obtained using process compensation are given before to draw a conclusion in section V.

2 On Chip Performance Monitors

To allow on-chip performance monitoring, a set of specific oscillators were designed to monitor individually the performances of NMOS and PMOS in terms of speed and leakage current.

Each sensor is made of three specific oscillating structures called respectively ‘Speedometer NMOS’, ‘Speedometer PMOS’ and ‘Leakometer’. Note these structures were designed to be as representative as possible of real circuits especially in terms of density and metal layers. The signals delivered by these structures are periodic square signals and it is the period of these signals that provides insights on the quality of the design in terms of speed and leakage.

These monitors were developed and validated on different successive technology nodes for all available process options to address a large product portfolio needs. The validation of these sensors was done through a large silicon campaign characterization to prove their efficiency in tracking process skews including process corners deviations but also within-wafer and within die variations.

As an illustration of this silicon validation campaign, figure 1 gives the measured frequencies at the output of the ‘Speedometer NMOS’ and ‘Speedometer PMOS’. These measures represent five corner lots intentionally processed to obtain as N/P transistors SLOW, TYPICAL or FAST.

As shown and expected, the measured frequencies for the corner lots FAST/FAST, TYPICAL/TYPICAL, SLOW/SLOW nearly pile up on the first bisecting line validating the sensors. Moreover, for cross corner lots (FAST/SLOW and SLOW/FAST) the measured obtained respectively below and above the bisecting line. This result was expected from specifications and simulation results.

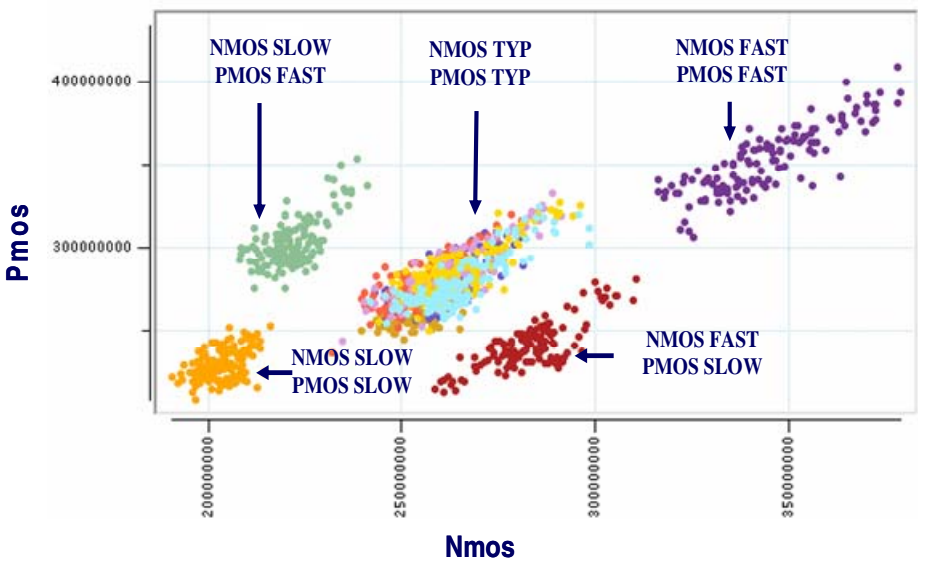

Fig. 1. Speedometer NMOS frequency vs Speedometer PMOS frequency for different corner lots (normalized).

3 Efficiency of Voltage Scaling as a Static Process Compensation Technique

If post silicon tuning techniques are now recognized as mandatory for the design of low power and/or high speed circuits in advanced technologies, their use requires the definition and the qualification of safe post silicon design and test flows. These flows, to be efficient, must target the best trade-off between delay, dynamic/static power consumption, reliability, tuning flexibility and design overhead in addition to exhaustive validation methods at each step of the flow.

In this section, we present the benefits and robustness of the developed process compensation flow. As illustrated in figure 2, this flow requires three additional steps compared to a standard design flow. In a first step, on-chip ring oscillators (sensors) and their control circuitry are integrated to the circuit at the design stage. In a second step, on-chip sensor's data are read at test level to enable part grading and on-chip fuse code is used to identify fast and standard parts. In a third step, post silicon tuning techniques such as static voltage scaling are performed to compensate and optimize fast parts speed and power performances.

This flow, shown figure 2, was established with close cooperation between system design teams and technology development teams.

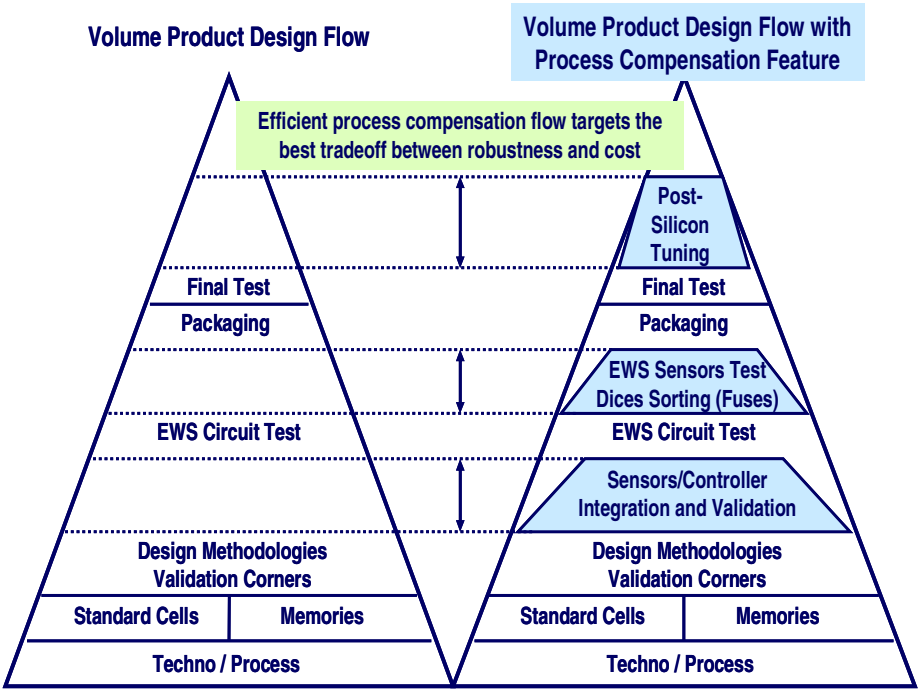

Fig. 2. Standard design and test flow vs advanced design and test flow with process compensation features

-a- Design approach

The first additional step resumes to the integration of the on-chip ring oscillators (sensors). To be compliant with a large product portfolio, the standard interface JTAG (Joint Test Action Group) is adopted to access the on-chip sensors data. This choice eases both the integration into circuits and the test in a production environment (see figure 3).

-b- Validation approach

As any product, integrated circuits designed accordingly to this methodology have to be validated. At design stage, it must be proved that a circuit may maintain its performances under reduced supply conditions.

To ensure the correct functionality of the design, exhaustive timing verifications are performed using multi-corners Timing Analysis (TA) including additional timing corners wrt to usual TA. This of course implies the characterization of all standard cell libraries and their post silicon characterization and validation.

-c- Test approach

To obtain accurate process data from the sensor and therefore choose the right fuse coding, the measurements of sensor outputs through the JTAG interface must be done at EWS test step (Electrical Wafer Sorting) in a controlled environment (see figure 3). This environment control must warrant a constant room temperature and a nominal

supply voltage for the Device Under Test (DUT). Note that during this sensor data collecting phase, the reproducibility and repeatability of the measurements was checked.

Based on the results of measurement, each sensor output is compared against the corresponding reference value. If Speedometer NMOS (PMOS) output is above the corresponding reference value the NMOS (PMOS) transistors of the DUT are classified as FAST and inversely.

Manufactured fast parts are fused with a code to indicate to the final system that they can run at a reduced supply voltage, while standard parts operate at the nominal supply voltage. This policy results in an overall worst case power consumption reduction as illustrated figure 4.

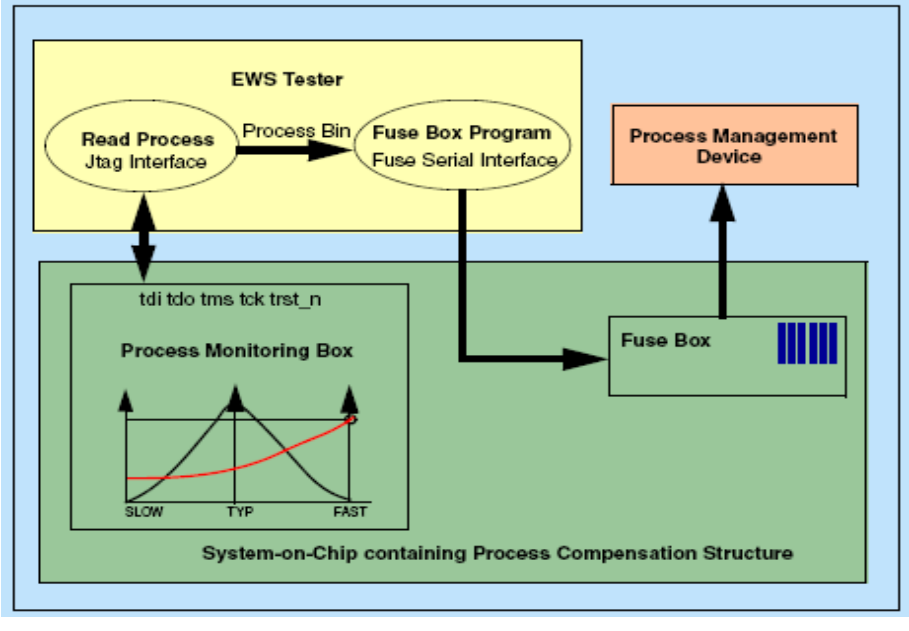

Fig. 3. Overview of the additional EWS test step to be applied to process compensated systems

-d- Process Compensation Implementation

According to the ITRS (International Technology Roadmap for Semiconductors), three types of products are identified: High Performance (HP), Low Operating Power (LOP), and Low Standby Power (LSTP) devices integrating different circuit level power optimization techniques such as multi-Vt [1], multi-Tox [1] and multi-Vdd [1]. This roadmap also suggests some additional power optimization techniques to be applied at architecture, and operating systems levels but also software level.

Among these techniques, voltage scaling technique was chosen since it reduces simultaneously both static and dynamic power consumption and this during all the product lifecycle. If this power optimization technique may be applied at different granularity, it was decided to apply it at the chip level. Several reasons explain this policy choice. First, the necessity of a generic- process compensation methodology which avoids the integration of level shifters and isolation cells, and results in a

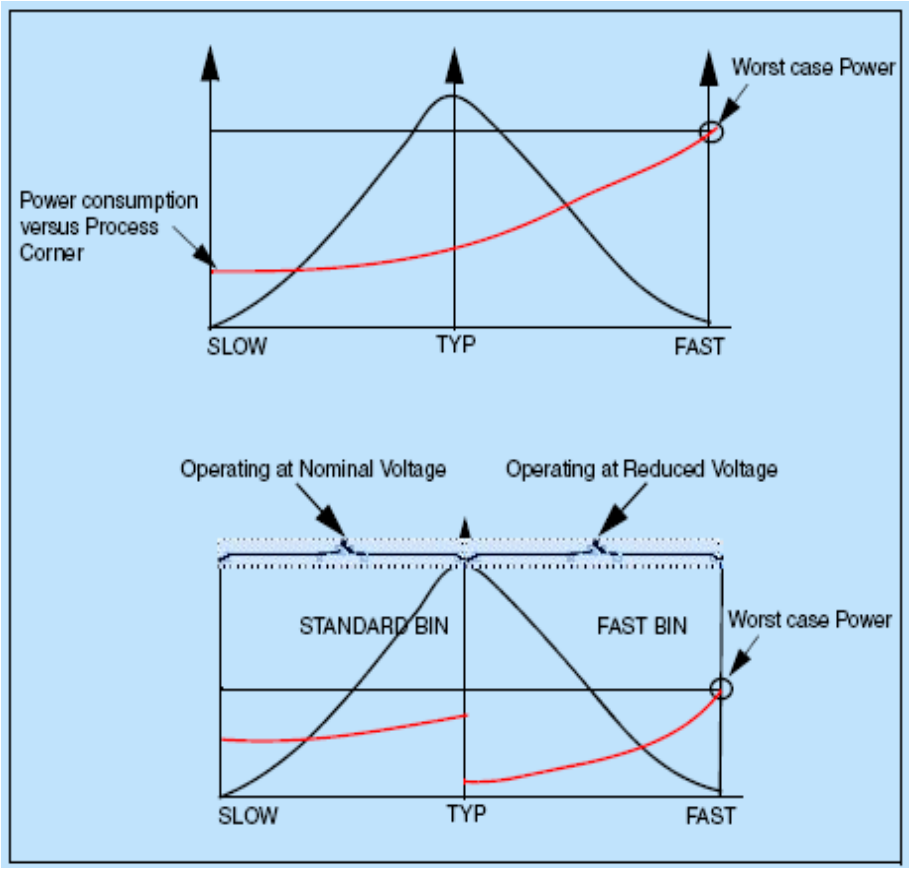

Fig. 4. Circuit power consumption versus process corner distribution (SLOW, TYPICAL and SLOW) before and after process compensation implementation

minimal area overhead. Second, it eases the design and offers a reasonable trade-off between design time, robustness and power savings.

Indeed, figure 4 shows the decrease of the worst case power consumption when the post-silicon process compensation is implemented on fast parts.

-e- Experimental results

This process compensation flow has been applied to several products. Within this section we present some concrete results related to a circuit designed in a 65 nm CMOSLPGP mix technology. This 1GHz Digital Channel Multiplexer for Satellite Outdoor Unit has a silicon area of 12.75 mm² and a digital total power of 950mW for standard parts at 1V supply voltage as described in reference [7].

The static voltage scaling policy was to supply slow dices with a nominal digital supply voltage of 1 V and to supply fast and leaky circuits with a voltage value reduced by 80mV.

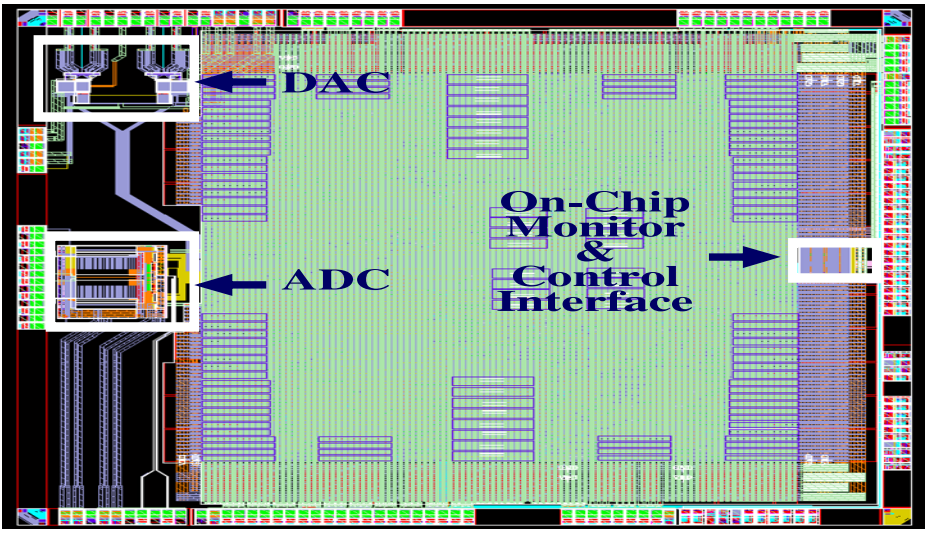

Fig. 5. 1GHz Digital Channel Multiplexer for Satellite Outdoor Unit in a 65 nm CMOSLPGP mix technology with embedded on-chip monitors (sensors)

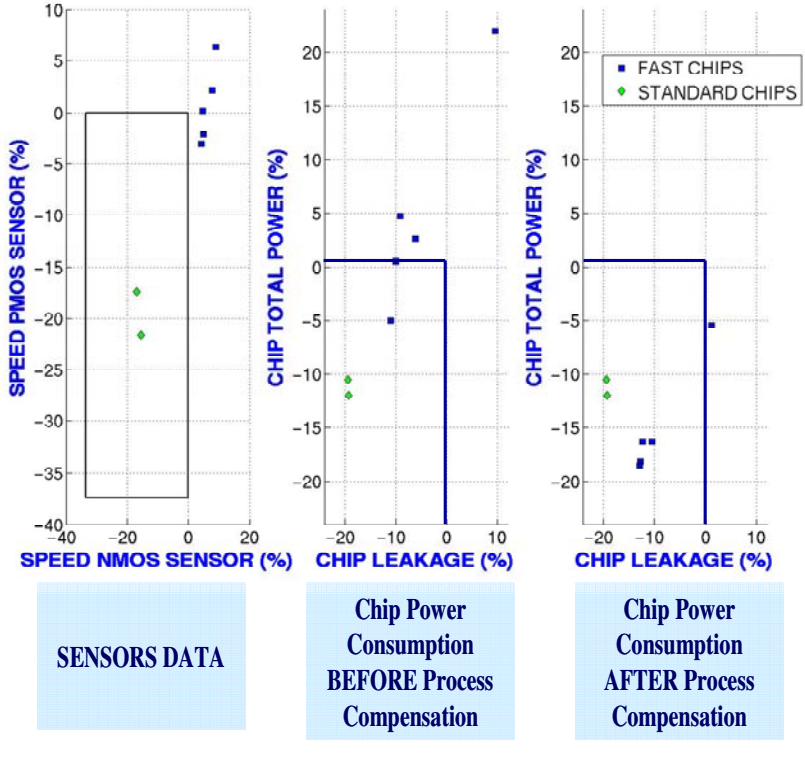

Fig. 6. Normalized Circuit performances before and after process compensation

As presented on figure 6, without applying any static voltage scaling policy, fast circuits may work at a maximal frequency up to 8% greater than the nominal maximum frequency. This is mainly explained by the quality of NMOS and PMOS devices. However their static power consumption may be 23% more important than the one of standard (nominal) chips.

As expected, when the proposed process compensation flow is implemented, the total power consumption reduction ranges between 10% and 20% and the circuit still operates correctly while maintaining the nominal operating frequency.

The obtained results demonstrate that the introduced process compensation flow reduces the total power of fast chips without compromising performances and may also avoid the use of costly packages to dissipate the power consumption of fast parts.

These results also demonstrate that the on-chip sensors and their associated control interface give accurate results at the cost of a slight area overhead of 0.04mm² and a moderate design and test time increase. However, this test-time increase must be compared to the 20% energy savings on fast circuits, energy savings that remains over the full lifecycle of the product.

4 Discussions and Perspectives

In addition to a significant power reduction on fast circuits, the integration of on-chip sensors may enhance the production quality. Indeed, the integration of sensors allows

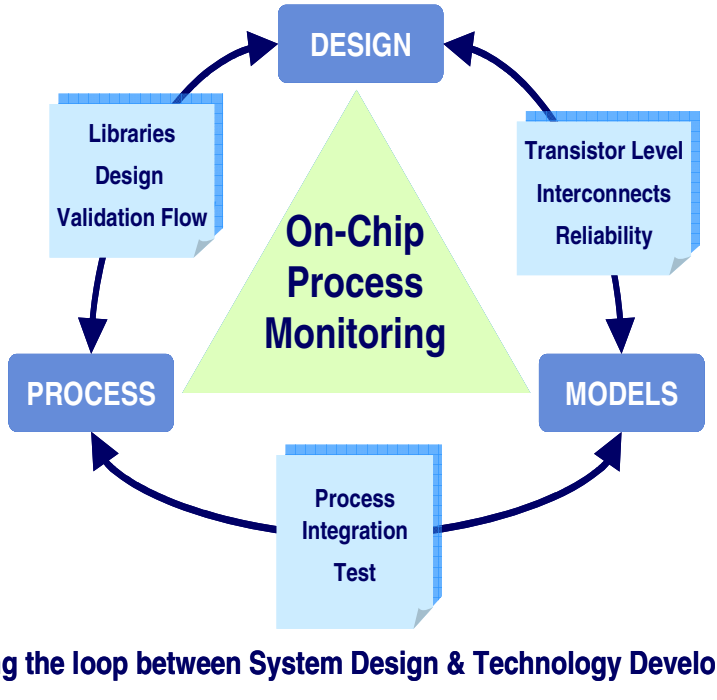

Fig. 7. Closing the loop between the design, test and process teams involved in the production of volume circuits

giving chips a unique ID with process centering data. As a result, it allows tracking on-chip process variability over fab-to-fab, wafer-to-wafer and die to die, and eases the implementation of diagnosis methodologies and yield learning [8].

In a second phase, the sensors may be used to check the process maturity evolution during the ramp up of a technology. This last point resumes in closing the loop between the design, test and process teams involved in the volume production circuits as illustrated figure 7.

Finally, a last advantage offered by the integration of on-chip sensors is the ability of monitoring hot spot zones identified during simulation at design level. Among the hot spot zones that can be monitored one can found circuit areas subjected to dynamic IR drops, temperature variations due to localized high activity rate.

5 Conclusion

The main contribution of this paper is to introduce a simple and robust process compensation flow for high volume circuit production. Some concrete results related to the power savings obtained by the application of this flow on a 12.75 mm² chip have been introduced. This savings may reach 20% of the total power consumption without impacting circuit functionality and operating frequency.

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