Impact of Inductance and Routing Orientation on Timing Performances of Coupled Interconnect Lines

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Abstract - As the interconnect lines play an increasingly dominant role in determining circuit performance, the dynamic delay variation due to the switching activity of neighboring lines has to be accurately characterized. The goal of this work is to simulate the effect of inductance and routing orientation and then to investigate their effects on timing performances by considering three configurations of three parallel coupled interconnects. For a Deep-Sub-Micron process, we show that when analyzing VLSI circuits, if standard distributed RC models are used, and inductive effects and routing orientation are ignored, large errors can occur in the prediction and evaluation of the circuit behaviour. Both affect greatly circuit performances.

Keywords: VLSI interconnect, routing orientation, crosstalk, signal integrity.

I. INTRODUCTION

In high speed circuits, signal integrity and timing are important issues for correct circuit operations. In VLSI circuits it is very common to have wires running adjacent to one another. In submicron designs, due to the greater proximity of adjacent wires on the same layer, increase in the heights of wires, relative to their widths, and increase in the switching speeds of signals, the parasitic coupling effects are significant. Coupling effects produce interference between signals, referred to as crosstalk noise, and many increase signal delays and decrease signal integrity. Signal integrity losses are further aggravated if multiple interconnect lines couple energy from or to each other. Crosstalk can have a significant impact on signal integrity and delay and even result in erroneous circuit operation. Crosstalk may cause undesirable effects including excessive overshoot, undershoot, glitch, additional signal delay and even in reduction in signal delay.

The appropriate interconnect model has changed several times over the past two decades due to aggressive technology scaling. Now, new and more accurate models are necessary. The increasing speed in SOC's (System On Chip) circuits and the increasing length of interconnect, can now both cause transmission line effects. Operating frequencies that have increased over the past decade, are expected to maintain the same rate of increase over the next decade approaching 10 GHz by the year 2012. On-chip inductance is becoming necessary to be included in the model, and its importance will increase as technologies downscale [1, 2]. [3] proposes a simple rule to define when inductance must be included in the modelling of a single line, based on the discrepancy between RC and RLC models. The effect of on-inductance on a single interconnect are classified in [4], into desirable effects, such as an improvement in the rise time of signals, a reduction of the power consumption and a reduction of the number of inserted repeaters, and undesirable effects. Two figures of merit have been proposed in [5] to determine the relative accuracy of an RC impedance to model on chip interconnect by using the asymptotic value of the attenuation constant. However, this assumption is not always verified in VLSI designs. Coupled interconnects are analyzed in [6], which introduces Elmore-like closed form solutions to analyze the behaviour of coupled lines such as propagation delay, rise time and overshoots. But none of these works illustrates the impact of routing orientation. A first study has been introduced in [7] by considering two configurations of parallel coupled lines, one with drivers on the same side, and the other with the drivers in opposite directions. The simple 2-coupled lines are not sufficient enough to verify the signal coupling effects. Thus, it is considered here 3-coupled lines. This case is representative of a beam of interconnections, where a central line is studied surrounded with two neighboring lines.

In this paper, to illustrate the importance of on-chip inductances and propagation orientation, different sets of simulation with interconnects based on up-to-date technologies are presented. This paper is organized as follows. In section 2, we present the simulation technique which was used to determine the interconnection timing characteristics.

Then, in the following section 3 and 4, corresponding to the best-case and the worst-case, we present the impact of inductance and routing orientation. In the last section, we summarize all the results to show the importance of taking into account the inductive and routing orientation influence to avoid logic errors and to predict accurate performances.

II. RLCG EQUIVALENT PARAMETERS CALCULATION AND SIMULATION MODEL FOR COUPLED INTERCONNECTS

For this study, we consider a typical geometry of an upper metal-layer consisting of three copper lines. The Cu interconnections are between two very dense metal layers, so that perfect metallic walls are taken into account on both sides of the wires. We used these dedicated ground planes as return paths. The principles of the analysis we have followed in order to obtain the numerical values of the R, L, C, G equivalent parameters from which a set of coupled transmission lines could be modeled, have been presented in [8]. Most existing noise models and avoidance techniques consider only capacitive coupling. However, at current operating frequencies, inductive crosstalk effects can be substantial and should be included for complete coupling noise analysis. Due to the slow decay of inductive coupling with increasing line spacing and the uncertainty of the current return loop in on-chip interconnect structures, the full L matrix must be extracted in contrast to capacitance extraction that only considers the nearest neighbors [9]. The effect due to inductance is changed by not only R, L, C values but also drivability [10], slew, power/ground lines for return loop [11], parallel line number, distance between lines… but in this paper to study the impact of routing orientation we keep the structure and geometrical parameters and simulation conditions constant. The corresponding electrical parameters extract from a 130 nm technology process are:

$R = 3$ ohms/µm, $C_{11} = C_{33} = 2.50$ fF/µm, $C_{22} = 1.80$ fF/µm, $C_{12} = C_{23} = 1.10$ fF/µm, $L_{11} = L_{22} = L_{33} = 5$ pH/µm,

$L_{12} = L_{23} = 4$ pH/µm, $L_{13} = 1.5$ pH/µm .

In this case, the conductance G is negligible (10^{-6} mS/ cm) and must not be incorporated in the model. These RLCG values are used to build the distributed π-RLC model (we use 40 cells) in the electrical simulations under HSPICE simulator. For each line, the driver is modelled as a linear resistor (i.e. Thevenin model) with an input slope of 15ps and loading capacitance of 5fF is added at the far-end of the line. The power supply is 1V.

In a three lines configuration, we distinguish two extreme cases:

- when the three lines have the same transition, it is the best-case
- when the neighboring lines have an opposite transition than that of the central line, it is the worst-case.

For each case, we can also differentiate three configuration of different orientation, to study the impact of routing orientation, as illustrated Fig. 1.

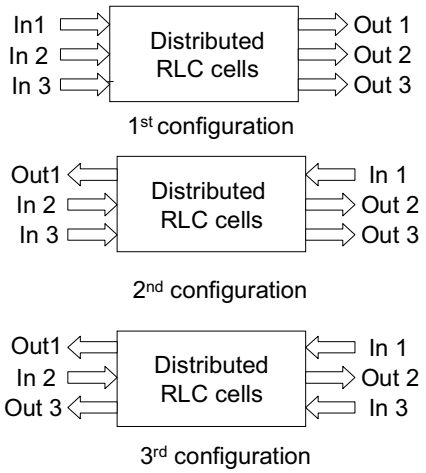


Fig. 1: Configurations to determine the propagation orientation influence.

III. THE THREE LINES HAVE THE SAME TRANSITION (BEST-CASE).

The best-case time delay occurs when the three-coupled lines are switching with the same polarity. For each configuration case and for any given length, we plot the inner interconnect delay in Fig. 2. The interconnections are first modeled by an RC distributed model. In this paper, we only consider the case where the three drivers switch at the same time.

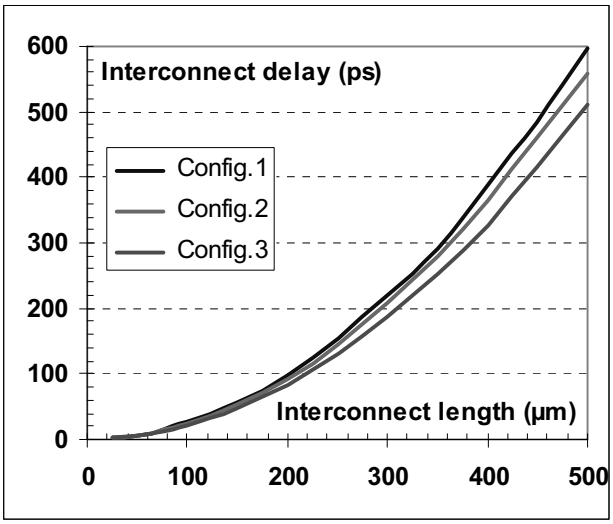


Fig. 2: Orientation impact on timing performances when the three lines have the same commutation

The variations of the delay of the middle line according to the length are weak for the various configurations. The average temporal gain is of the order of 6% for the configuration 2 with regard to the configuration 1 and of 15% for the configuration 3. In configuration 1, the three lines are held at the same potential; therefore, the capacitances between them never charge and do not affect the transient characteristics. For the two other configurations, the influence of the coupling on the waveform of the output signal of the

inner line since the beginning of the switching shows a deformation all the stronger as both neighboring line are concerned (Fig.3).

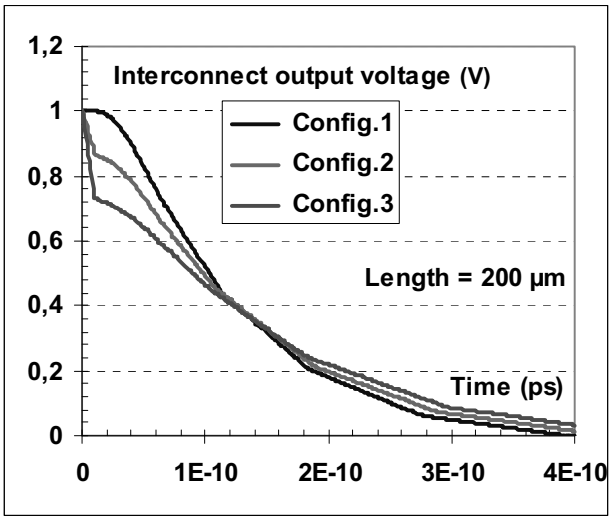
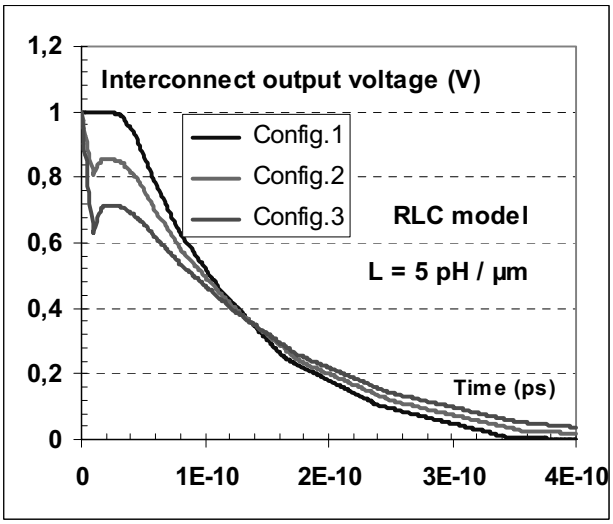


Fig. 3: Inner interconnect output voltage for different propagation configurations by using an RC model for the interconnects.

The moment of switching at Vcc/2 which determines the line delay is only little modified, as illustrated in Fig. 3, what has led the not consideration of this effect so far. However, at current operating frequencies, inductive crosstalk effects can be substantial and should be included for complete coupling noise analysis. The deformation of the output signal is strongly increased, even for values of rather weak inductance (L = 5 pH/µm), with important values of resistance (R = 3 ohms/µm), which gives a ratio Lω /R = 0.021. Fig 4 illustrates the output voltage disturbance for interconnects of 200µm for two different values of inductance.



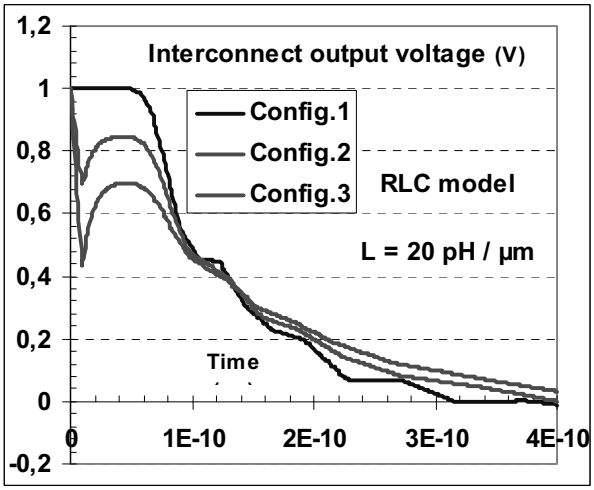


Fig. 4: Inner interconnect output voltage for different propagation configurations by using an RLC model for the interconnects for two different values of inductance.

We see clearly the influence of routing orientation on the output voltage which can lead to a problem with signal integrity with the possibility that if a line with a such negative pulse is connected to the clock input of a flip-flop, then this pulse can be interpreted as an additional clock pulse and cause the flip-flop to latch erroneous data.

IV. WORST-CASE TIME DELAY.

The worst-case time delay occurs when the inner line switches with an opposite polarity of the two outer lines. As with the preceding case, we first determine by electrical simulations the variation of interconnect delay versus the length, for the different configurations (Fig. 5).

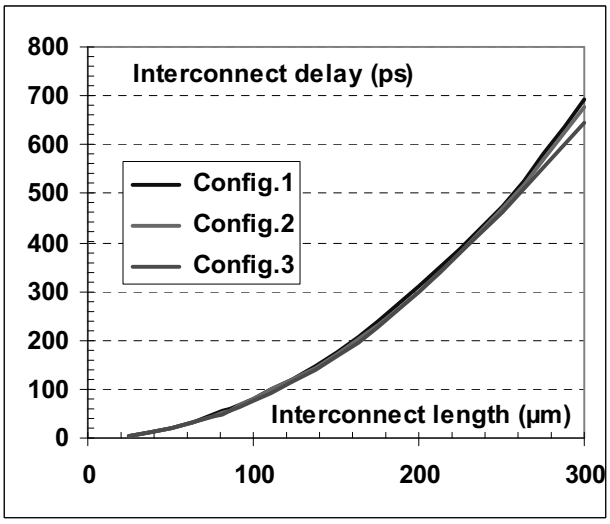


Fig. 5: Orientation impact on inner interconnect delay in worst-case

The interconnect delay varies just a little according to the configurations. The temporal variation of the configuration 2

with regard to the configuration 1 is only on average 2%, and 4% for the configuration 3. The interconnect delay of the central line is insensitive of the orientation of the neighboring lines, whatever the length, Fig. 6.

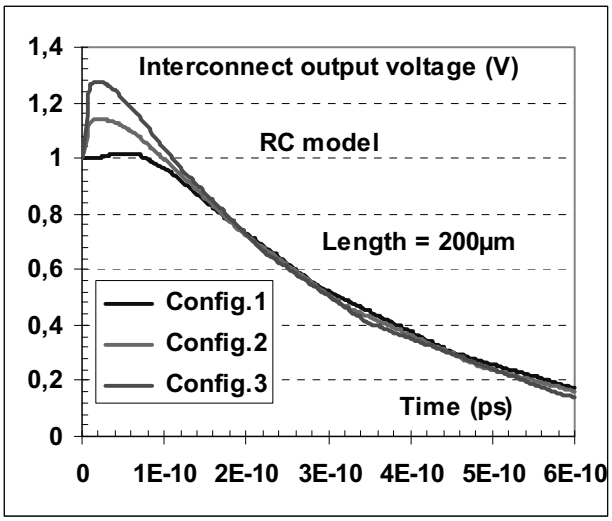


Fig. 6: Inner interconnect output voltage for different propagation configurations by using an RC model for the interconnects.

The waveform of the output signal shows an important overshoot, from the beginning of the switching, as soon as one of the neighboring lines have not the same propagation direction. The problem of voltage fluctuations has been identified in previous work approaching the problem [12] as a key factor for high performance integrated circuits. This overshoot increases with the inductance value, by keeping the same ratio of mutual inductance to self inductance, as shown Fig. 7.

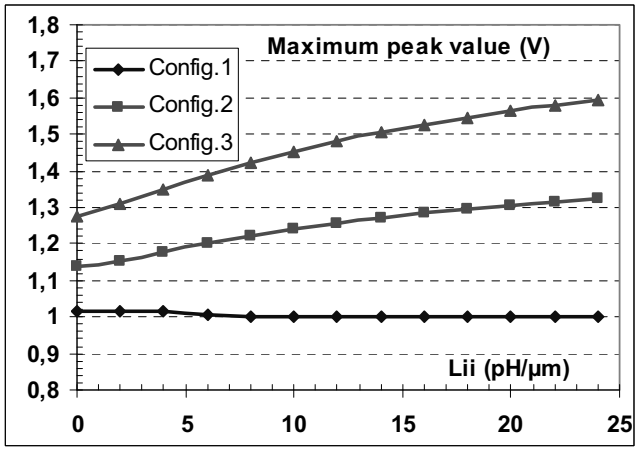


Fig. 7: Maximum peak value of inner interconnect output voltage for different propagation configurations versus self inductance value.

The overshoot delay is not very dependent on the configurations, and on the modeling RC or RLC. For the configuration 2, the overshoot delay is 98.7ps for RC model with an increase of 3.4% for L = 3 nH. For configuration 3, the delay is 110.4ps with a variation of 5.2%.

By maintaining the self inductance constant (Lii = 20pH/µm), we allocate a coefficient k to mutual inductance Lij to determine its influence. In the case of configuration 3, the figure 8 represents the variation of the output voltage for various values of mutual inductance. We see that this has an influence on the overshoot, more k is big more the peak of overshoot is important, while beyond the influence becomes negligible.

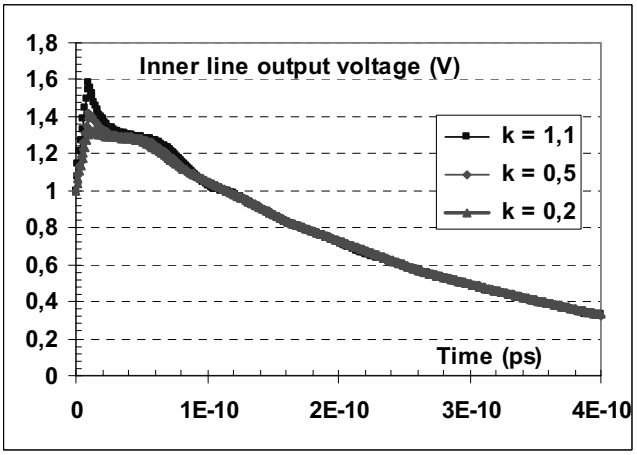


Fig. 8: Inner line output voltage for different mutual inductance values.

For different values of k, let us draw now on the fig.9 the variation of the maximum peak value of the overshoot for configuration 2 and 3 (the configuration 1 doest not lead to overshoot). We see clearly that the value of the peak of overshoot varies linearly with the values of mutual inductances, these one being stronger configuration 3 than configuration 2 , that is according to the number of neighbouring lines having a propagation direction opposite than that of the inner line.

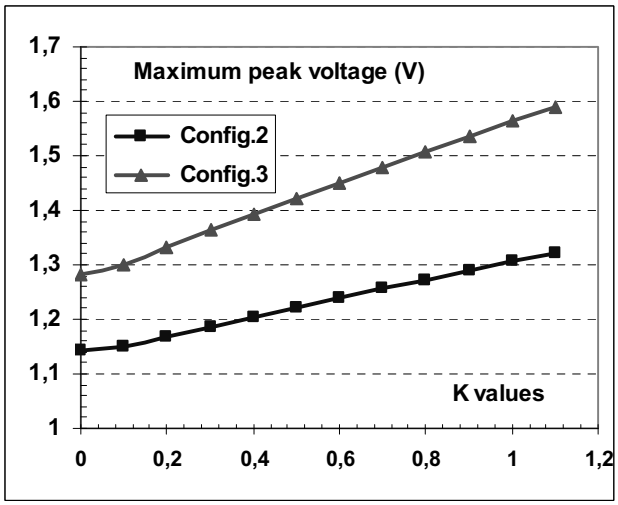


Fig. 9: Maximum peak value of the overshoot versus mutual inductance values.

V. CONCLUSION.

In this work, performances corresponding to the switching activity of the neighboring line were developed by considering three configurations of parallel coupled interconnects, with different propagation direction. We illustrate the growing significance of self and mutual inductances and routing direction by examining their effects on performance. It is demonstrated in this paper that when analyzing VLSI circuits, if standard distributed RC models are used while ignoring inductive effects, large errors can occur in the prediction and evaluation of the circuit behavior. We observed that the self and mutual inductances greatly affect deep sub-micron VLSI circuit performances. The study of these three cases illustrates the influence of the current' direction, giving a good understanding of the contribution of the self and mutual inductances. The line orientation becomes important, and can no longer be ignored, when the interconnections are modeled with an RLC model. This information must be integrated into extraction tools.

VI. REFERENCES

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