Setting Test Conditions for Improving SRAM Reliability

Renan Alves Fonseca, Luigi Dilillo, Alberto Bosio, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, Nabil Badereddine

Setting Test Conditions for Improving SRAM Reliability*

R. Alves Fonseca[1] L. Dilillo[1] A. Bosio[1]
P. Girard[1] S. Pravossoudovitch[1] A. Virazel[1]
[1]LIRMM Université de Montpellier II / CNRS
161, rue Ada – 34392 Montpellier Cedex 5, France
Email: <lastname>@lirmm.fr

N. Badereddine[2]
[2]Infineon Technologies France
2600, route des Crêtes – 06560 Sophia-Antipolis, France
Email: nabil.badareddine@infineon.com

***Abstract*— In the context of SRAM testing, we propose a methodology to define proper conditions under which SRAMs should be tested to improve their reliability. This methodology is especially suitable to deal with the impact of threshold voltage variability affecting SRAM core-cell transistors. By establishing an objective manner of comparing different test conditions, the proposed study shows how it is possible to detect SRAM core-cells with poor quality by applying a reduced set of test runs. The proposed methodology also allows determining the most appropriate DfT (Design–for-Test) technique for each peculiar SRAM design and technology.**

I. INTRODUCTION

Some studies analyze the impact of threshold voltage variability due to Random Dopant Fluctuation (RDF) on SRAM core-cells [1][2]. This causes slight degradations on transistor parameters which induce non-catastrophic faults in SRAM. As memory test is performed in a digital manner, a device at the border of error can pass the test and be declared as good device. This device has a high probability of failing when in-field. In order to avoid this situation, production tests are performed under aggressive environmental conditions (stress conditions). The principle is to detect also devices at border of error as failing devices by performing the same digital test under given stress conditions. Generally, stress conditions that can be controlled during test are temperature and power supply voltage (VDD). We consider also the variation of SRAM core-cell parameters (word line signal and bit line voltage) as stress conditions. Stress conditions must be carefully determined in order to do not deteriorate devices while maintaining acceptable fault coverage. The proposed methodology allows to find the optimal stress conditions that should be applied to test SRAM core-cells in order to maximize fault coverage.

II. METHODOLOGY DESCRIPTION

The methodology is based on electrical simulations to evaluate the impact of stress conditions on the SRAM core-cell functioning considering all possible variations of threshold voltages. We assume that threshold variations follow a Gaussian distribution. The reliability of the methodology also depends on this assumption. For each stress condition, two parameters are evaluated: *bad coverage* and *false coverage*. The former is the probability of a core-cell that is in the border of error to be detected as faulty during the test under stress conditions. The latter is the probability of a core-cell that works perfectly to be detected as faulty core-cell during the test under stress conditions. Thus, the optimal stress condition has high bad coverage and low false coverage. In order to compute bad coverage and false coverage of a stress condition, we extract performance metrics from electrical simulations that indicate the correctness of a core-cell considering different threshold voltage values. For each performance metric, acceptation limits classify the core-cell instance in *fail*, *bad* or *good*. We extract performance metrics both in normal conditions and in stress conditions. Bad coverage corresponds to the core-cells considered as bad in normal conditions, which are detected as fail under stress conditions. False coverage corresponds to the core-cells considered as good in normal conditions and that are identified as fail under stress conditions. The probability associated to each threshold voltage instance is used to compute the values of bad coverage and false coverage.

III. CASE STUDY

We used this methodology to analyze the effectiveness of five stress parameters for an industrial 65nm core-cell design. The stress parameters analyzed were the following ones: temperature, power supply voltage, word line pulse width, word line pulse voltage and bit line voltage. Each stress parameter was analyzed with different values, giving origin to different stress conditions. For this design, we detected that the word line pulse width parameter, which was proposed as a DfT technique in [3], is very effective. The combination of two test runs, with reduced and enlarged word line pulse width, was able to capture 100% of the bad core-cells, whereas the false coverage remains very low. We also noted that testing with a variation of 20% of VDD presents very high false coverage, which means that many good core-cells are identified as failing. Stress conditions based on temperature are also effective. They present high bad coverage (not 100%) for some temperatures and always present low false coverage.

* This work has been funded by the French government under the framework of the CATRENE CT302 "TOETS" European project

REFERENCES

[1] B. Cheng et al. ,"Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling", Solid-State Device Research Conf., pp. 258-261, 2006.
[2] R. Alves Fonseca et al, "Detecting NBTI Induced Failures in SRAM Core-Cells", IEEE VLSI Test Symposium, 2010.
[3] M. Sharifkhani et al., "Dynamic data stability in SRAM cells and its implications on data stability tests", IEEE Int. Workshop on Memory Technology, Design, and Testing, pp. 55-64, 2006.

978-1-4244-5833-2/10/$26.00 ©2010 IEEE