Adaptive LUT-Based System for In Situ ADC Auto-correction

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***Abstract* — Complex chips may today include several Analog-to-Digital and Digital-to-Analog Converters. These modules interface the external analog word with the internal digital computation circuitry such as processor cores. Correct internal digital computation consequently critically depends on high quality conversion even under stringent performance requirements. In order to meet these requirements, the new generations of high speed and resolution ADCs are calibrated after manufacturing. In this paper, we propose an original auto-correction scheme for ADC with an in situ calibration capability able to take into account the specific dynamic and the environment of the application and the aging effects. The scheme is validated through extensive simulations.**

I. INTRODUCTION

Nowadays, most part of the signal processing in areas like instrumentation, telecommunications, control and consumable electronics is carried out at the digital level.

The role of Analog-to-Digital Converters (ADCs) placed at the borders of the digital domain acquires a particular relevance, since the signal degradation introduced by these components cannot normally be recovered by subsequent processing. As the new generations of ADCs provide increasing speed and resolution, design requirements become more and more stringent, resulting in ever more difficulty to keep a high production yield. At the same time, the strong demand for integrated systems suitable for different standards or application field forces designer to develop wideband ADC. Finally, due to sensitivity of new technology to the environment (temperature, power supply value…), the design have to take into account all the possible user cases. This increases again the design constraints and leads designer to find new strategy for design.

An attractive solution to make both the design and the manufacturing of high performance devices easier consists in relaxing the design constraints and calibrating the devices after the devices manufacturing. The main parameter suitable for post correction is the Integral Non-Linearity (INL). Several techniques exist for off-line INL post correction [1-8]. Some of them are architecture-dependent and some others consider the ADC as a black box. These techniques can significantly increase the manufacturing yield but a strong limitation is the fact that the correction definition can be made only once for a given value of the ADC parameters. Moreover, no new calibration is possible even in case of a later change in the ADC parameters due to the environment or aging for example.

In this context, we propose a solution for "on-line" auto-calibration of ADC. In the literature some techniques can be found for digital on-line correction of ADC [9-11], but, they are dedicated to specific ADC architecture and they imply a large additional circuitry. For auto-correction purpose, it is necessary to evaluate on-chip the converter INL. And, one of the main issues here is to perform the INL estimation with a minimal silicon area overhead.

In the remainder of the paper, section 2 gives the fundamental principle of the widely used digital correction: the Look-Up-Table based correction. The state of the art of LUT-based techniques with its associated limitations is described. Section 3 gives details on the proposed solution allowing the on-chip auto-correction. In section 4, this adaptive LUT-based correction technique is validated through simulations with two different case studies. Finally, section 5 gives some concluding remarks

II. LUT-BASED CORRECTION

A. Principle

As explained in the introduction several techniques have been developed for ADC correction. The Look-Up-Table (LUT) based technique [3-7] is clearly one of the most efficient solutions because it works only in the digital domain after conversion of the signal. As presented in Figure 1, the fundamental principle consists in using the output code of the ADC to address a table (LUT) and substitutes this output code with the one in the table which includes a pre-computed correction of the output codes.

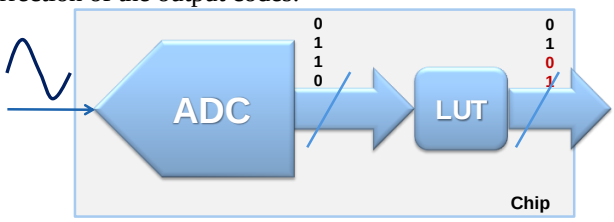

Figure 1. LUT-based post-correction of ADC

For this purpose, the LUT is usually filled during the production phase of the ADC after estimation of its non-linearity. The first step of the process is thus the estimation of the ADC INL.

B. Integral Non-Linearity

In this section, our objective is to define precisely what it is required for efficient LUT-based correction of ADCs. Indeed, INL consists of several independent components [12][13]. The first level model simply considers that INL of code *i* is split into two parameters as given by equation (1):

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$$INL(i) = LCF(i) + HCF(i) \quad (1)$$

Where LCF is the Low Code Frequency component and HLC is the High Code Frequency component of INL. The LCF shows the smooth variation of the INL versus codes and HCF emphasizes the sharp variations of INL. Generally, the LCF component can be modeled with a quite simple 3rd or 4th order polynomial; on the contrary HCF is strongly architecture dependent and cannot be described with a general analytical equation.

In fact, the previous model assumes that the INL is only static but in reality the INL can be affected by the input signal frequency [14][15]. To be more precise, INL doesn't depend on the frequency of the input signal but on the speed of signal variation at any point of the dynamic range of the ADC. To take into account this effect, the INL of the code *i* can be now expressed by equation (2):

$$INL(i,d) = SLCF(i) + HCF(i) + DLCF(i,d) \quad (2)$$

Where *d* is the slope: $d = \delta Vin/\delta t$ of the input signal at the input signal value corresponding to the code *i*. The LCF component is divided into a static part (SLCF) independent of the input signal variation and a dynamic part (DLCF) which corresponds to the variation of the INL according to the input signal slope. This last component is related to the frequency-dependent elements of the converters such as some parts of the amplifiers or comparators… Especially when no sampling-and-hold circuit is used for the converter. The HCF component is related to the imperfections of the ADC quantizer for which the output is fairly independent of the frequencies within the bandwidth.

Although the INL model presented in equation (2) is more precise it doesn't take into account the influence of the environment or the aging effect. We consequently consider now a complete INL model as described in equation (3):

$$INL(i,d,k) = SLCF(i,k) + HCF(i,k) + DLCF(i,d,k) \quad (3)$$

Where k emphasizes the external parameters such as temperature, drift due to aging, new application setup with a different sampling frequency, variation of the power supply… Generally, it is very difficult to estimate how all these "external" parameters might affect the INL nevertheless for high performance and large bandwidth ADC these parameters have to be considered.

The objective is not to perform a perfect measurement but to estimate the INL with the required accuracy for the correction process. In this context, an accurate estimation of the SLCF component is mandatory, but a precise estimation of the HCF component is not required even if this component remains essential for efficient correction in most cases. Finally, the DLCF component has to be taken into account because ADCs are generally defined for large bandwidth although each application uses a small part of this bandwidth.

C. Static versus dynamic correction

In the classical LUT-based correction techniques there are two different approaches: static or dynamic correction.

The static correction of an n-bit ADC uses an n-bit LUT of 2^n words. In the nominal operation of the ADC, the LUT is simply addressed by the current output code [3-5]; this implies a one-to-one correspondence between the ADC and the LUT giving a 2^n words LUT for an n-bit ADC. Some solutions exist to reduce the size of the LUT by correcting only a selected subset of the ADC codes. It is to note that static correction is efficient only if the input frequencies are close to the frequency used to fill the LUT [6] or if ADC INL are relatively insensitive to input frequency. Indeed, this static correction technique cannot correct the DLCF component of the INL.

The dynamic correction has been developed to overcome the limitations of the static one. In order to take into account the dynamic non-linearity (DLCF), it is necessary to consider not only the current output codes but also the previous ones. Consequently, additional computed data must be used to fill and address the LUT. Two different dynamic correction approaches have been proposed in the literature.

Firstly, the phase-plan technique [6] for which the input signal slope is used as an additional addressing data. The resulting table has two dimensions. The main issue is to be able to obtain a good estimation of the slope of the input signal.

The second dynamic correction method is called state-space correction [7-8]. The basic principle is to consider not just the current output code but instead the K last output codes that may be, in some way, an image of the input slope. The size of the correction table is related to the number K of considered samples: K previous samples plus the current sample gives a space of dimension K+1, and, consequently, a K+1 dimension table of 2^n words. The drawback of this method is the huge size of the table and the long time to address it using (K+1)*n bits for an n-bit ADC. Again, solutions have been proposed to reduce this size: the samples may be under-sampled and truncated [8] or certain bits can be masked after a learning phase. These different addressing techniques have been compared in [8] and it appears that the effectiveness of the correction decreases as the size of the LUT decreases to the point where the 'dynamic' correction is not better than the static one!

D. Summary

The static LUT-based correction is very efficient because it is possible to achieve a good correction with a quite small LUT. But, the static technique can not take into account the dynamic part of the INL. In the other hand, although dynamic correction is a promising technique, the global benefits can be discussed because of the complexity and required silicon area.

None of the static or dynamic techniques is able to estimate and correct the influence of the environment or aging expressed by equation (3).

III. In Situ LUT-based Auto-correction

A. Principle

In this context, we propose a new solution for auto-correction of ADCs using a small LUT but with the capability to take into account the dynamic effects as well as the environment and aging effects.

The fundamental idea is to propose an in situ LUT-based auto-correction scheme with the on-chip capability of computing and filling the LUT. By completing the LUT 'in situ', i.e. directly in the application, the corrected codes are computed according to the input signal dynamic, aging and environment

conditions. The proposed solution needs the on-chip generation of an input signal and INL estimation as illustrated figure 2.

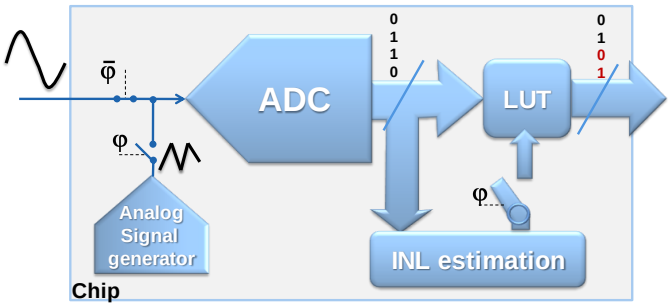

Figure 2. Adaptive LUT-based post-correction

During the calibration phase a control signal disconnects the primary input of the ADC and connects the integrated signal generator. The output INL is estimated and the computed corrected codes are stored into the LUT. After this calibration phase the ADC is disconnected from the embedded generator and the ADC works with its normal primary inputs, the output code being corrected on-line by the values stored into the LUT.

Classical calibration processes are usually made only once after manufacturing. This means that classical calibrations are made with no information on the targeted application and environment conditions. They are consequently performed for a wide band of frequencies, standard environment conditions, and independently from the aging effects. In our solution, because the calibration circuitry is integrated into the chip, the above calibration phase can be repeated at any time and at any location into a given application and for local and aging conditions.

Concerning the dynamic correction, it has been previously commented that the corresponding multi-dimensional LUTs are very large. In addition, the integration of the BIST circuitry for generation of the input signal, analysis of the output codes and generation of the correcting codes would represent a prohibitively large additional circuitry. For this reason, we propose to use a static correction but using for the calibration an input signal exactly in the frequency range of the targeted application. To be able to cover all possible applications, the generator must be flexible and able to generate an input signal in the corresponding frequency bandwidth. In other words, we assume that in the narrow frequency band of the targeted application, the INL is not very sensitive to small dynamic effects.

B. *Integrated module requirements*

As explained in the previous paragraph, the corrected codes are computed using an estimated INL curve. The computation simply consists in rounding down the measured INL curve after subtraction of the ideal INL. However, the INL estimation cannot be limited to the LCF part of the INL. The integrated module must be able to estimate sharp variations of the INL which correspond to an approximation of the Differential Non-Linearity (DNL).

The histogram-based method is a conventional test method mainly used to measure the Integral Non-Linearity (INL) of an ADC under test [16][17]. The process is made of three steps. The first step consists in building the experimental histogram that represents the number of times each ADC output code appears for a given input signal. Then, this experimental histogram is compared with an ideal histogram obtained in the case of both an ideal ADC and an ideal analog input. Note that for a linear input signal this ideal histogram is perfectly flat along ADC codes. Finally, the main ADC parameters (such as INL) are extracted from the comparison between the two histograms. Other techniques have been developed [18-23] for INL estimation; they are based on an INL modeling using polynomial or Fourier series expansion. In [22][23], the authors showed that only the technique based on Fourier series expansion can give local information on the INL. Unfortunately, the silicon integration of such Fourier based techniques is impossible because it needs the integration of both FFT computation and complex computations for INL extraction. As a consequence, the only possible solution for silicon integration is the histogram-based method.

Concerning the analog signal generator, it must be able to generate signal with different dynamic properties. As explained in paragraph *III.A* the generated signal has to be inside the required bandwidth of the targeted application. To be more precise, the slope of the generated signal must be in the range of the slope of the possible input signal in the considered application. In addition, we want all the codes to be corrected using this range of input signal slope. It is important to note that we don't need a large variety of input signal slopes, but we want all the codes to be corrected using the application range of slope. From this point of view, the classical sine wave signal is not satisfactory because it exhibits a large variety of slopes but not for all the codes. We consequently prefer to use a linear input signal with a slope selected in the range of the application slopes.

C. *Histogram-based Analyzer*

As explained in the previous section, the proposed correction scheme requires an on-chip estimation of the INL and the histogram-based method is the most efficient in terms of additional silicon. Many ADC BIST solutions have been proposed in the literature [24-33] mainly for test and characterization purpose including a solution patented by the authors [31]. We consequently propose to re-use these fundamental existing BIST concepts but of course they need to be modified and adapted to the purpose of auto-correction. In the remaining part of this section this BIST concepts are reminded and the required modifications are presented.

A straightforward implementation of the histogram test technique requires two memories of 2^n words to store the experimental and the ideal histogram, plus a DSP to compute the ADC parameters from the stored histograms. Of course, this would not be a viable solution in a BIST or BISR (Built-in-Self Repair) context. In order to reduce the required hardware resources, the digital analyzer [30] is implemented using the concept of on time decomposition. First, the classical parallel computation of the different ADC parameters is replaced by a sequential computation of each parameter. Second, the computation of every parameter is itself decomposed in a sequential process. This time-spread computation allows us to drastically reduce not only the

required memory hardware but also the digital analyzer able to perform the different computations. Indeed, due to this time decomposition concept, the digital analyzer allowing the computations on the stored histograms is only composed of two small modules.

The first module is the Detector Module (DM) is an n-bit register (for n-bit ADC) configurable in either a counter or a comparator and allows us to initialize the register. This module positions the code to be processed and compares it with the current ADC code.

The second bloc is the Exploitation Module (EM) is composed of a P-bit register together with a configuration logic controlled by two signals. Basically, the EM module can either operate as an up/down counter to realize addition and subtraction or provide the 2's complement of the value stored in the register to manage the sign of results. Note that obviously, this module can compute division because the divisor is a power of 2. Indeed, the binary division by 2^P simply corresponds to a P-bit shift. The number of bits of the Exploitation Module is given by the following equation:

$$P = -\log_2(\delta INL) + n \quad (4)$$

Where δINL is the required accuracy for the Integral Non-Linearity measurement and n the ADC resolution. For INL correction with LUT accuracy of 0.2LSB is sufficient. The number of blocs is thus equal to 3+n. As illustration, the Figure 3 gives the circuitry needed for implementing a 3 bit-EM register.

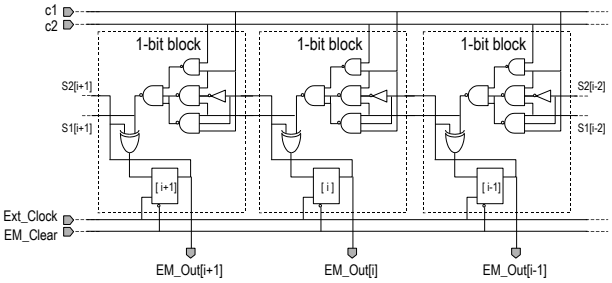

Figure 3. The Exploitation Module register

D. Analog signal generator

As for the histogram BIST, many papers have been published proposing efficient implementation for on-chip input signal generation. Consequently, an existing published solution is reused and modified to be compatible with the specific requirements of our on-chip auto-correction technique. In [27] a solution is proposed for ramp and triangle wave analog signal generation. For our auto-correction scheme, only the ramp generator is interesting and will be adapted.

This analog generator is based on the very simple principle of a constant current charge of a capacitor. Figure 4 shows the conceptual scheme of the ramp signal generator [27] where Ic, C, Init and Step are respectively the charging current, the charge capacitor, the initialization signal and the signal for ramp duration.

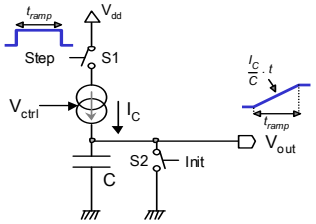

Figure 4. Ramp generator

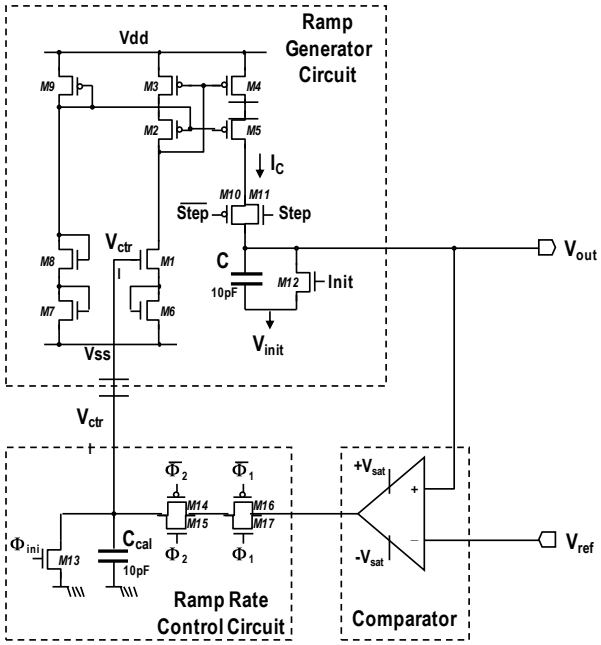

Figure 5. Ramp generator

In order to achieve a satisfactory quality in terms of linearity, the generator is based on Wide Swing current mirrors. These mirrors copy the current generated by a single transistor with a controlled gate-source voltage. This architecture allows one to achieve 15 bits of linearity. In addition, an adaptive scheme is implemented to calibrate the slope of the ramp in situ, in the application. It is made of a comparator and a ramp rate control circuit which control the value of the charging current. Figure 5 shows the transistor level representation of the adaptive ramp generator.

Using such an analog adaptive scheme, the calibration process starts with a number of iterations in which the control voltage is progressively incremented until the ramp voltage reaches the reference voltage (Vref) within the given period. This control voltage then oscillates around the proper value in the following iterations, indicating that the calibration is completed has illustrated in Figure 6 for low frequency stimulus.

The basic idea is obviously to use this adaptive scheme to adapt the slope of the ramp for the in situ calibration into the application. The ramp period is fixed by a digital signal and the adaptive system manages the charging current to obtain the period for a dynamic range equal to the ADC under calibration.

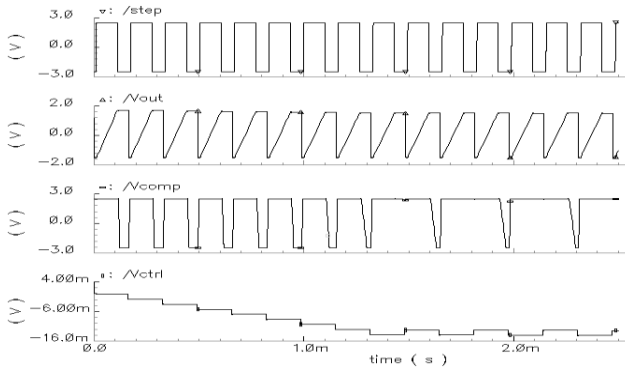

Figure 6. Adaptive ramp generator simulation

E. *Global implementation and operation*

The algorithm for the LUT filling is depicted in Figure 7. For each ADC output code O(i), we compare the absolute value of its INL to 0.5LSB. If the |INL| is smaller than 0.5LSB, we fill the LUT with the expected code O(i) at the address O(i). If the INL is higher than 0.5, we calculate a corrected output code which will be stored in the LUT at the address O(i). To do so, we round the INL value to the nearest integer. Then we subtract the expected code O(i) to the computed compensation $C_p(i)$ to obtain the corrected output code $C_r(i)$. Obviously, $C_r(i)$ is bounded by 0 and 2^N-1.

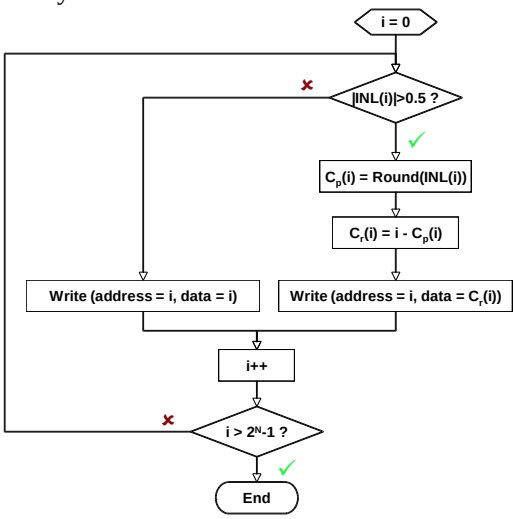

Figure 7**, *LUT training algorithm***

The controller used to manage the INL estimation and the correction algorithm is very simple with a negligible impact in terms of area overhead in comparison to the LUT and the ADC.

IV. VALIDATION OF THE IN SITU AUTO-CORRECTION

A. *Platform*

Under *Labview*, we have developed a platform where an ADC is defined by its resolution and its INL, and we can extract its transfer function and its response to different input signals such as sine wave, triangle, ramp… The platform is divided into 4 parts: the first defines the test stimuli, the second sets the ADC characteristics, the third computes the dynamics parameters (SINAD, THD, ENOB and SFDR) and the last displays the output responses with or without correction.

B. *Validation*

The validation is performed with a 10-bits ADC. We studied two conditions (#1 and #2 in Table 1) corresponding to two different applications with two-targeted bandwidths. For the first condition, the maximum INL is equal to 2.7LSB. For the second condition, the maximum INL increases to 0.3LSB due to the dynamic part of the INL.

	Dynamic parameters	ADC	LUT #1	LUT #2
Cond. #1	ENOB	8,75	9,45	9,14
	THD	-57,88	-77,07	-61,96
	SFDR	-59,77	-72,66	-64,48
Cond. #2	ENOB	8,41	9,15	9,34
	THD	-54,62	-61,75	-71,24
	SFDR	-57,63	-63,62	-70,38

Tableau 1, Dynamic parameters for ADC with and without post-correction

1) *Correction of INL in condition #1*

As depicted in Figure 8, the INL is closed to 0 for lower code and reach 2.7 LSB for upper code. In such case, the uncorrected ADC has an ENOB of 8.71 bits, a THD equal to -57.38dB and a SFDR equal to -59.49dB. After applying post-correction, the ENOB is 9.45bits, the THD is equal to -77.07 and the SFDR is equal to -72.66dB. As soon as the INL is outside the bandwidth of -0.5LSB and +0.5LSB, the output is corrected as shown in Figure 8.

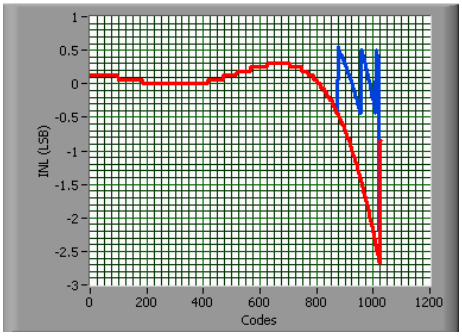

Figure 8, measured INL with and without post-correction

2) *Correction of INL in condition #2*

As exposed in [6], the post-correction technique is better for input signal frequencies near from the frequency used for the histogram test. Consequently, the LUT filled in previous condition is less effective in condition #2 (see dynamic parameters in Tableau 1 for LUT #1 in condition #2). However, due to this adaptive LUT-based correction approach, we can apply a new calibration for a better correction in this condition. So, for the INL depicted in Figure 9, the ENOB decreases to 8.27bits rather than after post-correction, the ENOB is still 9.34bits. The THD is -54.62 and -71.24 without and with post-correction respectively. The SFDR is -57.63dB rather than -70.38dB after post-correction.

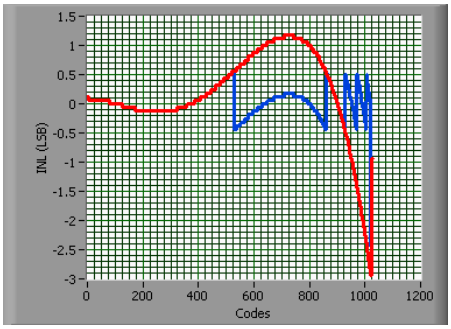

Figure 9, measured *INL with and without post-correction*

V. Conclusion

In the context of high speed and high resolution ADCs with calibration capabilities, we have proposed in this paper an original auto-correction scheme which is able to perform the auto-calibration in situ, i.e. directly in the application. This in situ auto-calibration approach has the main advantage of taking into account implicitly the environment conditions and the aging effects. In addition, the calibration is performed with an integrated adaptive signal generator providing an input signal tuned according to the application, i.e. taking into account the dynamic effects coming from the application signal speed. Both adaptive input signal generator and output INL estimator based on the histogram technique are described. The whole correction scheme is proved to be effective through extensive simulations.

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