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A Low Power Interface Circuit for Resistive Sensors with Digital Offset Compensation

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Abstract - This paper presents an innovative conditioning and read-out interface for resistive MEMS sensors. The proposed structure includes a digital offset compensation for robustness to process and temperature variations. Simulation results demonstrate an impressive resolution to power consumption ratio and a good immunity to environmental parameters. Experimental results finally demonstrate the efficiency of this promising read-out architecture.

I. INTRODUCTION

Since resistive sensors exist, the Wheatstone bridge has been the most commonly used conditioning and read-out architecture [1]. Even with the development of MEMS in the last decade, the Wheatstone bridge remains the preferred solution to transpose a physical magnitude into the electrical domain as soon as a resistive transduction method is used. The Wheatstone bridge introduces a major issue for low-power sensors, the dependence of resolution to power consumption [2]. On the one hand, the smaller the resistance, the higher the current in the bridge is. On the other hand, the higher the resistance, the higher the noise floor is. Moreover, the output signal is directly proportional to the supply voltage. Finally, power consumption is the price to pay for high resolution in a Wheatstone bridge.

Low-power requirements, in mobile applications, are probably one of the main reasons to explain why capacitive transduction has been preferred for many MEMS [3]. Indeed, even if the fabrication process is often more complex than for resistive sensors, the power consumption of capacitive transduction is far below the one of resistor-based sensors.

In order to extend the potential application of resistive MEMS, a power-efficient interface circuit is required. In this paper, we first study the limitations introduced by the Wheatstone bridge to the intrinsic performance of a bare

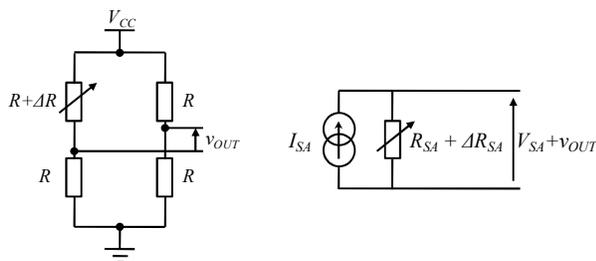


Figure 1. Resistive sensor conditioning and reading: in a Wheatstone bridge (left) or as a stand-alone resistor (right).

resistive sensor. We, then, introduce the principle of the proposed “active bridge” as an efficient alternative that allows power consumption savings and optimum resolution. We also present a possible implementation of this low-power interface with an offset cancelation scheme to increase sensor robustness to temperature and process scatterings. Finally, experimental results on a demonstrator illustrate the versatility of the proposed solution.

II. PRINCIPLE OF THE “ACTIVE BRIDGE”

A. Wheatstone bridge versus bare sensor

Let us first consider a bare resistive sensor with two possible conditioning schemes: i) placing it in a Wheatstone bridge or, ii) biasing it with a current generator (Fig. 1). To compare the resolution of both solutions, one can study the signal to noise ratio (SNR). For simplicity, voltage ratios are used in this paper. First, resolution for the Wheatstone bridge writes [4]:

$$SNR_{Wheat} = \frac{\Delta R}{R} \frac{V_{CC}}{4} \frac{I}{\sqrt{4kTR} \sqrt{BW}}, \quad (1)$$

where k is the Boltzmann constant and BW the considered bandwidth. As previously mentioned, the resolution increases with the supply voltage and decreases with the resistance (even if $\Delta R/R$ is independent of R). If we now consider the direct biasing of the gauge with an ideal current source (I_{SA}), it comes:

$$SNR_{SA} = \frac{\Delta R_{SA}}{R_{SA}} \frac{R_{SA} \times I_{SA}}{\sqrt{4kTR_{SA}} \sqrt{BW}}. \quad (2)$$

Now, the resolution increases with the resistance and, for the same gauge ($\Delta R/R = \Delta R_{SA}/R_{SA}$), a better resolution is achieved if $R_{SA} \times I_{SA} > V_{CC}/4$ [5]. In order to compare deeply both resolutions, we substitute R_{SA} , in (2), by the ratio V_{SA}/I_{SA} . Similarly, V_{CC}/I substitutes R in (1), I being the total current in the bridge. Finally, the ratio of SNR_{SA} to SNR_{Wheat} writes:

$$\frac{SNR_{SA}}{SNR_{Wheat}} = 4 \sqrt{\frac{V_{SA}}{V_{CC}} \frac{I_{SA}}{I}}. \quad (3)$$

From (3), it is obvious that the stand-alone resistance configuration can produce significant performance improvements. Assuming $V_{SA} = V_{CC}/2$ and the same current consumption, the stand-alone resistor resolution (i.e. SNR)

will be $2\sqrt{2}$ higher than the Wheatstone bridge one. For same resolutions, the stand-alone sensor will consume 8 times less current than a Wheatstone bridge.

Electrical simulations (Fig. 2) are reported for a 10 ppm relative variation of the resistance ($\Delta R/R$) in case of a resonant sensor ($20\text{kHz} < \text{BW} < 25\text{kHz}$). For each biasing current, we use $R = 2.R_{SA}$ to keep V_{SA} equal to $V_{CC}/2$, which corresponds to the voltage drop across a resistance in the Wheatstone bridge. This simulation setup will be used along this paper in a $0.35\mu\text{m}$ CMOS technology.

Results confirm what we expected from (3), and the stand-alone resistance leads to a better resolution for a given power consumption or a lower power consumption for a given resolution. However, let us note that this intrinsic resolution is somewhat unachievable as it may correspond to a very low output signal that depends only on the supply voltage (e.g. $8.25\text{mV}/\%$ for 3.3V). Additional amplification is thus required and increases the power consumption. For reference purposes, we assume that $200\mu\text{A}$ are necessary to amplify the intrinsic signal without notable noise degradation and two additional curves are reported (Fig. 2). As a partial conclusion, a good readout interface is then a circuit that would give rise to a SNR curve located between the standard solution one (Wheatstone bridge + LNA) and the ideal case one (Standalone resistance).

B. The “Active Bridge”

The low-power detection of a small resistance variation without noise and power degradation is the challenge that we are addressing with the active bridge. The seed idea is to compensate the dissipative behavior of resistors by using the same current to bias the resistor and to amplify the small output signal.

The proposed circuitry relies on a common gate arrangement of a MOS transistor (T_I in Fig.3.a). If the transistor is saturated, it will amplify a small variation of the sensing resistance through a modulation of the gate-source voltage (V_{GS}). Indeed, a small increase of R_{BRIDGE} will induce a reduction of V_{GS} and thus a far more important increase of the drain-source voltage of T_I to keep the drain-

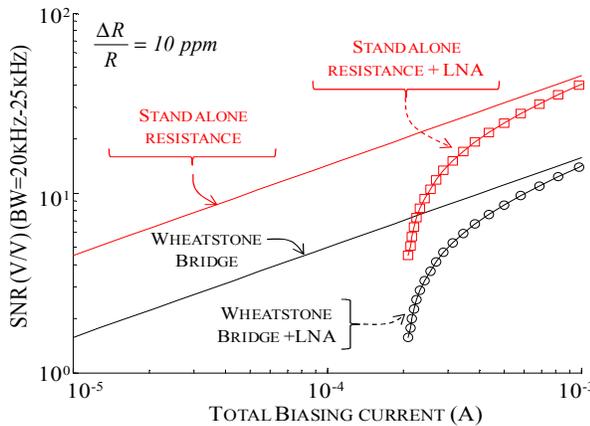


Figure 2. SNR as a function of the current consumption for various conditioning and reading schemes.

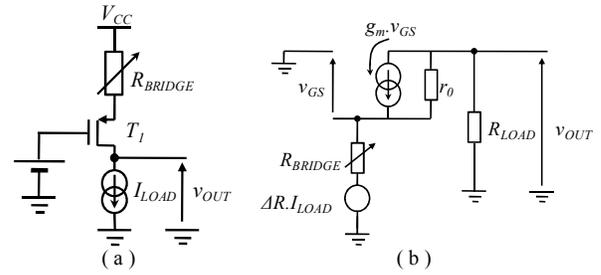


Figure 3. “Active bridge” principle (a) and its small-signal model (b).

source current constant. Therefore, a small variation of the voltage drop across the sensor translates in a larger variation of the output voltage.

In order to determine the output signal, we use a small signal analysis in which a small variation of the gauge will induce an input voltage ($\Delta R.I_{LOAD}$) representing the variation of the voltage drop across the resistance. The obtained model (Fig. 3.b) leads to the following small signal output voltage:

$$v_{OUT} = \frac{g_m R_{LOAD} r_0 + R_{LOAD}}{r_0 (1 + g_m R_{BRIDGE}) + R_{LOAD} + R_{BRIDGE}} \Delta R.I_{LOAD}, \quad (4)$$

where R_{LOAD} is the output resistance of the current source I_{LOAD} . There are different ways to implement the current source of the active bridge. The most adequate is a cascode-like current source that increases R_{LOAD} and reduces the noise impact of the current source [6]. Simulation results (Fig. 4) illustrate the SNR improvement due to the cascode current source (diamonds) with respect to the implementation of I_{LOAD} with a simple N -MOS transistor. For large value of R_{LOAD} , the intrinsic signal ($\Delta R.I_{LOAD}$) may be amplified sufficiently to avoid the use (and the consumption) of an additional amplifier. As an example, if we consider $R_{LOAD} \gg r_0$, a gain of several hundred could be reached thus leading to sensitivity higher than $1 \text{ V}/\%$. At this point, we have demonstrated that the “active bridge” concept is an efficient interface for a resistive sensor. In the next section, we will study the robustness of such a device with respect to process variability and ambient temperature.

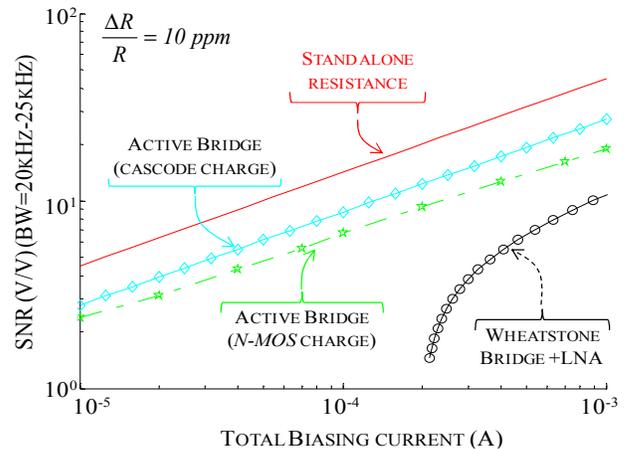


Figure 4. SNR of the active bridge compared to both “ideal” and standard solutions as a function of the current consumption.

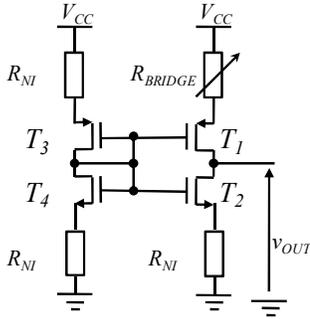


Figure 5. Differential architecture of the “active bridge”.

III. ROBUSTNESS OF THE “ACTIVE BRIDGE”

The main interest of using a Wheatstone bridge is its immunity to environmental disturbances. This is due to its differential topology that rejects effects of global variations such as temperature or supply voltage. Due to its large sensitivity, the simple structure (Fig. 3.a) saturates as soon as a temperature variation occurs. Hence, in order to merge, the “active bridge” benefits and the Wheatstone bridge robustness, we propose to extrapolate the “active bridge” to a differential topology. One possible implementation, out of numerous variants [7], is presented in this paper (Fig. 5). This version is self-biased and does not require any reference voltage or external stages thus keeping the power consumption and the silicon cost very low.

Electrical simulations (Fig. 6) of the proposed differential architecture demonstrate that, unlike for the simple bridge, the sensitivity drift is very small. Over a wide range of temperature (160°C), the sensitivity reduces from 1.66 V/% down to 1.5 V/%. This corresponds to a change in sensitivity of less than 0.07%/°C.

Another robustness issue comes when considering process-induced offset. Due to the huge sensitivity of the structure, even a very low mismatch between identically designed devices will bring the output voltage to deviate from the calculated bias point. That is the reason why open-loop operation of such a device is not possible. We have then studied several offset cancellation scheme. The one presented here (Fig. 7) uses a digitally controlled feedback trimmer.

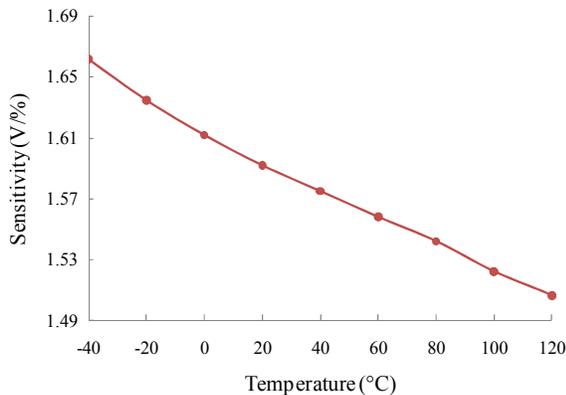


Figure 6. Sensitivity as a function of temperature for the differential active bridge with cascode-like charge.

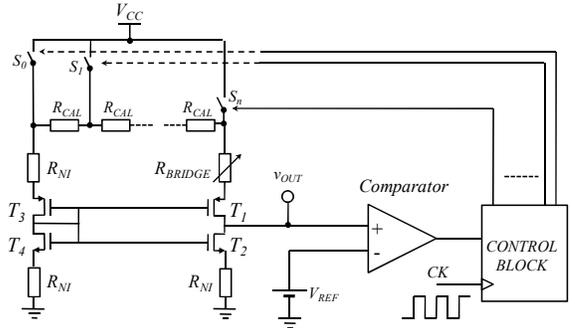


Figure 7. Differential “active bridge” with offset cancellation feedback.

The later implements a resistance ladder to balance the differential “active bridge”. A set of switches configure properly the ladder when a clock signal is applied to a digital control block featuring a voltage comparator as input stage. It is worth noting that the comparator and its reference voltage is a conceptual view and that the digital input of the control block will be designed to reduce extra power consumption.

Assuming 1% of mismatch between identically designed resistances, the value of R_{CAL} is set one thousand times smaller than R_{BRIDGE} ($=R_{NI}$). The number of elements in the ladder can be freely chosen with a direct impact on the output quiescent voltage resolution but with a minor impact on power consumption and size.

To validate the proposed offset cancellation scheme, we have performed Monte-Carlo simulations using both process (wafer to wafer) and mismatch (intra die) variations. In this worst case, immunity to process variation is clearly established (Fig. 8).

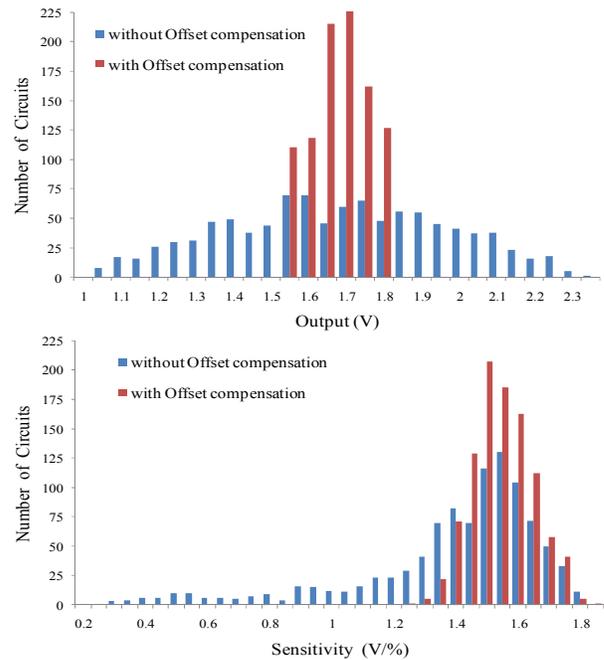


Figure 8. Effect of the offset cancellation structure on the bias point (output voltage, top) and on the sensitivity (bottom).

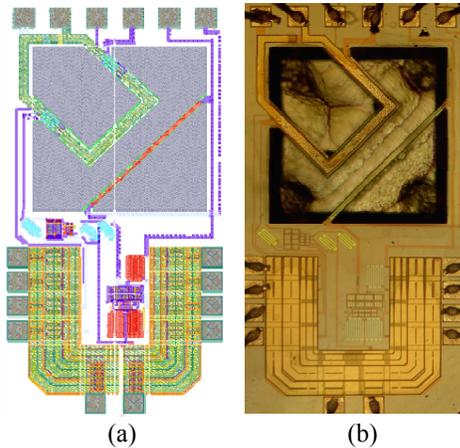


Figure 9. Layout (a) and photograph (b) of an all-in-one earth magnetic field sensor with differential active bridge conditioning and reading.

IV. EXPERIMENTAL RESULTS

A first demonstrator has been designed and fabricated for the conditioning and reading of a resonant earth magnetic field sensor [8]. The circuit was manufactured in a $0.35\mu\text{m}$ technology from AMS and the post-process to release MEMS structures has been arranged by CMP (Fig. 9).

This first prototype allowed the validation of the differential active bridge for all previously reported aspects. We also observed the ability of simulation to predict the silicon results. For this first « monolithic » demonstrator, the supply voltage was the only-possible input apart from the physical magnitude to be measured. For shortness, we report in this paper only the variation of the sensitivity as a function of the power supply voltage (Fig. 10). A similar behavior has been obtained when studying the bias current variation with supply voltage. The wide range of operation, the predictability of dependence and the efficiency of the structure are obvious.

In this prototype, a single $4\text{k}\Omega$ strain gauge was arranged in a differential active bridge together with three reference resistors (as in Fig. 7). Under a supply voltage (V_{CC}) of 2V, a power consumption of about $300\mu\text{W}$ is sufficient to obtain an output signal close to 1V for a 1% variation of the resistive gauge. The same gauge in a Wheatstone bridge would deliver a 5 mV output signal with a 1mW power consumption. However, dependency of the sensitivity with the supply voltage is a real issue in terms of calibration and/or power supply rejection ratio. This point may be tackled by biasing the structure with a current rather than a voltage.

The stability with temperature and thus the variations of the sensitivity with temperature has not been yet characterized. With a second prototype not illustrated in this paper, we have also verified that an active bridge may adapt to a wide range of resistance at a price of a varying sensitivity. Indeed, when increasing the value of the gauge for a given structure, the bias current reduces and the output signal follows.

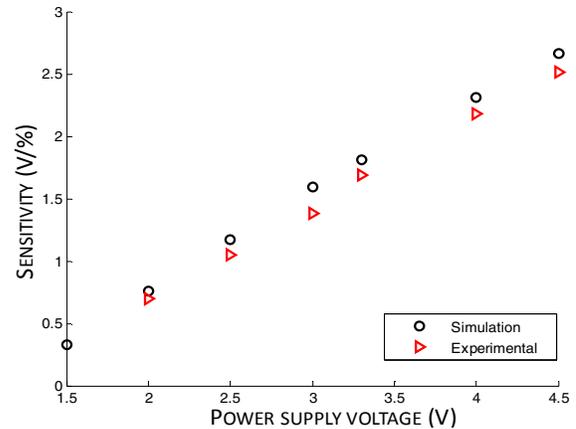


Figure 10. Differential Active bridge sensitivity as a function of the supply voltage.

V. CONCLUSION

In this paper, we presented an innovative interface circuit suitable to all kind of resistive sensors. Based on “level 1” modeling, electrical simulations and experimental results, we illustrated several of the key features of the structure that are recalled as a conclusion:

- Robust to temperature and process variations,
- Easy to scale to any resistive sensor,
- Low-power operation,
- Maximal resolution (very small SNR degradation compared to bare sensor).

Works in progress concern the study of closed loop operation in order to adapt the digital feedback and to obtain a low-power resistive sensor interface with digital output.

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