Effective Interconnect Networks Design in CMOS 45 nm Circuits to Joint Reductions of XT and Delay for Transmission of Very High Speed Signals

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Effective Interconnect Networks Design in CMOS 45 nm Circuits to Joint Reductions of XT and Delay for Transmission of Very High Speed Signals

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***Abstract*— When high speed integrated digital circuits technology scales down from one node to the other as ITRS recommends, a significant gain is obtained on signal speed, consumption and area of CMOS transistors. Nevertheless a specific issue occurs from the 45 nm technology node. The obtained gain on active devices is foiled by an increase of interconnect propagation delays and critical crosstalk (XT) levels in the Back-End of Line (BEOL). This issue especially concerns relatively long (few hundred of μm) interconnects of the intermediate metal level. By introducing drivers (repeaters) in order to divide long interconnect in shorter sections and choosing optimal drivers sizes, speed can be maximized as well as crosstalk levels are alleviated. The present studies aims at specify couple of intervals for both section lengths and drivers size in accordance with speed and crosstalk levels requirements of future ICs. When it becomes hard to meet all requirements, it is shown that the interconnect density constraint should be relaxed.**

I. INTRODUCTION

According to Moore's law and ITRS recommendations [1], each new generation of integrated circuits (ICs) has to target a high level of integration. Nevertheless, from generation of the CMOS 65 nm technology node, the IC's speed increase gained on active devices is partially loosed. This is mainly due to interconnects delays increase as dimensions of interconnects are shrunk to satisfy integration requirements [2]. Moreover, from the 45 nm generation, worrying crosstalk (XT) levels are expected [3],[4]. These critical XT levels might easily affect signal robustness and integrity. Thus, they would cause many malfunctions such as voltage level errors and signal overshot leading to transistors damages and ICs consumption increase [5],[6]. These XT levels are particularly noticeable in the intermediate metal level of the Back-End of Line (BEOL) stack (Fig. 1) which contains relatively long interconnect (hundreds of μm long) that are very closed to each other. In accordance with ITRS, the half pitch of interconnects of the intermediate level, equal to distance *s* between adjacent interconnects, is around 50 nm while their thickness *t* is exceeded hundred nm. In term of electrical characteristics, two major phenomena on circuit performance come with dimension shrink in the BEOL. The first one is the rise of the *RC* product, where *R* and *C* are respectively the distributed resistance and capacitance of interconnect. It is worth noting that, in first approximation, the interconnect delay increase is linear with *RC* and quadratic with interconnect length. Consequently, fast signal transmissions (up to 5 GHz) becomes impossible on relatively long interconnects. Repeaters must be introduced to speed up signals propagation thanks to interconnect division into smaller sections. The second phenomenon stands in increase of mutual capacitances between adjacent interconnects in the same metal level, causing possible dramatic XT levels. However, if interconnect is divided in smaller sections, the XT level tends to decrease thanks to length reduction. In this way, repeaters introduction helps to reduce XT levels while maximizing ICs speed at the same time. The choice of the optimal number of drivers to be introduced is a first manner to reach the targeted signals speed and respect constraints of maximal XT levels at the same time. Another approach toward these goals stands in the choice of the optimal driver size. Nevertheless, it is worth noting that both drivers introduction and driver dimensioning could significantly increase active device area. The present study firstly targets specifications on couple of intervals ($[l_{opt}]$, $[S_{opt}]$), respectively standing for the interconnect section length and drivers sizes in order to optimize performance. Then, two major questions must be answered. The first question stands in knowing if speed maximization on one hand and XT level on the other, converge across the same couples of intervals ($[l_{opt}]$, $[S_{opt}]$). Affirmatively, the second issue stands in specifying if speed and XTs optimizations are sufficient to reach laid down constraints in accordance with future high speed digital circuits requirements. Finally, this study proposes a third scheme to reach more demanding requirements. These last consist in dedicating a specific additive metal level characterized by relaxed interconnect density for the most critical paths. Indeed, by relaxing interconnect density constraint, both *RC* product and mutual capacitance C_m are decreased, alleviating harms due to integration listed previously.

TABLE I. TYPICAL 45 NM INTERCONNECT PARAMETERS

BEOL	Dimensions	Materials
Intermediate Metal Level	$50 < w = s < 70$ nm $t \approx 140$ nm	copper $\sigma \approx 35$ MS/m
Dielectric SiOCH	$h \approx 120$ nm	$\varepsilon'_r \approx 2.6$ $\varepsilon''_r = 0$
Metal barrier TaN/Ta	$t_{mb} \approx 7$ nm	$\sigma \approx 1{,}4$ MS/m
Dielectric barrier SiCN	$t_{db} \approx 40$ nm	$\varepsilon'_r \approx 5$

II. Description of Carried Out Simulations to Evaluate Interconnect Performance in the BEOL

A. *Drivers and interconnects description of the intermediate metal level associated to the BEOL of the the 45 nm node*

In ICs, interconnect generally links upstream driver with downstream driver (CMOS inverters) as represented on Fig 2. Upstream and downstream driver's electric behavior acts as source-drain resistance R_{inv} and gate capacitance C_{inv} respectively. R_{inv} and C_{inv} depend on one hand on technology which fixes the gate length L_g (e.g. 45 nm) and on the driver size on the other hand. Driver size is a specification of the gate width W_g. expressed in multiple of L_g. Thereby the driver size has strong impact on the delay between two active devices. As a large driver (e.g. x 32) has lower resistance than a small one (e.g. x 2) its response delay will be shorter. Active devices are interfaced with interconnects which significantly raise themselves the delay while they are relatively long (hundreds of µm). Interconnects are characterized by distributed *RLCG* parameters. Because of the high density of the BEOL network, not only self *RLCG* but also neighboring mutual $R_mL_mC_mG_m$ parameters between interconnects are considered. At last access resistances R_{acc} at the interface due to contacts and inter levels vias must be taken into account.

In the following part, interconnect performance inside a network of the very metal level is evaluated. Driver parameters are evaluated by electric simulations. Self and coupled *RLCG* parameters are accurately evaluated by electromagnetic simulations. Theses last take into account interconnect width w, space s and thickness *t*, dielectric high *h* as well as technologic stack including material properties, metallic and dielectric barriers (as illustrated on Fig. 1 and Fig. 3). Tab. 1 illustrates typical parameters specification of the 45 nm technology node [7].

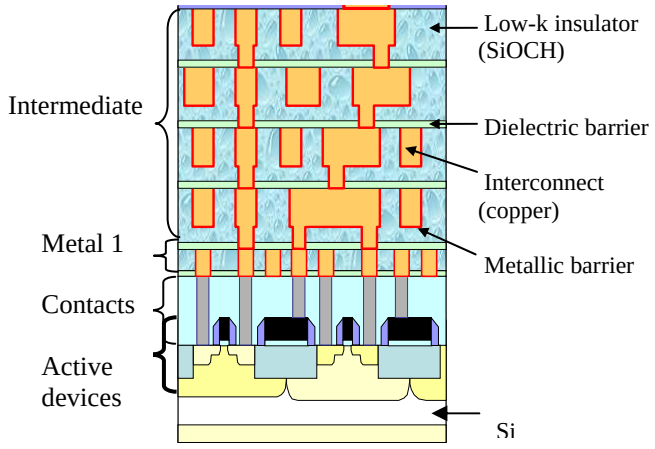

Figure 1. IC cross section illustrating hierarchical interconnects levels

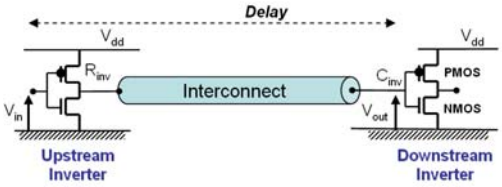

Figure 2. Schematic illustration of inter-gates path (input and output voltages on interconnect loaded by inverters are represented also)

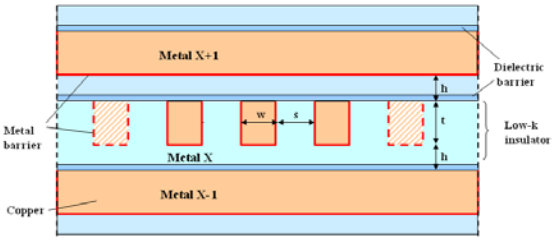

Figure 3. Illustration of intermediate metal levels modeling in BEOL

B. *Carried out simulations*

Simulations depicted according to the scheme presented on Fig. 4: three adjacent interconnects are driven by inverters inside the very intermediate metal level. Two main features are concerned. The first one is worst case XT level: the middle interconnect is not driven while two adjacent ones are driven from low to high level. Because of coupling (especially capacitive) between adjacent interconnects, a harmful voltage level appears on the adjacent downstream driver (Fig. 4 and Fig. 5). The second one is worst case delay: interconnect in the middle is driven from low to high level while two adjacent ones are driven from high to low level. The delay is a measure of the duration between the time of excitation (at 50% of voltage level) at the input of the upstream inverter and the time of arrival at the input of the downstream inverter (Fig. 2 and Fig. 5). This configuration is a worst case scenario because the delay is unfavorably increased by XT.

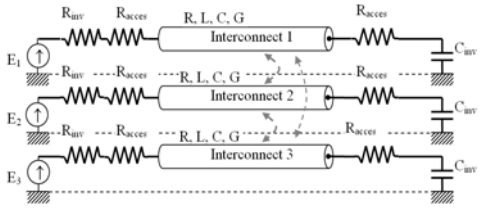

Figure 4. Illustration of 3 coupled interconnects with respective loads and excitations

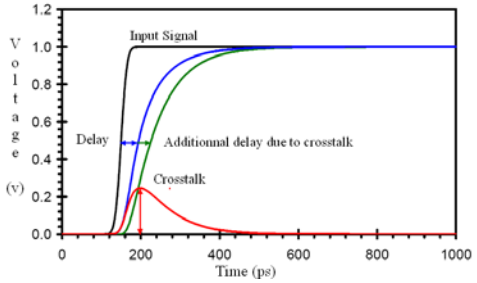

Figure 5. Typical time response illustrating delay, XT and delay increased by XT

III. Effect of Interconnect Length on Speed

Beyond critical length of interconnect sections, delays become so high that high speed signal (few GHz or more) transmission are prevented. Thereby length of interconnect sections must be limited at few hundreds of µm. On the other hand, as few paths could reach up to around 1 mm in the BEOL, repeaters must be introduced to section path into shorter interconnect sections. But the cost linked to path cutting, including drivers insertion, contacts and vias, becomes prohibitive if interconnect sections are too short. In order to refine these assertions, this study focus on nominal lengths of interconnects sections comprised between few tens of µm and few hundreds of µm. The concerned metrics are both costs and performance. At last, the effect of interconnect lengths on performance is evaluated for different driver sizes (x 4 and x 64). As we can see on Fig. 6 and Fig. 7, delays dramatically increase with interconnect length whatever the driver size. Nevertheless, the choice of sufficiently large drivers helps to reduce delays up to almost 50% whatever the interconnect length. This gain is due to the fact that resistances of small driver (e.g. x4) predominate capacitances in comparison with respectively resistances and capacitances of the interconnects. An other way to reduce delays is to introduce repeaters to diminish interconnect section length. Indeed, from around 70 µm, gain on delay is obtained by sectioning interconnect, that means introducing repeaters.

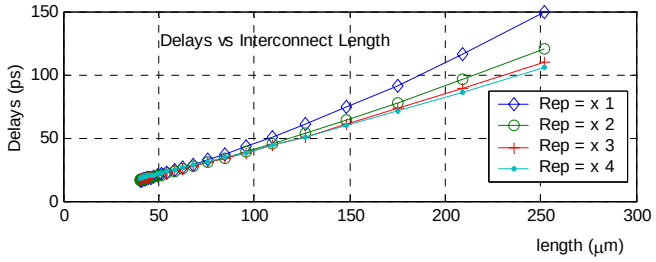

Figure 6. Impact of interconnect length on delays for driver size = x4 and different number of reapeaters

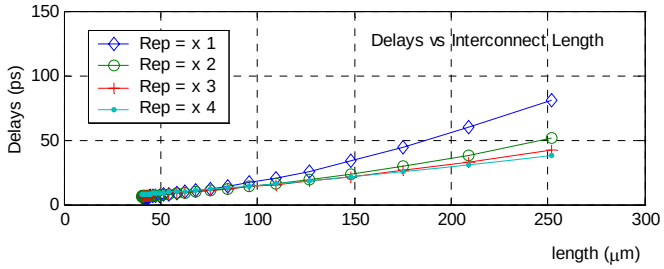

Figure 7. Impact of interconnect length on delays for driver size = x64 and different number of reapeaters

IV. Global Design Optimisation to Reach Robust High Speed Performance

A. *Optimisation of drivers number and size to respect strict crosstalk constraints*

As this study especially focuses on XTs, two cases are envisioned. In the first case, so-called Far-End XT (FEXT), excitation on the victim interconnect is at the same end that excitation of the aggressing one. In the second case, so-called Near-End XT (NEXT), excitation on the victim interconnect is at the other end that excitation of the aggressing one. Typical XT constraint span between 30 and 40 %. These targeted limitations allow avoiding transmission errors on digital signal. Nevertheless these constraints should be stricter in order to limit additional circuit consumption (especially short-circuit consumption) and signal overshoots which will damage active components. Thereby the present study focuses on an extended interval of XT levels comprised between 25 and 40 %. It has been shown above that reduction of interconnect section length is a mean to diminish both delay and XT levels. Nevertheless, as we can see on the Fig. 8, the benefit of length reduction on XT has not the same strength for small driver and large drivers. Indeed, for small drivers, XT level is nearly constant with section length while for large drivers XT levels significantly increase with section length. Moreover, for short section lengths (under around 150 µm) XT level decrease with drivers size while for long section lengths the opposite behavior is observed.

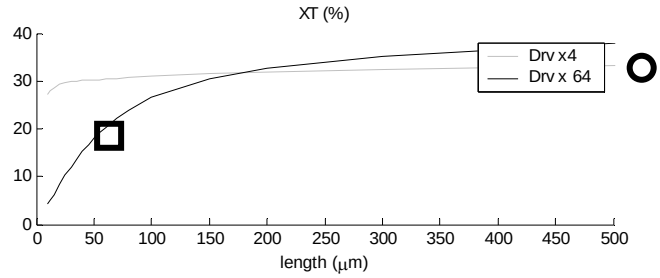

Figure 8. Comparison of the impact of interconnect section length on performance for driver sizes = x4 and x64

In first conclusion, if XT constraints are not too much strict (e.g. > 35%), small drivers associated to relatively long interconnect sections (hundreds of µm) are sufficient. For example of comparison on Fig. 8, if this minimum level is around 40 % for a 500 µm interconnect, a small driver (x4) without repeaters can be used (circle point). In this case, the active component cost is relatively low thanks to both small size and number of required drivers. On the other hand, if the maximum acceptable XT level becomes smaller, larger and more numerous drivers are needed. For example (square point on Fig. 8), if this minimum level is around 20 % for a 500 µm interconnect, a large driver (x64) with numerous repeaters must be used.

B. *Optimisation of drivers number and size to reach robust high speed performance*

Signal speed and maximal XT levels are supposed to be laid down by designer for a targeted IC's application. But the more the application is demanding in terms of speed and robustness the higher cost and consumption will be. Indeed, if jointly signal speed and XT levels requirements are low (e.g. speed < 1 GHz and maximum XT level <40 %), long interconnect sections with small drivers are sufficient without particular issue for XT levels because they are nearly constant

with interconnect section length for small drivers (e.g. x4 on Fig.8). But in the case of high speed signals that are concerned by the present study, the speed will be maximal for relatively short section lengths (around 50 µm). On fig. 9, is represented the optimal section length L_{opt} that maximize the signal speed. It can be observed that L_{opt} is nearly constant with driver size. Then, L_{opt} is compared with maximal section length L_{max} respectively linked to 25, 30 and 40 % maximal XT level specifications. It can be observed that L_{opt} is in accordance with XT requirements whatever the driver size, except for the strictest case (XT < 25 %) for which minimal driver size (> x4) is required (circle point on Fig. 9).

In second conclusion, as far as designers respect the maximal section lengths L_{max} linked to XT requirements, they could choose short section length (around L_{opt}) to obtain very high speed circuits with a significant cost linked to repeater introduction. On the other hand, if the circuits speed requirement is not too much high, they can spare repeaters by choosing L between L_{opt} and L_{max}.

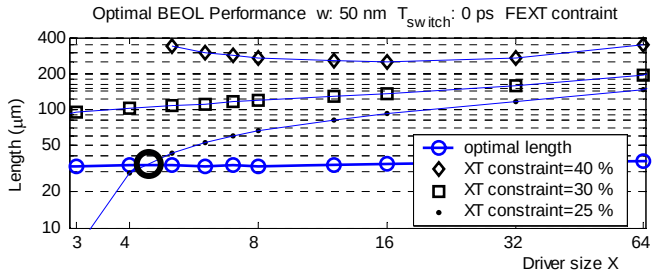

Figure 9. Impact of driver sizes on the maximal required section length in accordance with different XT constraints for a nominal ½ pitch = 50 nm

C. *Effect of interconnect density on performance*

The cost due to potentially large numerous drivers can be prohibitive or the circuit speed obtained can be insufficient. There is also a third way to find best trade-off between cost and performance. By relaxing the interconnect density in the critical intermediate metal levels, all other design constraints could be lightened, as it is shown on Fig. 10 for a relaxed ½ pitch = 70 nm. Moreover, even for strict XT constraint (e.g. 25 %), the use of large drivers is not necessary. Finally, as it is shown on Fig. 11, interconnect density relaxation in the BEOL is an efficient way to increase signal speed. For example, interfacing interconnect with optimal drivers size S_{opt} equal to x32, the increase of the ½ pitch from 50 nm to 70 nm allows to increase the optimal speed from 7 µm/ps up to 10 µm/ps, that is 43% gained on speed.

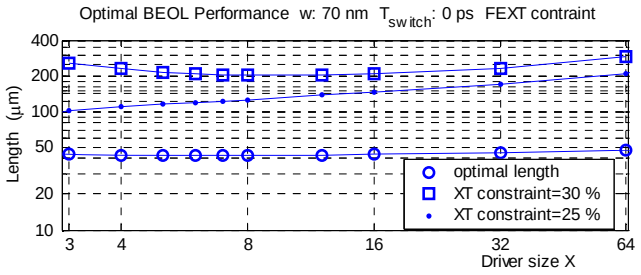

Figure 10. Impact of driver sizes on the maximal required section length in accordance with different XT constraints for a relaxed ½ pitch = 70 nm

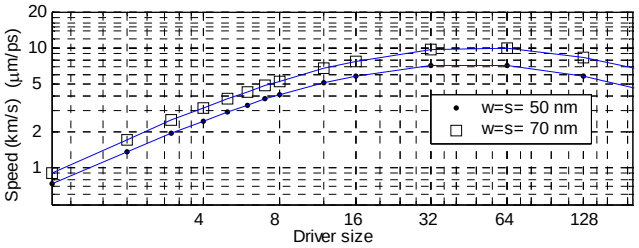

Figure 11. Comparison of the impact of driver sizes on the signal speed for different ½ pitch respectively equal to 50 nm and 70 nm.

V. Conclusions

It as been shown that very high speed circuits of the 45 nm generation require both relatively short sections (around 50 µm), corresponding to potentially numerous repeaters and relatively large drivers (e.g. x32). These requirements imply a significant cost on active component area and consumption. These optimal section lengths and driver sizes are in accordance with very strict XT level constraint. Nevertheless if the circuit speed requirement is lower, numerous large drivers can be spare. Nevertheless, a maximal section length corresponding to a minimal number of repeaters is required depending on the maximum XT level specification whatever the circuit speed. For example for an ½ pitch = 50 nm and a required maximum XT level equal to 30 %, the section length do not have to exceed around hundred µm. A proposed way to lower these joint constraints on cost and performance is to relax the interconnect density. It will allow either improving global efficiency of interconnect network or reducing drivers size and IC's consumption. A mean to reach the interconnect density relaxation is to add specific intermediate metal levels inside the stack of the BEOL. After that, designer should establish the best trade-off between the rise of active device area linked to the use of potentially large repeaters and the additive cost linked to additional metal levels in the BEOL.

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