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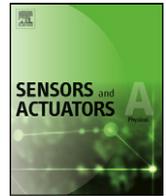
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## Design of smart drivers for electrostatic MEMS switches

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### ABSTRACT

This paper introduces the design of smart high-voltage CMOS drivers for electrostatic actuators. Smart must be understood as the capability of the driver to deliver the required voltage to close a MEMS switch and to diagnose whether the electrode moves well or not. This way, stuck or broken switches could be easily identified during operation. To implement such an online diagnosis, we propose to equip the driver architecture with a dedicated circuitry that can detect pull-in events. Pull-in corresponds to a rapid change of the actuation capacitance thus producing a charging current peak. The idea is therefore to monitor the charging current, and to track a current peak that could be small with respect to the current that charges parasitic capacitors. In this paper, we propose two different architectures to cancel parasitic capacitance effects. Both are introduced, studied by simulation and implemented on silicon. Complete demonstration is finally performed with an academic prototype of a MEMS switch.

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### 1. Introduction

Over the last decade, MEMS RF switches have raised interest for replacing traditional PIN diodes in RF telecommunications because of their unrivaled low insertion losses [1]. Although much works have been carried out to improve their reliability, the integration of such devices in high-end systems cannot be considered without some level of tolerance against possible MEMS failures. One possible tolerance scenario then includes redundancies, diagnosis and reconfiguration. This scenario has been chosen here to ensure system-level tolerance to RF MEMS failures.

The targeted system is a reflect array antenna for telecommunication applications. It is based on an array of RF cells, each one containing several metallic patches. Between these patches, MEMS switches are disposed in order to configure RF paths (short or open) so that a continuous phase shift, between incident and reflected waves, can be programmed by changing switch configuration [2]. Redundancy is inherent to the system architecture as different switch configurations may achieve similar phase shifts; so that alternative RF path may be used if non-working MEMS are identified. In [3], it is shown by simulation that only 1.5% of the MEMS can cause a failure of the antenna, whereas, with an optimal correction, the system can tolerate 23% of defective MEMS while still complying with specifications. In order to achieve this level of tol-

erance, the required information is to know the actual position of each switch.

As a huge quantity of MEMS per unit of area is used over a large surface, the control and driving circuitry, including the diagnosis functionality, are integrated into small ASICs distributed on the panel. Each ASIC locally controls a set of MEMS switches. This distributed network of ASIC reduces routing congestion problems and eases diagnosis by placing the diagnosis circuitry close to the switch. The chosen technology is a High Voltage CMOS process [4] because of the high pull-in voltage of the considered switches. It allows integrating both low voltage transistors, for receiving the configuration and transmitting the diagnosis result, and high voltage transistors for driving and testing MEMS RF switches.

The MEMS electrostatic actuator, used to configure RF paths, is composed of a free-ended beam electrically grounded and electrostatically actuated by an independent bottom electrode. Direct measurement of the actuator's capacitance, between beam and control electrode, is a simple electrical way to determine switch position. This solution has been used for capacitive MEMS switches in [5–7] through capacitive bridge based measurements. However, bridge measurements lead to the evaluation of total capacitance that includes large parasitic capacitance, in parallel with the actuator, between the actuation electrode's path and ground. Therefore, such technique needs a calibration phase and a storage memory to remove the effect of parasitic capacitance, assuming a constant value. Another published technique consists in measuring the actuation current only during the switching [8]. This technique is used to monitor reliability of a MEMS switch as a degradation of the switch causes some changes in the current waveform. However,

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the parasitic capacitance effect on the charging current is still not rejected.

In large systems such as our reflect array antenna, parasitic capacitance is so large, compared to actuator's one, that a small uncertainty during calibration would cause a wrong diagnosis. In our case, diagnosis must cope with parasitic capacitance two orders of magnitude higher than actuator's capacitance. In [9], a ramp actuation voltage has been used to better reject the influence of the stray capacitance and obtain a binary diagnosis of a capacitive MEMS actuator. An edge detector circuit and an integrator are used to measure the capacitance variation during the pull-in of the switch. This solution is interesting but requires complex on-chip electronics to design HV ramp generators.

In this paper, we investigate two new, simple, and fully integrated solutions for measuring the capacitance variation during pull-in event. The first is based on a single step actuation voltage and a time based technique to discriminate stray capacitance from parasitic. The second one is based on a two step actuation voltage and a differential technique. For both solutions driving and diagnosis circuits are fully integrated to form smart drivers. Smart must be understood as the capability of the driver to deliver the required voltage to close a MEMS switch, a somehow classical feature, and to diagnose whether the electrode moves well or not which is really innovative. This way, stuck or broken switches can be easily identified during operation. Compared to previously published papers [10,11] from the same authors, this paper emphasizes the use of a behavioral model for the design and simulation of smart drivers and reports extensive experimental results on real RF MEMS switches.

The paper is organized as follows. Section 2 introduces the RF MEMS switch and a simple, but efficient, behavioral model of the actuator is proposed for system-level simulations. Section 3 presents the design of the smart High-Voltage (HV) driver, starting from the basic level-shifter cell. Two diagnosis circuitries are then proposed to detect the pull-in event while cancelling parasitic capacitance effects. Section 4 presents and discusses experimental results obtained with some smart drivers connected to real RF MEMS switches. Section 5 finally summarizes results and, concludes on the effectiveness of the proposed solutions.

## 2. Electrostatic actuator modeling and simulation

### 2.1. RF MEMS switch architecture

The RF MEMS switch used to validate our smart drivers is based on the basic capacitive shunt architecture, shown in Fig. 1, which is very common in RF applications. The role of the switch is to connect two metallic planes together in order to provide a path for the RF waves into the patch. Some details about the fabrication process are available in [12]. The moving part of the switch is a gold cantilever beam, fabricated using standard surface micromachining process, and attached (both mechanically and electrically) to a ground plane. It is actuated by means of a large polysilicon bottom electrode. When actuated, the cantilever beam lands on a thin dielectric layer ( $\text{Si}_3\text{N}_4$ ), deposited on a finger connected to the signal plane, thus connecting the signal plane to the ground plane through a capacitor ( $C_{\text{RF}}$  in Fig. 1). Since plane (and finger) thickness is greater than the thickness of the bottom actuation electrode, the air gap between the cantilever beam and the actuation electrode never closes, preventing the device from known reliability issues associated with high electric fields in dielectrics. The price to pay is a higher actuation voltage and a lower ratio  $C_{\text{Act,up}}/C_{\text{Act,down}}$  which makes the use of  $C_{\text{Act}}$  measurement for diagnosis more challenging, as it will be developed later on in this paper. In addition, the parasitic RC network that results from the routing of the actuation electrode must be taken into account. Note that to

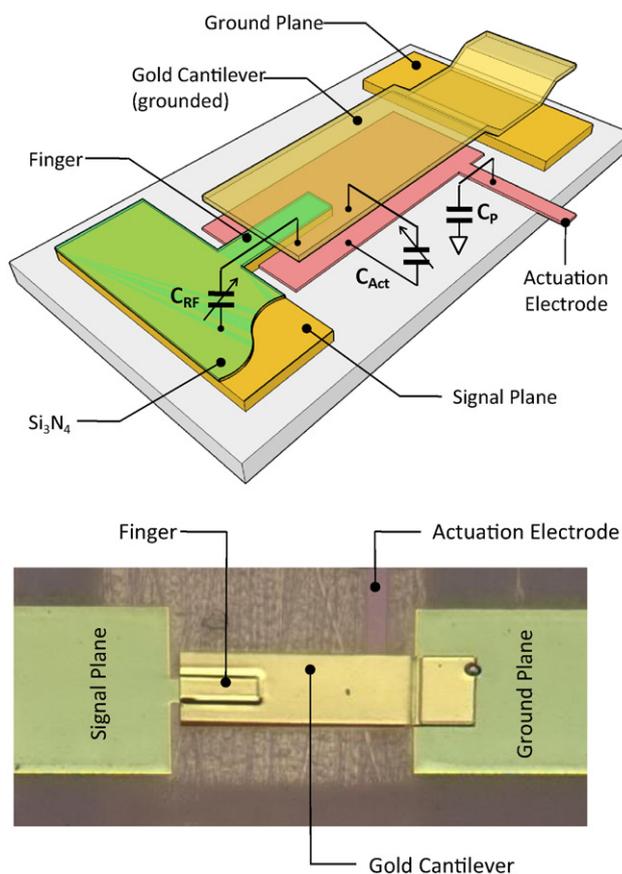


Fig. 1. Architecture of the MEMS RF switch: 3D artist view (top) and photograph (bottom).

avoid RF leakage within the cell, the material used for the actuation bottom electrode (polysilicon) is kept voluntarily resistive in this application.

### 2.2. Electrostatic actuator modeling

The purpose of the modeling is to allow simulations in the microelectronic design environment in order to study various design options for the driver and the diagnosis circuitries. High-level modeling is therefore preferred, as long as all first-order phenomena are well represented. The dynamic model introduced here is based on analytical description of the device in two physical domains: mechanical and electrical, including the electromechanical coupling related to electrostatic forces.

The major constraint for the design of a smart driver with diagnosis capabilities is to preserve the integrity of the RF path. For this reason, it was assumed that no measurement can be performed on the RF signal plane (e.g.  $C_{\text{RF}}$  cannot be measured directly). For this reason, the RF part of the switch is left apart from the modeling presented here. According to Fig. 2, actuator modeling is based on a spring-mass-damper system (kMD), translating along the vertical axis. The mass displacement  $z$  is controlled by an electrostatic actuator made of two parallel plates of surface  $S_A$ , separated by an initial gap  $g_0$ . Assuming that the bottom electrode is covered by a dielectric layer of thickness  $t_{\text{ox}}$  and of relative permittivity  $\epsilon_r$ , the resulting capacitance between the two electrodes is given by:

$$C_{\text{Act}} = \frac{\epsilon_0 S_A}{g_{\text{eff}}} \quad (1)$$

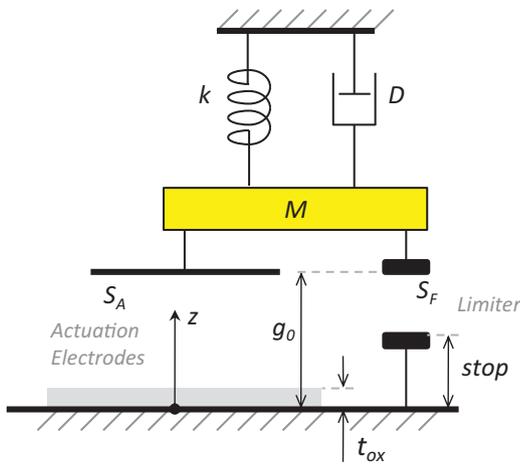


Fig. 2. Mechanical representation of an electrostatic actuator model with main parameters.

where  $g_{eff}$  is the effective gap calculated by taking into account the two serial capacitances:

$$g_{eff} = z - t_{ox} + \frac{t_{ox}}{\epsilon_r} \quad (2)$$

The cantilever beam movement is practically hard-limited by the RF finger. In order to avoid convergence troubles within Spectre® a damping effect is modeled into the limiter block. This

somehow makes the landing of the beam onto the finger surface smoother. The action of the limiter  $F_L$  is therefore established depending on the switch position  $z$  and velocity  $\dot{z}$ . As long as the moving part stays far from the finger surface, the limiter is disabled. Within a short range above the finger surface, the limiter acts in force–source mode and the damping effect is modeled by an additional damping force given by:

$$F_L = \alpha \left( \frac{\eta S_F}{z - stop} \right) \dot{z} \quad (3)$$

where  $\eta$  represents the air viscosity in Pa s,  $S_F$  is the overlap surface between the bridge and the finger and  $\alpha$  an exaggeration factor (set to 1 by default). If the conditions  $z \approx stop$  and  $\dot{z} \approx 0$  are reached, the limiter switches to position–source mode and holds the bridge at  $z = stop$  as long as the electrostatic actuator maintains the cantilever down.

Fig. 3 shows the straightforward implementation of this model under Cadence®. Each part of the model is described using the proprietary Verilog-A language. The discipline kinematic is used to represent the  $z$  node. Using this discipline, the “across” quantity (same as voltage) represent the vertical position of the bridge, while the “through” quantity (same as current) represents the forces. Forces equilibrium on node  $z$  is therefore a direct application of Kirchhoff’s circuit laws.

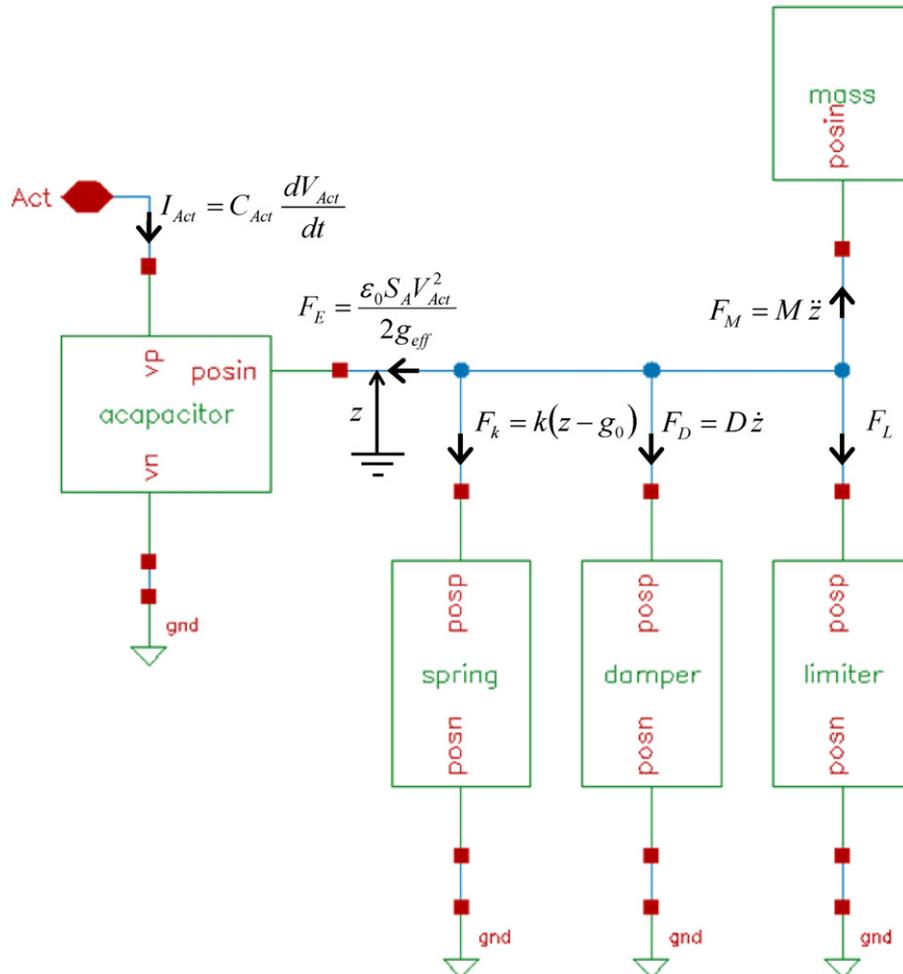


Fig. 3. Behavioral representation of the electrostatic actuator model implemented within Cadence® for system-level “electrical” simulations.

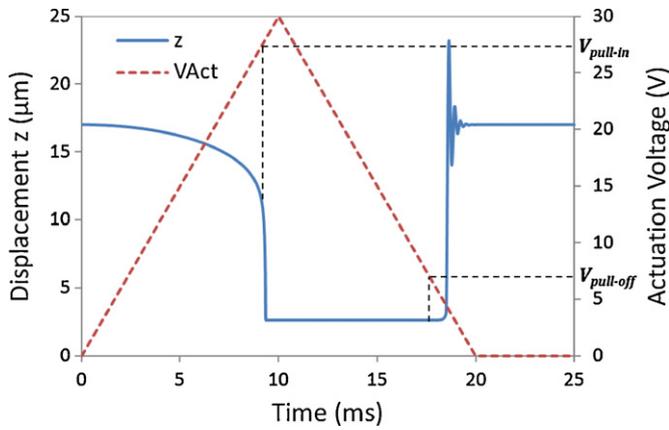


Fig. 4. Transient simulation of the switch actuation (pull-in and pull-off) to validate the model behavior.

2.3. Electrostatic actuator simulations

Simulations were carried out using a realistic set of parameters summarized in Table 1. The initial gap of  $d_0 = 17 \mu\text{m}$  is estimated after characterization of the bridge profile which bends upward after fabrication due to non-controlled residual stress. Other parameters are either estimated from prototypes or taken from the literature.

The result of the transient simulation in Fig. 4 shows that the behavior of the electrostatic actuator is well represented. The pull-in voltage is found around 27 V which is in perfect accordance with the theory (with  $z = d_0$ ):

$$V_{\text{pull-in}} = \sqrt{\frac{8kg_{\text{eff}}^3}{27\epsilon_0 S_A}} = 26.8 \text{ V} \tag{4}$$

When the switch is closed, the spring applies a constant restoring force that can be easily calculated as  $F_k = 0.5(17 - 2.65)10^{-6} = 7.175 \mu\text{N}$ . So that pull-off occurs for:

$$V_{\text{pull-off}} = \sqrt{\frac{2F_k g_{\text{eff}}^2}{\epsilon_0 S_A}} = 7.65 \text{ V} \tag{5}$$

This value is also consistent with the transient time simulations of Fig. 4.

Fig. 5 illustrates the transient response of the switch to an actuation pulse. In this simulation, the actuation driver is modeled by an ideal voltage source connected to the switch through a RC network that represents the electrical path in terms of serial resistance  $R_{\text{ser}}$  and parasitic capacitor  $C_{\text{par}}$ . The displacement  $z$  is plotted together with the current  $I_{\text{Act}}$  delivered by the source. It is worth noting that this simulation corresponds to a slow actuator due to the high level of damping. As a consequence, the electrical time constant is

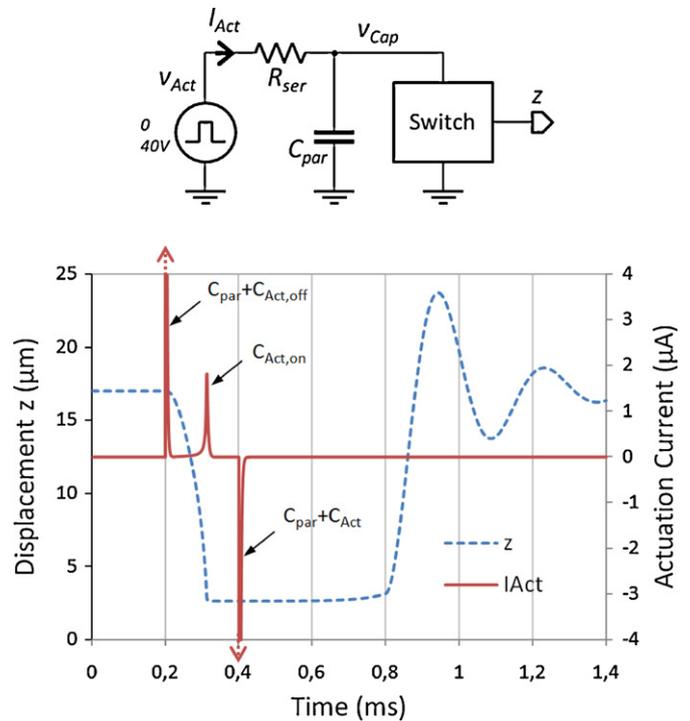


Fig. 5. Transient response of the switch to an actuation pulse and associated driving current.

small compared to the mechanical one. When the driver is turned on ( $t = 200 \mu\text{s}$ ), the transient current exhibits a first peak corresponding to the charge of both parasitic and actuation capacitances ( $C_{\text{par}} + C_{\text{Act,off}}$ ) during few microseconds. The mechanical switching occurs a hundred microseconds later and implies a fast increase of  $C_{\text{Act}}$  ( $t \approx 300 \mu\text{s}$ ) that produces a second current peak corresponding to the need for additional charges (as  $C_{\text{Act,on}}$  is larger than  $C_{\text{Act,off}}$ ). When the driver is turned off ( $t = 400 \mu\text{s}$ ), both capacitances are quickly discharged. When the pull-off occurs,  $300 \mu\text{s}$  later, the voltage across the capacitors is already null as well as the total charge of the capacitance and no further effect on the transient current is observed.

As a short conclusion for this part, a compact model of the switch has been developed which allows simulations of driving circuitry at transistor level within a microelectronic design environment. A non-invasive way (from the RF point of view) to get a feedback on the switch action is to monitor the actuation current when the driving signal is applied. The next section addresses in detail the design of an integrated High-Voltage driver with focus on the diagnosis issues.

Table 1 Electrostatic actuator model parameters.

Cell	Symbol	Quantity	Value
acapacitor	$S_A$	Actuation electrode surface	$100 \times 10^{-9} \text{ m}^2$
	$\epsilon_0$	Abs. permittivity	$8.85 \times 10^{-12} \text{ F m}^{-1}$
	$\epsilon_r$	Bottom dielectric relative permittivity	3.9
spring	$t_{\text{ox}}$	Bottom dielectric thickness	$0.3 \mu\text{m}$
	$k$	Spring constant	$0.5 \text{ N m}^{-1}$
	$d_0$	Initial gap	$17 \mu\text{m}$
mass	$M$	Mass	$1 \times 10^{-10} \text{ kg}$
damper	$D$	Damping factor	$5 \times 10^{-6} \text{ N m}^{-1} \text{ s}^2$
	$s_{\text{flayer}}$	Gap for damping action	$0.5 \mu\text{m}$
limiter	$\eta$	Air viscosity	$18 \times 10^{-6} \text{ Pas s}$
	$S_F$	Finger overlap surface	$25 \times 10^{-9} \text{ m}^2$
	Stop	Finger height	$2.65 \mu\text{m}$

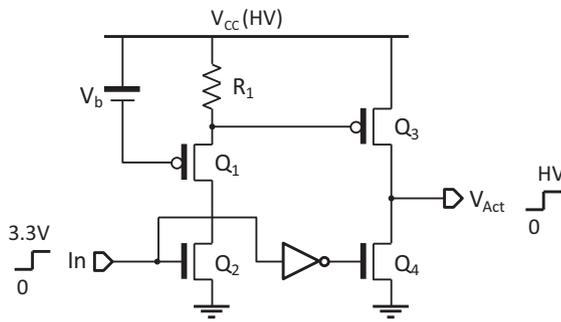


Fig. 6. Schematic of the basic HV driver architecture.

### 3. Smart driver design

The primary function of the driver is to provide the actuation voltage  $V_{Act}$  that is close to 46 V in our case. For this, the High-Voltage (HV) 0.35  $\mu\text{m}$  CMOS technology (h34b4c3) from Austria MicroSystems (AMS) was chosen to develop the integration of such drivers in the context of a multiple channels chip. This technology tolerates drain-source voltage drop across transistor channels ( $V_{DS}$ ) up to 50 V. The design of a basic driver stage is first addressed. Then, two approaches are proposed to upgrade the driving circuitry with a diagnosis capability.

#### 3.1. High-voltage driver

The challenge when designing a HV driver is to combine the low voltage level of the control circuitry (3.3 V in a 0.35  $\mu\text{m}$  CMOS process) with the high output voltages (50 V in our case). In this study, it was assumed that two independent power supplies were available: a logical one (3.3 V) and a HV one (that may vary from 20 V to 50 V to adapt various pull-in conditions).

A common practice for the design of a HV driver is to build a common-source stage with a single HV NMOS device and a pull-up resistor tied to the HV supply. The transistor gate is in that case simply driven by a low-voltage signal. When the output is 0, this architecture suffers from static power consumption which is not acceptable in embedded applications. An alternative is then to use a CMOS driver preceded by a level-shifter to drive the HV PMOS transistor. Plenty of level shifter architecture can be found in literature. Among them, a classical structure is presented in [13]. In theory, it consumes no static power if the needed bias voltages are not taken into account. However, the structure is based on a bi-stable principle which lacks of robustness and the leakage current can cause non-negligible current consumption. For this reason a simpler but also more robust structure has been preferred. The circuit shown in Fig. 6 is inspired from [14]. The pair of HV transistors  $Q_3$  and  $Q_4$  forms the complementary output driving stage. In this configuration, the gate of  $Q_4$  can be directly driven by logical levels (0–3.3 V). The gate of  $Q_3$  must be driven between  $V_{CC}$  and a lower voltage that turns  $Q_3$  on, while keeping the magnitude of  $V_{GS,3}$  within 20 V which is a technological constraint. This condition is ensured by the level-shifter stage made of  $Q_1$ ,  $Q_2$  and  $V_b$ . When input is 0,  $Q_2$  is off. There is no current flowing in the level-shifter and  $V_{GS,3}$  is 0. When input is 3.3 V,  $Q_2$  is turned on. The current flowing in the level shifter is regulated by the voltage drop across  $R_1$  so that  $V_{GS,1} \approx -V_{t,p} \approx -1.7$  V. The voltage drop  $V_b$  is designed to be about 10 V (50% of the 20 V limit). It is implemented by a set of diode-mounted transistors in series, biased by a resistive load tied to the ground. This ensures that  $V_b$  stays constant for a wide range of supply voltage. It finally comes that the voltage on the gate of  $Q_3$  in on-state is close to  $V_{CC} - V_b + V_{t,p} \approx 41.7$  V. Note that the static consumption of the driver is here mainly determined by

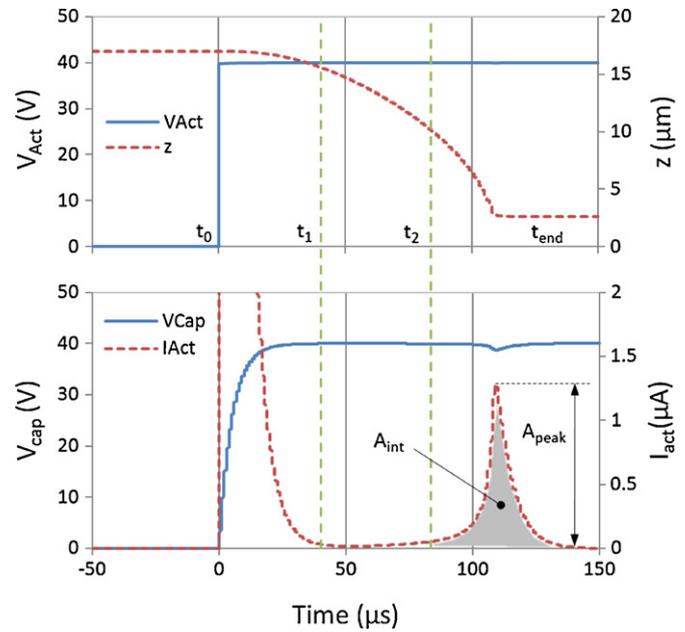


Fig. 7. HV driver and MEMS transient simulation of an actuation event.

$R_1$  whose value is practically restricted by its cost in term of silicon area.

#### 3.2. Proposed diagnosis circuits

Fig. 7 details transient signals related to an actuation event. It is obtained by the simulation of the HV driver previously described and modeled at transistor level together with the switch model and a RC network ( $R_{ser} = 1$  M $\Omega$  and  $C_{par} = 5$  pF) representing a realistic case of routing parameters. As mentioned before, the diagnosis approach must not interfere with the RF path. Fortunately, the switch pull-in produces a distinctive actuation current profile which is a good start for an investigation.

The driver output is turned on at  $t_0 = 0$ , providing instant rapid and stable 40 V voltage for  $V_{Act}$ . As mentioned above, the first current peak that is observed corresponds to the charge through  $R_{ser}$  of the total capacitance  $C_{par} + C_{Act,off}$ . The charge is almost completed when  $V_{Cap}$  reaches its final value of 40 V ( $t_1 \approx 30$   $\mu\text{s}$ ). At that time the beam is still in the up position. At  $t_2 = 75$   $\mu\text{s}$ , the cantilever gets close to its lower position producing a fast increase of  $C_{Act}$ . This causes a small current peak corresponding to the charge of  $\Delta C_{Act} = C_{Act,on} - C_{Act,off}$ . Note that during this charge, the  $V_{Cap}$  voltage exhibits a small notch that can be neglected. Finally, all signals become stable after  $t_{end} = 150$   $\mu\text{s}$ .

Since the second current peak will not occur in the case of broken or stuck MEMS, it makes sense to develop a diagnostic strategy based on the measure of the actuation current. A first idea would be the simple measure of the amplitude of the second current peak ( $A_{peak}$ ). This approach is not recommended since the peak amplitude strongly depends on the routing parameters ( $R_{ser}$ ,  $C_{par}$ ) that may vary in a significant range. This is confirmed by the simulation results shown in Fig. 8a, where  $A_{peak}$  is reported for various combinations parameters  $R_{ser}$  and  $C_{par}$ . On the contrary, the amount of charges transferred to the electrostatic actuator when  $C_{Act}$  changes from  $C_{Act,off}$  to  $C_{Act,on}$  is relatively independent of routing parameters. Fig. 8b shows that the current integral ( $A_{int}$ ) measured within the time window corresponding to the second current peak only varies by less of 4% for the same routing parameters range. As a consequence, a diagnostic approach based on the actuation current integration seems more appropriate.

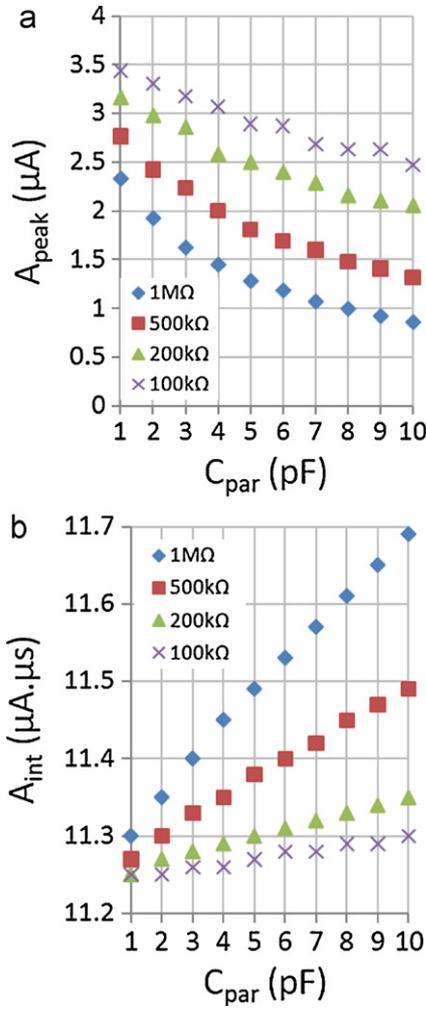


Fig. 8. Sensitivity of  $A_{peak}$  (a) and  $A_{int}$  (b) to routing parameters.

The total amount of charges stored in  $C_{par}$  and  $C_{Act}$  during the whole actuation process does not depend on  $R_{ser}$  and writes:

$$q = V_{Act}(t)(C_{par} + C_{Act}(t)) \quad (6)$$

Looking at the actuation current, we have:

$$i_{Act}(t) = \frac{dq(t)}{dt} \quad (7)$$

$$i_{Act}(t) = (C_{par} + C_{Act}(t)) \frac{\partial(V_{Act}(t))}{\partial t} + V_{Act}(t) \frac{\partial(C_{Act}(t))}{\partial t}$$

The second current spike is caused by the second term in Eq. (7), when the actuation voltage is constant and the actuation capacitance changes. As the actuation voltage is assumed to be constant between  $t_2$  and  $t_{end}$ , the integration of the actuation current during this period becomes:

$$A_{int} = \int_{t_2}^{t_{end}} V_{Act,end} \frac{d(C_{Act}(t))}{dt} dt = V_{Act,end} \Delta C_{Act} \quad (8)$$

with

$$\Delta C_{Act} = C_{Act,end} - C_{Act,0} = C_{Act,on} - C_{Act,off}$$

Eq. (8) clearly demonstrates that the total charge corresponding to the actuation current during the second spike does not depend on the parasitic capacitance. However, it is valid only if the two spikes are well separated in time. This implies that the duration of the first spike (related to  $R_{ser} \times C_{par}$ ) should be smaller than the time response of the switch.

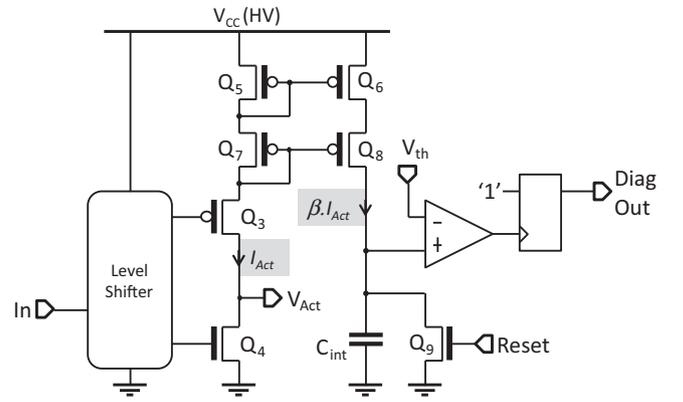


Fig. 9. Structure of the HV driver with actuation current integrator.

### 3.3. Smart-driver architecture #1

A first version of the HV driver with diagnosis is depicted in Fig. 9. In this circuit, the actuation current is mirrored into a capacitor  $C_{int}$  so that the voltage across  $C_{int}$  represents the integral of the current  $I_{Act}$ . A cascode current mirror configuration, with a copy ratio  $= W_{Q_6, Q_8} / W_{Q_5, Q_7}$ , has been preferred to improve the  $V_{DS}$  matching of the pair  $Q_5/Q_6$  and thus to guaranty a better accuracy of the copy. Transistor  $Q_9$  is used to reset the integrator state and then start the integration process on a falling edge of the Reset control input. Note that the gate of  $Q_9$  is associated with dummy transistors (not represented) to minimize integration errors due to charge injection.

If the voltage across  $C_{int}$  reaches a specific threshold voltage  $V_{th}$ , a '1' is stored in the latch meaning a successful commutation of the switch, otherwise the diagnosis output is '0'. The independent control of the Reset pin allows the integration process to start anytime.

Two strategies can be investigated here: If the MEMS mechanical time constant is small, or uncertain, the integration may start from  $t_0$ . In that case, the total actuation current is summed up in the integrator. On the other hand, if the MEMS time constant is well characterized, the integration may start from  $t_2$  so that only the current associated with the pull-in event is accumulated. Obviously, the second method, when possible, will produce a better result. Let us study both.

Fig. 10 shows the transient voltage across  $C_{int}$  obtained by simulation of the Smart-driver in the same condition as before ( $C_{par} = 5$  pF,  $V_{Act} = 40$  V). Integration starts here at  $t_0$ . From a quali-

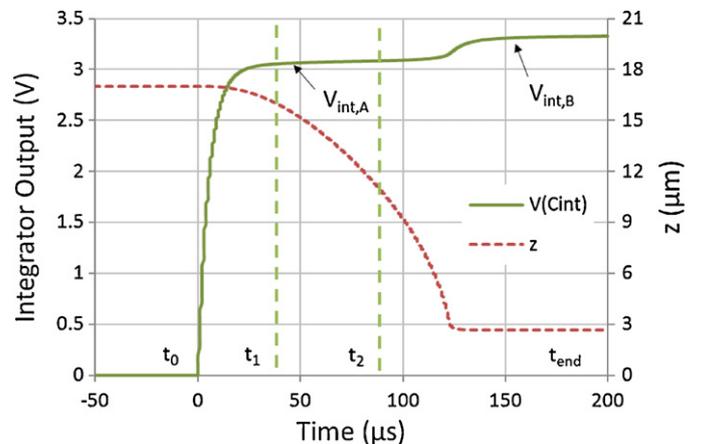


Fig. 10. Transient simulation of the smart-driver and diagnosis circuitry with working MEMS switch.

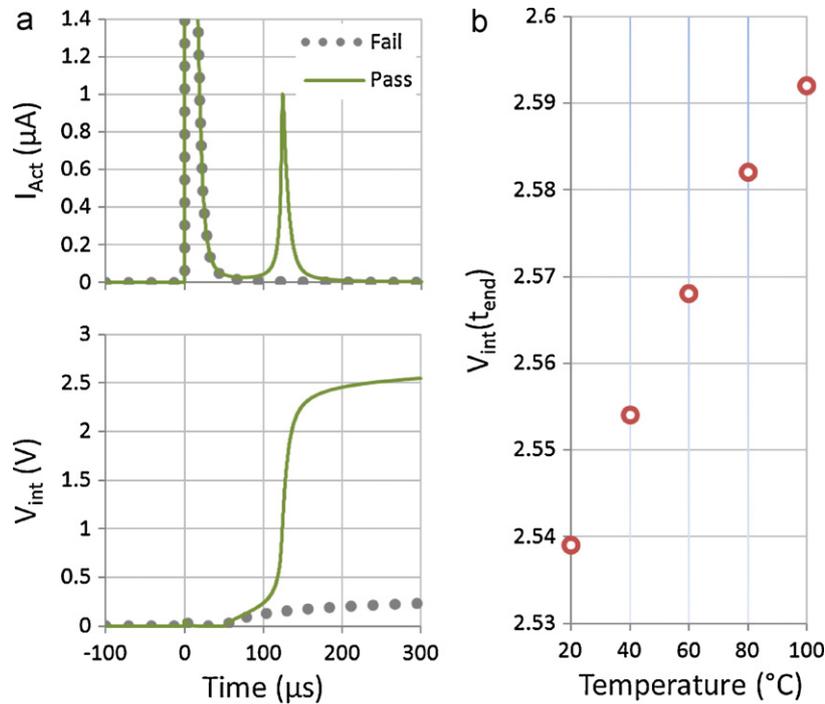


Fig. 11. Diagnosis output for integration time starting at  $t_2$ , with working and stuck MEMS (a) and effect of temperature (b).

tative point of view, one can see the two independent integration steps corresponding to the charge of  $C_{par}$  and  $\Delta C_{Act}$  respectively.

The design parameters for the integrator are the value of  $C_{int}$  and the copy ratio  $\beta$  of the current mirror. If the integration begins at  $t_0$ , the parameters must be designed accordingly to an expected maximum value of the routing capacitance  $C_{par}$ , given that the integrator output after  $t_1$  must not saturate the comparator which is supplied by the low-voltage and leave room for the further integration of the  $\Delta C_{Act}$  charging current. The integrator level after  $t_1$  is given by:

$$V_{int,A} = \frac{\beta}{C_{int}} \int_{t_0}^{t_1} i_{Act} dt = \frac{\beta}{C_{int}} V'_{Act} (C_{par} + C_{Act,off}) \quad (9)$$

with

$$V'_{Act} = V_{Act} - 2V_{tp} \approx V_{CC,HV} - 3.4V \quad \text{and} \quad C_{Act,off} \ll C_{par}$$

In the previous simulation, the ratio  $\beta$  is 1:6 and  $C_{int}$  is 10 pF. With the maximum expected value for  $C_{par}$  of 5 pF, the theoretical output voltage after  $t_1$  is 3.05 V, as confirmed by simulation, very close to the comparator supply voltage.

The charging  $\Delta C_{Act}$  brings the integrator output to the voltage at  $t_{end}$ :

$$V_{int,B} = V_{int,A} + \frac{\beta}{C_{int}} V'_{Act} \Delta C_{Act} \quad (10)$$

Assuming  $\Delta C_{Act} \approx 400$  fF, the voltage  $V_{int,B}$  is 244 mV above  $V_{int,A}$ . This is also verified in simulation.

Since this diagnosis approach is based on the comparison of the absolute voltage of the integrator output, the absolute uncertainty on parasitic capacitance value  $C_{par}$  must be well below  $\Delta C_{Act}$ . Beside, other uncertainties such as the comparator offset may only be addressed by an individual calibration of each driver channel, that would determines a value for the threshold  $V_{th}$ .

Taking advantage of the MEMS time constant by starting the integration after the charge of  $C_{par}$  will bring a clear improvement on the diagnosis efficiency. Integrator parameters  $\beta$  and  $C_{int}$  are then adjusted to best fit the comparator input dynamic. Using  $\beta = 1:3$  and  $C_{int} = 2$  pF, the expected value of  $V_{int}$  after the integration

time is 2.44 V. Note that decreasing the value of  $C_{int}$  too much would increase charge injection effects from gate  $Q_9$  and is therefore not recommended.

Fig. 11 shows the simulation results obtained by starting the integration process at  $t_0 + 50 \mu s$ . The “Pass” response is obtained using the MEMS switch model, while the “Fail” response corresponds to the simulation of a broken switch ( $C_{Act} = 0$ ). The  $C_{int}$  voltage reaches 2.53 V when the pull-in occurs and is 10 times less (220 mV) otherwise. The plot on the right confirms that the architecture is intrinsically not sensitive to temperature effects. A variation of only 2% off the integration result is observed on a 20–100 °C temperature range. Note that the switch model does not include temperature effects at that time.

As it has been demonstrated earlier, the amount of current charging  $C_{Act}$  also poorly depends on the routing parameters  $R_{ser}$  and  $C_{par}$ . In consequence, a diagnosis approach based on the delayed integration of the actuation current is a potentially robust way to achieve the pull-in event detection without the requirement of calibration.

The method introduced above requires the good knowledge of the switch dynamic behavior, which must feature a slow-enough, predictable and stable time response to isolate the pull-in event from the charge of the parasitic capacitance. If these conditions are not met, an alternative approach to eliminate the effects of the routing parameters is proposed in the following.

#### 3.4. Smart-driver architecture #2

An alternative to cancel the effect of the parasitic capacitance  $C_{par}$  during the switch actuation is proposed with the driver architecture presented in Fig. 12. The measurement sequence start with an initialization of the charge in  $C_{int}$  by turning on both  $Q_{9a}$  and  $Q_{9b}$  so that  $V_{Cint} = V_{ref}$ . During phase #1,  $V_{CC}$  is set to provide only half of the final actuation voltage  $V_{Act}$  at the driver output,  $Q_{9b}$  is turned off and the driver is activated ( $In = '1'$ ). The actuation current is summed up in  $C_{int}$ . After the integration time, and assuming that the driver output is below the pull-in voltage the voltage,  $V_{int,B}$  is

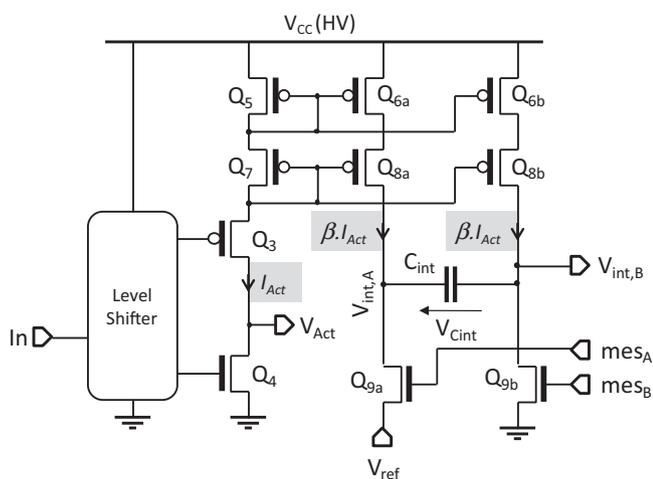


Fig. 12. Schematic of the HV driver with differential integrator of the actuation current.

given by:

$$V_{int,B} = \frac{\beta}{C_{int}} \frac{V_{Act}}{2} (C_{par} + C_{Act,off}) \quad (11)$$

During phase #2, the transistor Q<sub>9a</sub> is turned off, and Q<sub>9b</sub> is closed to connect the node V<sub>int,B</sub> to ground. At this moment, the voltage V<sub>int,A</sub> is:

$$V_{int,A} = V_{ref} - V_{int,B} \quad (12)$$

V<sub>CC</sub> is now adjusted to make the driver outputs V<sub>Act</sub> so that another V<sub>Act</sub>/2 voltage step is applied on the switch. The pull-in occurs and then after another integration period, V<sub>int,A</sub> becomes:

$$V_{int,A} = (V_{ref} - V_{int,B}) + \frac{\beta}{C_{int}} \frac{V_{Act}}{2} (C_{par} + C_{Act,on}) \quad (13)$$

$$V_{int,A} = V_{ref} + \frac{\beta}{C_{int}} \frac{V_{Act}}{2} \Delta C_{Act}$$

In summary, the amount of current charging C<sub>par</sub> is summed up in C<sub>int</sub> during the first V<sub>Act</sub>/2 step, and then subtracted during the second V<sub>Act</sub>/2 step, leaving the integrator output with an image of the ΔC<sub>Act</sub> charge only. The complete sequence shown in Fig. 13 has been obtained with only the parasitic capacitance connected to the driver. Because ΔC<sub>Act</sub> = 0 in this case, the diagnosis output (V<sub>int,A</sub>) is V<sub>ref</sub> at the end. The simulation is performed with R<sub>ser</sub> = 1 MΩ, C<sub>par</sub> = 10 pF, β = 1:16 and C<sub>int</sub> = 15 pF. With V<sub>CC</sub> = 40 V, the actuation voltage is roughly V<sub>Act</sub> = 37.2 V. According to Eq. (11),

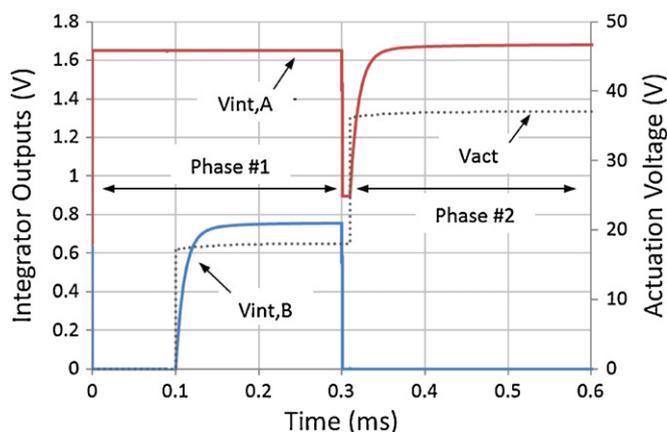


Fig. 13. Simulation of the HV driver “differential diagnosis” sequence without switch connected.

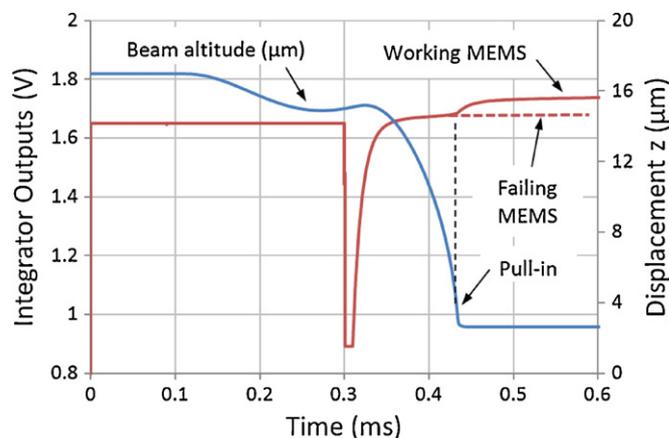


Fig. 14. Simulation of the HV driver “differential diagnosis” sequence with working MEMS switch.

the voltage V<sub>int,B</sub> after phase #1 reaches 775 mV, which is verified by the simulation.

In Fig. 14, the simulation is performed with an electrostatic switch connected to the driver. The change in capacitance during the pull-in produces an increase of V<sub>int,A</sub> of about 60 mV. The robustness of the approach against routing parameters has been investigated with results reported in Fig. 15. It appears that for each case, the diagnosis circuitry produces a result with working MEMS well distinguishable from the one obtained with a broken switch. Note that the result strongly depends on the ability to set the correct V<sub>CC</sub> that produce a precise V<sub>Act</sub>/2. In this simulation, this V<sub>CC</sub> is set manually to 21 V. Practically, this half-supply voltage can be generated on-chip within a dedicated circuit that will address process variations and better separation between working and failing case is then expected.

#### 4. Experimental results

A test chip including 16 drivers of architecture #1 and 1 driver of architecture #2 has been fabricated using a HV 0.35 μm CMOS technology from Austria Microsystems. This chip has been connected to surface mounted capacitors (in a first board) and MEMS switches (on a second board). In both cases, direct bonding between CMOS dies and PCB has been used to minimize parasitic capacitance. Fig. 16 illustrates these boards with closed-up views of the CMOS die and of the MEMS RF switch.

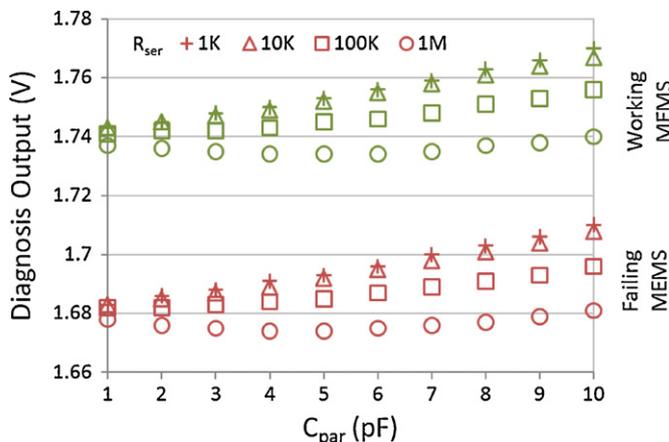
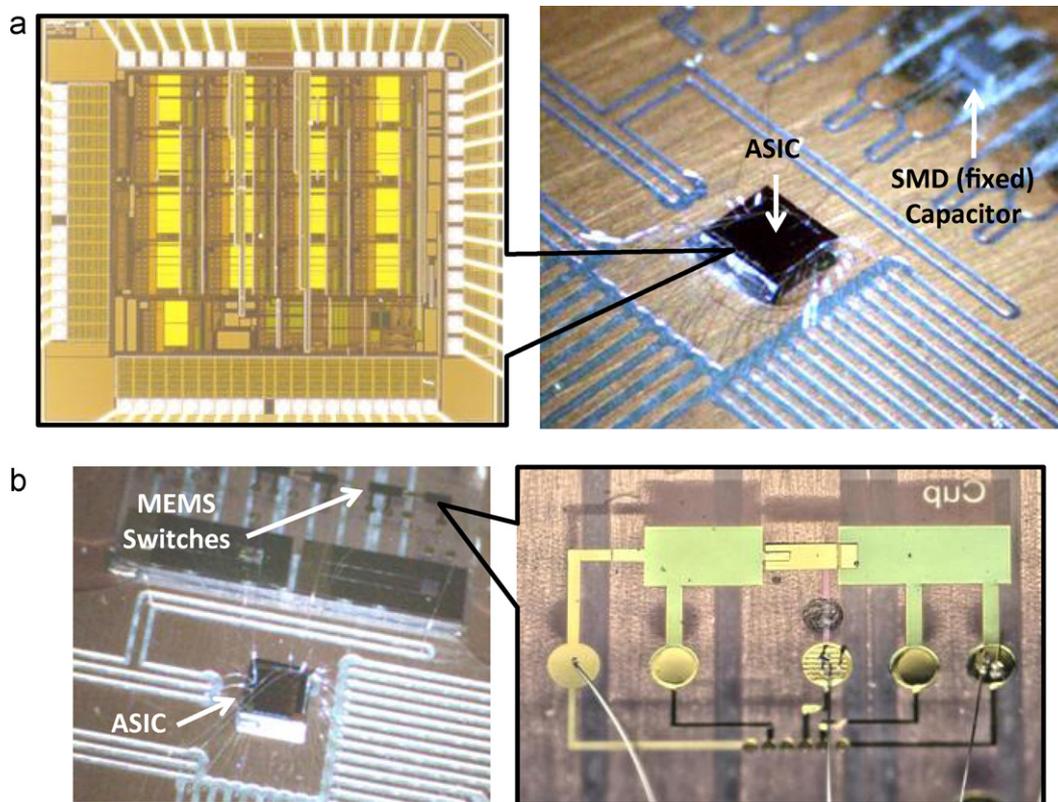


Fig. 15. Diagnosis output for different routing parameters (R<sub>ser</sub>, C<sub>par</sub>) with working and non-working MEMS.



**Fig. 16.** Two experimental boards are used for characterization. One (a) with the ASIC connected to fixed capacitance (SMD Capacitors) and the other (b) with the ASIC directly bonded to MEMS switches.

#### 4.1. Sensitivity to parasitic capacitance

We have first used the smart drivers connected to various fixed value capacitors used to emulate different magnitudes of parasitic.

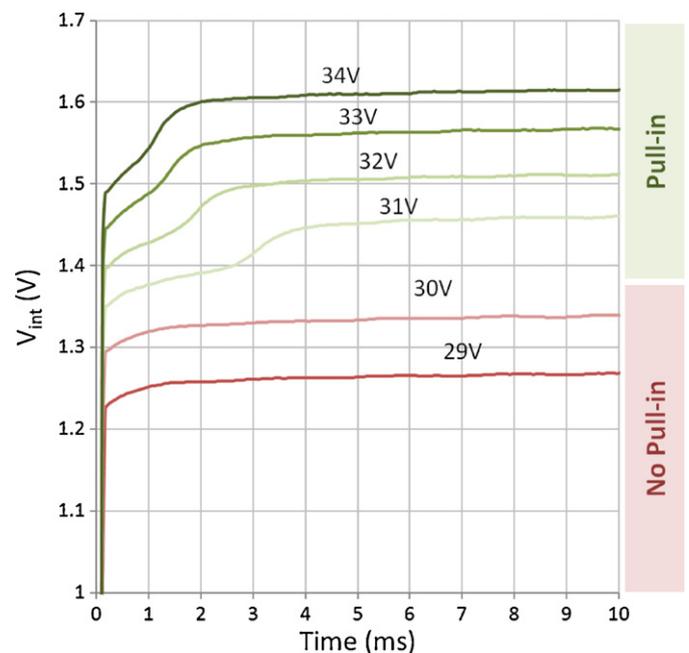
Regarding smart driver #1, an important parameter is the start time of the integration. If the integration starts at the same time than the actuation command, then the output saturates, due to the initial value of the current, whatever the parasitic capacitance is. This is due to the internal parasitic of the chip that are far above the minimum value to saturate. As mentioned in Section 3.3 and illustrated in Fig. 11, the best rejection of the parasitic capacitance is obtained for an integration start time delayed 50  $\mu\text{s}$  after the step command is applied. In that case, the sensitivity to parasitic capacitance is not measurable due to its negligible value. It is worth noting that this sensitivity is also strongly dependent on the actual value of the parasitic capacitance thus making the determination of the optimum delay very difficult. Finally, the delay must be set sufficiently high to reduce sensitivity to parasitic but sufficient low to start integration before the mechanical part reacts.

Regarding smart driver #2, this sensitivity is due to internal mismatches of the driver and does not depend on the parasitic capacitance in a reasonable range of study. This sensitivity has been characterized to 3.6 mV/pF, which is low enough to consider that the effect of  $C_{\text{par}}$  is correctly rejected.

#### 4.2. Diagnosis ability

We have first studied the transient response of the diagnosis cell analog output ( $V_{\text{int}}$ ) using various supply voltages (and therefore various actuation voltages for the switches) for smart driver #1 (Fig. 17). The delay before starting the integration process has been set to 50  $\mu\text{s}$  to prevent the integrator from saturation while keeping the two integration steps visible. As a consequence, only a part of

the parasitic capacitance ( $\propto C_{\text{par}}$ ) is represented in the output voltage. For lower values (below 30 V) the voltage is not high enough to actuate the switch. Without pull-in event, the diagnosis output only represent the amount of charge transferred to  $C_{\text{par}} + C_{\text{Act,off}}$  which obviously increases with the actuation voltage. For voltages over 30 V, the pull-in occurs and the second integration step shows up as



**Fig. 17.** Experimental output of the diagnosis cell ( $V_{\text{int}}$ ) for various supply voltages (architecture #1).

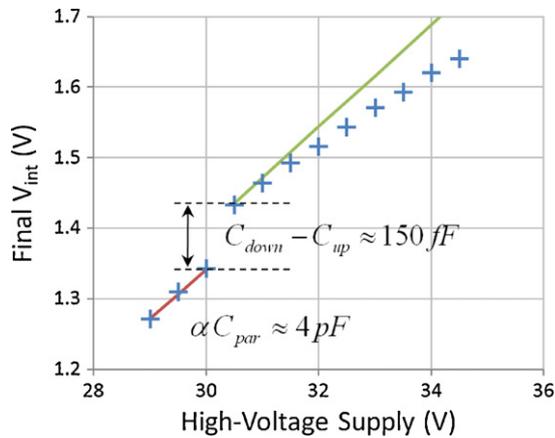


Fig. 18. Evaluation of  $\alpha C_{par}$  and  $\Delta C_{Act}$  from previous data.

expected. In our application, only a “go/no-go” output is required. It is worth noting however that the diagnosis output contains much more information regarding the behavior of the MEMS. One can observe for instance that when the applied voltage increases, the pull-in event comes earlier and faster. Information regarding the dynamic behavior of the switch can therefore be extracted from this response.

The final value of the integrator output is plotted as a function of the driving voltage in Fig. 18. From the first points (HV supply not sufficient to reach pull-in voltage), one can estimate the contribution of  $C_{par}$  around 4 pF. Then, the step in the integrator output when pull-in occurs corresponds to a change in capacitance of about 150 fF, which is smaller than expected (according to the model established earlier). For a simple “go/no-go” test however, the diagnosis cell provide enough information to produce the expected answer.

Fig. 19 reports the output of the diagnosis circuit during a MEMS actuation for smart driver #2. Qualitatively, the waveform is very similar to the one obtained by simulation (Fig. 14). An additional 25 mV is brought across the integrator capacitor ( $C_{int}$ ) during pull-in, corresponding to a 260 fF change in the MEMS actuator capacitance.

Due to the method used to evaluate the capacitance change (Fig. 18), the value obtained with smart driver #1 is under evaluated as it corresponds to the difference of capacitance between two stable states just before and just after pull-in corresponding to a 1 V step of actuation voltage. At the contrary, the differential method evaluates a difference of capacitance due to a voltage step close to 25 V (half the HV supply voltage).

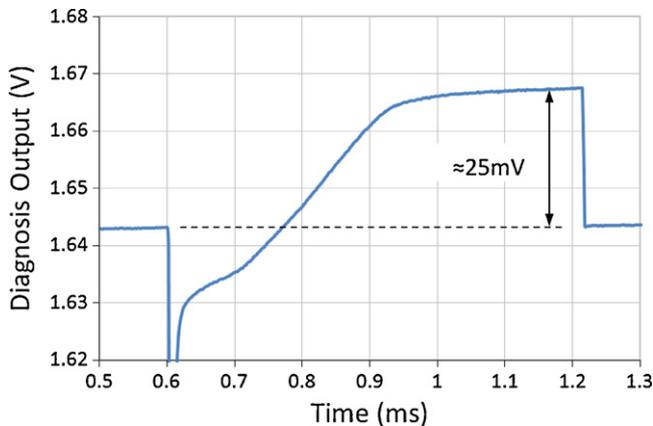


Fig. 19. Measured diagnosis output voltage with a MEMS switch (architecture #2).

Table 2  
Main characteristics of the proposed drivers.

	Smart driver #1	Smart driver #2
Maximal supply voltage (VDD_HV)	50 V	50 V
Maximal output voltage Surface	VDD_HV – 3 V 0.145 mm <sup>2</sup>	VDD_HV – 3 V 0.35 mm <sup>2</sup>
Static power consumption (no commutation)	0.036 mW	10 mW
Sensitivity to $C_{par}$	Very low after calibration	3.6 mV/pF
Sensitivity to $\Delta C$	533 mV/pF	96 mV/pF
Resistance output	1 M $\Omega$	1 M $\Omega$
Diagnostic type	Integration of the actuation current after a delay	Difference of the integrated actuation current between two phases

4.3. Discussion

Both drivers demonstrated their ability to actuate MEMS RF switches and main characteristics are recalled in Table 2. It is difficult to conclude between both drivers but assuming that the delay before starting the integration can be adjusted to cope with the actual parasitic capacitance and to the mechanical time constant, smart driver #1 would be preferred as it allows a better rejection of the parasitic capacitance, lower power consumption and a smaller silicon area per channel.

5. Conclusion

In this paper, we have presented two fully integrated smart HV drivers dedicated to electrostatic capacitive actuators. These drivers are, similarly to other state-of-the-art solutions, able to generate required bias to reach pull-in voltages but this is the first time, to our knowledge, that diagnosis capabilities are integrated on the same CMOS die than the driver. Moreover, each channel occupies a reduced silicon area thus allowing the control of systems with a large number of independent RF MEMS switches.

Diagnosis is based on the measurement of the actuation current which exhibits a peak when the pull-in event occurs. Two approaches have been investigated. The first one is based on a simple integration of the actuation current. In the case of “slow” switches, this method is efficient since it is possible to cancel the effect of parasitic capacitance by choosing properly the integration starting point. For “fast” MEMS, a differential measurement technique has been proposed. It cancels the effect of serial resistance and parallel parasitic capacitance by using a two-steps actuation voltage.

Design of both smart drivers has been validated by simulation thanks to a behavioral model of the electrostatic actuator. This model is simple but efficient because he renders the fast change of capacitance and solves the traditional convergence problem of such highly non-linear mechanical systems. Both solutions have been prototyped on CMOS and experimentally validated with a real RF MEMS switch.

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