Digital Test Method for Embedded Converters with Unknown-Phase Harmonics

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***Abstract* — This paper presents an extension of the ANC ("Analogue Network of Converters")-based method, which is an original Design-for-Test (DfT) technique associated to a dedicated test algorithm to characterize the harmonic components of a set of embedded converters using only digital test resources. The ANC-based method was primarily developed under the assumption that the harmonics' phase is proportional to the input phase. This assumption is not valid for all converter architectures, where filtering effects may affect the harmonics' phase. The improved ANC-based method is able to calculate the magnitude of the harmonic components with unknown phase. The fundamental principle of this improved version of the ANC-based method is the same, but further mathematical developments have been established using a model independent from the harmonics' phase. The simulation results and the experiments show an excellent agreement between the values measured using the method and the values measured with a usual test setup, for the THD and SFDR parameters. Simulations were carried out considering both random phases and realistic phase delays such as the ones induced by a low pass filter.**

Keywords: converter testing, harmonic characterization, unknown-phase harmonics, Design-for-Test

1. INTRODUCTION

The popularity of portable data and communication applications like smart phones, laptops, or MP3/MP4 players is currently the wellspring for integration of many different functions into a single package. Systems-in-Package (SiPs) or Systems-On-Chip (SOCs) that integrate very different analogue or mixed-signal blocks have been developed toward this aim. Although they offer clear benefits such as extreme miniaturization or connection length reduction, they imply in compensation very significant test challenges. Indeed in many mixed-signal circuits, the test of the analogue blocks may represent up to 90% of the whole test effort while these blocks represent only 10% of the whole chip area. The reason of such a challenge is twofold. Firstly, analogue testing is made of a long sequence of parametric measurements that are performed using highly precise, but very expensive, instruments. Secondly, the access, the control and the observation of deeply embedded analogue blocks – and consequently, the test access, the test control and the test observation- are increasingly limited, as far as the number of pads is greatly reduced. Consequently the internal accessibility of the whole system is drastically decreasing. Also, as signals become faster and systems are operated at higher speeds, external testing become more susceptible to noise, crosstalk and probing problems.

To overcome these problems, several authors have proposed different Built-In-Self-Test (BIST) techniques where signals are internally generated and/or analyzed [1-7]. Another possible and less expensive solution consists in introducing Design-for-Test (DfT) features to internally transform the analogue signals into digital signals that are made controllable and observable from the chip I/Os [8-11]. As a result, only digital signals are externally handled by non-expensive digital test equipment (Low Cost Tester).

In an example prototype for Set-Top-Box applications, like in most current mixed-signal systems, the converters are among the main components: 2 Analogue-to-Digital Converters (ADC) and 6 Digital-to-Analogue Converters (DAC) are embedded in the same SiP. The present specifications for these converters require a 10-bit resolution, but the next generations will make use of 12-bit converters. Testing this whole set of converters is a very complex task requiring a long test time because of the above mentioned problems of accessibility, signal integrity, accuracy of converter parameter measurements.

In this context, an original DfT technique called "Analogue Network of Converters" (ANC) was developed that permits to test the whole set of embedded ADCs and DACs [12]. An extremely minimal circuitry is added to the original chip allowing the application of a fully digital low-cost test to the System-in-Package/System-On-Chip. The basic principle relies on setting a test path with DACs and ADCs. The fault masking is avoided by using a post-processing algorithm that discriminates harmonics from the different converters inserted in the test path. The ANC-based method can also be exploited to test standalone ADCs using low resolution arbitrary waveform generators as it breaks the rule stating that the test equipment resolution should be at least 2 bits higher than the ADC under test [13].

The ANC-based method was developed with the assumption that the phase of the harmonic components is strictly proportional to the input signal nominal phase. However our experiments did not confirm this theoretical assumption. Indeed, we could observe that some harmonics may have a non-null phase, despite the input signal phase being set to zero. In this paper, we present an extension of the primarily developed method to the estimation of the harmonics of the output samples with a phase which is not correlated to the phase of the input signal.

The paper is organized as follows. Section 2 gives the fundamental knowledge on data converter testing based on spectral analysis and pinpoints the issues related to the phase of harmonics. Section 3 summarizes the principle of the ANC-based method. The mathematical developments of the improved ANC-based method are then presented in section 4, followed by the validation results in section 5. Finally, section 6 concludes the paper.

2. CONVERTERS, HARMONICS AND PHASES

A very popular test for data converters relies on spectral analysis. It is usually implemented in a DSP-based test architecture [9, 14]. Basically, a single tone sine-wave stimulus is sourced to the converter input, and then an FFT analysis is performed on the output sample set. The resulting spectrum is subsequently processed to compute the dynamic parameters such as the Total Harmonic Distortion (THD) or the Spurious Free Dynamic Range (SFDR). The spectrum also permits to estimate an essential static parameter, i.e. the Integral Non Linearity (INL), using the method proposed in [15].

A typical spectrum considering an ADC driven by an ideal sine-wave at frequency f_0 is illustrated in figure 1. This spectrum exhibits a fundamental bin at f_0, the harmonic components being located at multiple values of the fundamental frequency, and noise at other frequencies. The fundamental component corresponds to the input sine-wave while other components are induced by the converter non-idealities.

Figure 1. Output spectrum of an ADC under an ideal sine-wave stimulus

The dynamic parameters are subsequently evaluated from this spectrum. In particular, the typical definitions for the THD and SFDR parameters are given by:

$$THD(dB) = 10 * \log_{10}\left(\frac{\sum_{k\geq 2} H_k{}^2}{F^2}\right) \tag{1}$$

$$SFDR(dB) = 20 * \log_{10}\left(\frac{F}{\max(H_k)}\right) \tag{2}$$

where F is the amplitude of the fundamental and H_k the amplitude of the kth harmonic.

To introduce the theoretical fundamentals, let us consider an ideal sine-wave applied to an ADC. Using a Fourier series expansion, the output signal can be expressed by equation (3. This equation distinguishes the sampled sine-wave *x(n)* that would be delivered by an ideal ADC from the sum of all harmonic contributions introduced by the converter non-idealities. Hence H_0 corresponds to the offset contribution of the converter and H_1 corresponds to the contribution of the gain error and non linearity of the converter. The total amplitude of the fundamental component, previously defined as F, is the sum of H_1 and the contribution of the ideal ADC, which is included in *x(n)* in equation (3):

$$s(n) = x(n) + \sum_{k\geq 0} H_k \cos\left(k\left(\theta_n + \theta_i\right) + \theta_k\right) + \varepsilon(n) \tag{3}$$

where n is the sample index, θ_i the input phase, θ_k the phase of the kth harmonic, $\varepsilon(\,)$ the noise that affect the converted signal, and θ_n the nominal sampling phase given by:

$$\theta_n = 2\pi \frac{M}{N} n \tag{4}$$

where N is the number of samples and M the number of cycles (i.e. signal periods) in the sample set.

The theoretical developments that mathematically link the harmonic components to the converter INL are given in [15].

The expression of the output signal can be easily linked to the spectrum presented in figure 1 by developing equation (3):

$$s(n) = x(n) + \sum_{k\geq 0} \left(H_k \cos\left(k\theta_i + \theta_k\right)\cos(k\theta_n) - H_k \sin\left(k\theta_i + \theta_k\right)\sin(k\theta_n)\right) + \varepsilon(n) \tag{5}$$

The sum term corresponds to the Fourier series expansion made of the complex harmonic values resulting from the FFT. Indeed, $H_k \cos(k\theta_i + \theta_k)$ is equal to the real part of the harmonic computation and $H_k \sin(k\theta_i + \theta_k)$ is equal to the imaginary part.

Now if we consider the case of a converter with harmonics' phase proportional to the input phase:

$$\theta_k = k\theta_i \quad (\pi) \tag{6}$$

and by setting the input phase θ_i to zero, equation (5) becomes:

$$s(n) = x(n) + \sum_{k\geq 0} H_k \cos\left(k\theta_n\right) + \varepsilon(n) \tag{7}$$

In this case, the imaginary part of the spectrum is cancelled and only the real part of the spectrum directly corresponds to the amplitude of the spectrum.

However if we consider the case of a converter with harmonics' phase not correlated to the input phase, setting the input phase θ_i to zero leads to:

$$s(n) = x(n) + \sum_{k\geq 0} \left(H_k \cos(\theta_k)\cos\left(k\theta_n\right) - H_k \sin(\theta_k)\sin\left(k\theta_n\right)\right) + \varepsilon(n) \tag{8}$$

In this case, it clearly appears that both the real and the imaginary parts of the spectrum have to be considered and used in the computation of the dynamic parameters.

3. ANC FUNDAMENTAL PRINCIPLE

The Analogue Network of Converters, presented in [12], is a DfT concept developed to enable the fully digital test of a set of DACs and ADCs embedded in a complex system. It can also be used to relax the requirements on the test equipment in case of stand-alone converter testing [13].

In the ANC-based method, the analogue outputs of the DACs are basically connected to the analogue inputs of the ADCs so that only digital test resources are required to apply the test stimuli and capture the test responses. Similarly to a classical DSP-based test, single-tone sine-waves are used as test stimuli and the test response analysis is based on the FFT computation of the captured output samples. The method addresses networks embedding several ADCs and DACs, and is even more efficient as the number of tested converters increases. As illustrated in figure 2, the method requires at least two DACs and one ADC. The idea is then to exploit different configurations and different test conditions in order to separate the harmonic contribution of each converter. Switches enable to connect any DAC output (I_i) or combination of DAC outputs to any ADC input (O_i).

Figure 2. Analog Network of Converters (ANC) concept

The mathematical developments were established considering only static non-idealities of the converters, meaning that the harmonics' phase of each converter was not taken into account. In this case, the model presented in equation (3) simplifies and becomes:

$$s(n) = x(n) + \sum_{k \geq 0} H_k \cos\left(k\left(\theta_n + \theta_i\right)\right) + \varepsilon(n) \tag{9}$$

We are therefore in the situation where setting the initial phase θ_i to zero results in the cancellation of the imaginary part of the spectrum, and the real part directly leads to the amplitude of the spectrum.

To illustrate the method, let us first consider a test configuration where the DAC1 output is directly connected to the ADC1 input (Fig. 3). The spectrum of the resulting output signal is computed and the values of the harmonic components $H_k^{m,1}$ are extracted. Obviously, the output signal is affected by errors of both converters. In other words, the resulting spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of ADC1. According to equation (9), setting a zero initial phase shift, we can write the following equation:

$$H_k^{m,1} = Hdac1_k^{FS} + Hadc1_k^{FS} \tag{10}$$

where $Hdac1_k^{FS}$ and $Hadc1_k^{FS}$ correspond to the amplitude of the k^{th} harmonic of DAC1 and ADC1 respectively, for a full-scale input signal (*FS*).

Equation (10) establishes a relation between the harmonic contributions of the two converters involved in the test configuration. In this equation, the left member is known and corresponds to the amplitude of the k^{th} spectral bin measured on the spectrum, while the right member corresponds to the unknowns under calculation.

This short example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the ANC-based method. By using different configurations, we can establish different equations. The objective is then to determine the adequate set of configurations that results in a system of independent equations, which can be solved to discriminate the harmonic contribution of each converter. We have identified 3 different configurations (DAC1/ADC1, DAC2/ADC1 and DAC1+DAC2/ADC1) associated with 4 different test conditions (related to amplitude and phase of test stimuli) that permit to obtain a system of five independent equations:

$$\begin{cases} H_k^{m,1} = Hdac1_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,2} = Hdac2_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,3} = Hdac2_k^{FS/2} + Hadc1_k^{FS/2} \\ H_k^{m,4} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\pi) + Hadc1_k^{FS/2} \\ H_k^{m,5} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\varphi_1) + Hadc1_k^{FS}\cos(k\varphi_2) \end{cases}$$

$$\text{with} \quad \varphi_1 = \pi - 2\arccos\left(\frac{1}{4}\right) \quad \text{and} \quad \varphi_2 = \pi - \arccos\left(\frac{1}{4}\right)$$

The different configurations and conditions will be presented in the next section. Solving this system permits to compute the amplitude of the harmonic components, for each individual converter.

4. EXTENSION OF THE ANC-BASED METHOD

A limitation of the ANC-based method described in the previous section is that the phase of the harmonics is not taken into account in the mathematical developments. However, the method was proven efficient in practical experimentations with real-life converters [16]. This can be explained by the fact that in all experiments, the converters under study exhibited a phase of harmonics linearly proportional to the input signal nominal phase. In such a situation, when setting the input signal nominal phase to zero, the imaginary part of the spectrum is cancelled and the real part directly gives the amplitude in the spectrum. The system of equations established from the model given by equation (9) is therefore valid and leads to a correct estimation of the harmonic contribution of each individual converter. However the assumption that the harmonics' phase is linearly proportional to the input signal nominal phase is not always verified and highly depends on the converter architecture. We have seen that this assumption is often verified for types of architecture that use a sample and hold stage, but it cannot be assessed for other architectures where filtering and noise may affect the harmonics' phase. Our objective is consequently to improve the ANC-based method to cover all the real-life cases.

The fundamental principle of this improved version of the ANC-based method is the same, but the mathematical developments have now to be established using the complete model of the general case, i.e. the model described by equation (3).

4.1. First configuration: 1 DAC connected to 1 ADC

Let us consider again the configuration in which the DAC1 output is directly connected to the ADC1 input (Fig. 3). The signal applied on the DAC input covers the full scale of the converters. This configuration constitutes the first step of the ANC method.

Figure 3. First test configuration, first test setup

Obviously, the output signal is still affected by errors of both converters. The spectrum of the resulting output signal is computed and the values of the harmonic components $H_k^{m,1}$ are extracted. Now, considering the general case described in equation (3) and setting the input signal nominal phase θ_i to zero, we can write the following equations:

$$\begin{cases} \mathrm{Re}(H_k^{m,1}) = Hdac1_k^{FS}\cos(\theta_{dac1,k}^{FS}) + Hadc1_k^{FS}\cos(\theta_{adc1,k}^{FS}) \\ \mathrm{Im}(H_k^{m,1}) = -Hdac1_k^{FS}\sin(\theta_{dac1,k}^{FS}) - Hadc1_k^{FS}\sin(\theta_{adc1,k}^{FS}) \end{cases} \quad (11)$$

In the second step, the test path goes through DAC2 and ADC1 (Fig. 4). The amplitude of the test signal still reaches the full scale of the converters. Therefore, we obtain a second couple of equations given by (12), where $H_k^{m,2}$ is the amplitude of the kth harmonic measured on the ADC output.

Figure 4. First test configuration, second test setup

$$\begin{cases} \mathrm{Re}(H_k^{m,2}) = Hdac2_k^{FS}\cos(\theta_{dac2,k}^{FS}) + Hadc1_k^{FS}\cos(\theta_{adc1,k}^{FS}) \\ \mathrm{Im}(H_k^{m,2}) = -Hdac2_k^{FS}\sin(\theta_{dac2,k}^{FS}) - Hadc1_k^{FS}\sin(\theta_{adc1,k}^{FS}) \end{cases} \quad (12)$$

At this point, we have six unknown parameters ($Hdac1_k^{FS}$, $\theta_{dac1,k}^{FS}$, $Hdac2_k^{FS}$, $\theta_{dac2,k}^{FS}$, $Hadc1_k^{FS}$ and $\theta_{adc1,k}^{FS}$) and only four equations (11 and 12) from two acquisitions.

We can now play with the amplitude and phase of the input signal to establish new equations. The input signal phase has no influence on the converter harmonic contribution but the input signal amplitude A_{in} modifies the converter harmonic contribution ($Hdac1_k^{A_{in}} \neq Hdac1_k^{FS}$ if $A_{in} \neq FS$). No trivial relationship exists between these different harmonic contributions. Consequently, the use of different amplitudes induces additional unknown parameters. Nevertheless, it also introduces new test setup possibilities that can be exploited to get additional independent useful information.

Practically, we have looked for a system of equations that allows the discrimination of the three converter harmonic contributions using test stimuli with amplitude at full-scale and amplitude at half-scale.

The new third equation is the result of a test at half-scale through DAC2 and ADC1 (Fig. 5).

Figure 5. First test configuration, third test setup

The measured harmonics are the sum of DAC2 and ADC1 harmonic contributions for an input signal at half-scale.

$$\begin{cases} \mathrm{Re}(H_k^{m,2}) = Hdac2_k^{FS/2}\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right) \\ \mathrm{Im}(H_k^{m,2}) = -Hdac2_k^{FS/2}\sin\left(\theta_{dac2,k}^{FS/2}\right) - Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right) \end{cases} \quad (13)$$

Thanks to this test, we add two new equations, but four new unknowns ($Hdac2_k^{F/2S}$, $\theta_{dac2,k}^{FS/2}$, $Hadc1_k^{F/2S}$ and $\theta_{adc1,k}^{FS/2}$).

At this point, we therefore have ten unknown parameters and only six equations (11-13) from three acquisitions. It would obviously be vain to apply new test conditions with different input signal amplitudes in the same test configuration. To avoid this problem, the two DAC's outputs are added to establish a new configuration. This new configuration is described in the next section.

4.2. Second configuration: 2 DACs connected to 1 ADC

The second hardware configuration is made up of two DACs and one ADC. The input of the ADC is the sum of the two DAC outputs. Note that a similar test configuration has already been described in [17]. But in this case, the objective was to test only the ADC, the DACs having a higher resolution than the one of the ADC under test. This is not the case in our method, which permits to test an ADC using DACs of similar or even lower resolution as demonstrated in [13].

For the sake of simplicity, let us consider three converters with same resolution and dynamic range. Obviously, we cannot use the sum of two full-scale and in-phase signals from DAC1 and DAC2, because it would result in a signal with an amplitude of twice the converters' full-scale and would saturate the ADC. The solution to overcome this problem is to play with amplitude and phase shift of the input signals to result in a sum signal that remains within the full scale of the ADC.

Practically, the 4th test setup involves a full-scale input signal on DAC1 and a half-scale input signal on DAC2 with a π phase shift (Fig. 6). The resulting signal at the ADC input is a sine-wave at half-scale:

$$\cos(x) + \frac{\cos(x+\pi)}{2} = \cos(x) - \frac{\cos(x)}{2} = \frac{\cos(x)}{2} \quad (14)$$

Figure 6. Second test configuration, fourth test setup

The resulting couple of equations is the sum of the harmonic contribution at full scale of DAC1, the harmonic contribution at half-scale of DAC2 balanced by the phase shift and the harmonic contribution at ½ full-scale of ADC1.

$$\begin{aligned} \mathrm{Re}\left(H_k^{m,4}\right) &= \left[Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hdac2_k^{FS/2}\cos(k\pi)\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right)\right] \\ \mathrm{Im}\left(H_k^{m,4}\right) &= -\left[Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) + Hdac2_k^{FS/2}\cos(k\pi)\sin\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right)\right] \end{aligned} \quad (15)$$

The 5th required test setup is very similar to the previous one. The input amplitudes are the same as before but they are relatively phase shifted of φ_1. The resulting signal at the ADC input is now a sine-wave at full-scale with a phase shift of φ_2.

$$\cos(x) + \frac{\cos(x+\varphi_1)}{2} = \cos(x+\varphi_2) \quad (16)$$

$$\text{with } \varphi_1 = \pi - 2ar\cos\left(\frac{1}{4}\right),\ \varphi_2 = \pi - ar\cos\left(\frac{1}{4}\right) \quad (17)$$

The 5th couple of equations then corresponds to the sum of the harmonic contributions balanced by their phase shifts:

$$\begin{aligned}\mathrm{Re}\left(H_k^{m,5}\right)&=\left[Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\left[\cos\left(k\varphi_1\right)\cos\left(\theta_{dac2,k}^{FS/2}\right)-\sin\left(k\varphi_1\right)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right]+Hadc1_k^{FS}\left[\cos\left(k\varphi_2\right)\cos\left(\theta_{adc1,k}^{FS}\right)-\sin\left(k\varphi_2\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right]\right]\\ \mathrm{Im}\left(H_k^{m,5}\right)&=-\left[Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\left[\sin\left(k\varphi_1\right)\cos\left(\theta_{dac2,k}^{FS/2}\right)+\cos\left(k\varphi_1\right)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right]+Hadc1_k^{FS}\left[\sin\left(k\varphi_2\right)\cos\left(\theta_{adc1,k}^{FS}\right)+\cos\left(k\varphi_2\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right]\right]\end{aligned} \quad (18)$$

In summary, the proposed test strategy is composed of five successive tests. Each test consists in an acquisition and a spectral analysis (with Fast Fourier Transform) to evaluate harmonic bins. We obtain a system of 10 independent equations for each harmonic bin given hereafter.

$$\begin{cases}\mathrm{Re}\left(H_k^{m,1}\right)=Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right)\\ \mathrm{Im}\left(H_k^{m,1}\right)=-Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)-Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right)\\ \mathrm{Re}\left(H_k^{m,2}\right)=Hdac2_k^{FS}\cos\left(\theta_{dac2,k}^{FS}\right)+Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right)\\ \mathrm{Im}\left(H_k^{m,2}\right)=-Hdac2_k^{FS}\sin\left(\theta_{dac2,k}^{FS}\right)-Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right)\\ \mathrm{Re}\left(H_k^{m,3}\right)=Hdac2_k^{FS/2}\cos\left(\theta_{dac2,k}^{FS/2}\right)+Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right)\\ \mathrm{Im}\left(H_k^{m,3}\right)=-Hdac2_k^{FS/2}\sin\left(\theta_{dac2,k}^{FS/2}\right)-Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right)\\ \mathrm{Re}\left(H_k^{m,4}\right)=\left[Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\cos\left(k\pi\right)\cos\left(\theta_{dac2,k}^{FS/2}\right)+Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right)\right]\\ \mathrm{Im}\left(H_k^{m,4}\right)=-\left[Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\cos\left(k\pi\right)\sin\left(\theta_{dac2,k}^{FS/2}\right)+Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right)\right]\\ \mathrm{Re}\left(H_k^{m,5}\right)=\left[Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\left[\cos\left(k\varphi_1\right)\cos\left(\theta_{dac2,k}^{FS/2}\right)-\sin\left(k\varphi_1\right)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right]+Hadc1_k^{FS}\left[\cos\left(k\varphi_2\right)\cos\left(\theta_{adc1,k}^{FS}\right)-\sin\left(k\varphi_2\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right]\right]\\ \mathrm{Im}\left(H_k^{m,5}\right)=-\left[Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\left[\sin\left(k\varphi_1\right)\cos\left(\theta_{dac2,k}^{FS/2}\right)+\cos\left(k\varphi_1\right)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right]+Hadc1_k^{FS}\left[\sin\left(k\varphi_2\right)\cos\left(\theta_{adc1,k}^{FS}\right)+\cos\left(k\varphi_2\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right]\right]\end{cases}$$

with $\varphi_1=\pi-2\arccos\left(\frac{1}{4}\right)$ and $\varphi 2=\pi-\arccos\left(\frac{1}{4}\right)$

This system can be solved to determine the real and imaginary parts of harmonic contribution related to the different converters. From this, the dynamic parameters such as THD and SFDR can be computed for each converter. Solving this system of equations therefore makes the independent characterization of each converter possible.

4.3. Further configurations to test additional converters

Thanks to the converter characterization obtained from the second configuration, testing every additional converter embedded in the same complex chip is straightforward. For that, we can use one of the three previously characterized converters as a measurement instrument with non-ideal, but known, specifications.

The test time directly depends on the number of required captures. The first step of the test procedure needs five captures to test three devices. Then the new test configuration is achieved by connecting one converter to an previously characterized converter. Doing that, and considering (11), only one couple of variables is unknown: the harmonic contribution of the uncharacterized converter (amplitude and phase). As a consequence we need only one additional acquisition to test this converter. So, the number of acquisitions for a complex chip with n DACs and m ADCs is only of n+m+2 acquisitions without any external analogue equipment requirement.

Moreover, because the test stimulus application and the test response capture are performed using only digital ATE resources, it is possible to concurrently test several converters. Consequently, after the first step, each new step could use simultaneously all available characterized converters as measurement instruments. In this configuration, the test time could be drastically shortened.

5. VALIDATION

The theoretical extension of the ANC-based test method has been validated through simulation, using the converter model described in [12]. Converter non-idealities are included in the model based on real-life INL values extracted from measurements on several data converters. Sampling jitter and thermal noise are also considered. In addition, we also include a possible injection of an arbitrary phase shift on the converter harmonics.

5.1. Data converter model

To simulate the test strategy, we need to establish a model that takes into account the effects of the converter non-idealities. Three main sources of errors will be considered, i.e. the sampling jitter of the converter, the non-linearities of its transfer function and the thermal noise.

Let us consider an input sine-wave sourced to an ideal converter. This sampled signal can be expressed (in LSB unit) by:

$$x(n)=2^N\left(\frac{V_0}{V_{FS}}\right)\cos\left(\theta_n+\theta_0\right)+2^N\left(\frac{V_{DC}}{V_{FS}}\right) \quad (19)$$

where N and V_{FS} respectively represent the number of bits and the full-scale voltage of the converter, V_0 and V_{DC} respectively correspond to the amplitude and the DC component of the input sine-wave, and θ_0 and θ_n are respectively the initial and nominal sampling phase of the signal. The nominal sampling phase is given by:

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n \tag{20}$$

where M is the number of samples and P the number of periods in the record.

Let us now introduce the sampling jitter of the converter. Essentially, it is a phase noise that changes the ideal sampling time. The resulting deteriorated signal is given by:

$$r(n) = 2^N\left(\frac{V_0}{V_{FS}}\right)\cos(\theta_n + J_t + \theta_0) + 2^N\left(\frac{V_{DC}}{V_{FS}}\right) \tag{21}$$

where $J_t = 2\pi f_0 \delta_t$, with f_0 the frequency of the input signal and δ_t a centred Gaussian noise. According to [4] and thanks to a Taylor series development, the jitter contribution can be separated from the input signal expression in (21). Finally, considering an additional thermal noise we obtain the following expression:

$$r(n) = x(n) + \varepsilon(n) \tag{22}$$

where $\varepsilon(n)$ is the sum of the noise induced by the sampling jitter and the thermal noise (N_{Th}). The thermal noise is usually modelled by a centred Gaussian noise.

$$\varepsilon(n) = 2^N \frac{V_0}{V_{FS}} J_t \sin(\theta_n + \theta_0) + N_{Th} \tag{23}$$

The second significant source of errors that has to be considered is the non-linearity of the converter transfer function. A common approach to analytically model the converter INL is based on polynomial approximation [4, 18, 19]. However, such modelling does not permit to describe the sharp transitions usually encountered for actual INL. In order to alleviate this drawback, we choose a different approach which consists in using "true" INL curves extracted from measurements on real data converters.

Consequently, let us consider $s(n)$ the signal deteriorated by the two types of errors:

$$s(n) = \left[\ r(n) + INL([r(n)])\ \right] \tag{24}$$

where $INL(x)$ is a non-linearity curve measured through histogram testing of a real converter. This non-linearity curve is indexed by the rounded signal [$r(n)$], including the sampling jitter effect. The complete equation is rounded to model the quantization effect.

Equation (24) is the equation that models the deterioration of a sine-wave signal passing through a converter affected by sampling jitter, transfer function non-linearities and thermal noise. In addition, an individual phase shift can be introduced on each harmonic individually. This equation has been used for the simulations described in the following sections.

5.2. Validation of the extended method improvement with random phase harmonics

In order to validate the improved ANC-based method, we have considered a set of three converters, i.e. two DACs and one ADC. First, we have simulated each data converter in a stand-alone configuration applying a single-tone sine-wave stimulus to the converter input and performing an FFT analysis on the converter output. This corresponds to the usual DSP-based test and is used to get reference values for the THD and SFDR parameters. Then, we have simulated the set of converters in the different configurations and test conditions defined in the ANC-based method. Here again single-tone sine-waves are used as test stimuli and an FFT is performed on the captured output samples. From these five acquisitions, we have established the system of independent equations that links the measured harmonic contribution to the individual harmonic contribution of each converter (considering only the real part of the spectrum for the original ANC-based method and both the real and imaginary parts of the spectrum for the improved ANC-based method) and we have solved the system. Finally, we have computed the THD and SFDR parameters using the estimated amplitude of the harmonic components.

Results are summarized in Tables I to IV, which compare the values of the THD and SFDR parameters computed using the stand-alone configuration to the values of the THD and SFDR parameters computed using either the original or the improved ANC-based method, with and without phase shift injected on the converters' harmonics.

TABLE I. THD VALUES AND ESTIMATION ERRORS WITHOUT PHASE SHIFT ON CONVERTERS' HARMONICS

TABLE II. SFDR VALUES AND ESTIMATION ERRORS WITHOUT PHASE SHIFT ON CONVERTERS' HARMONICS

TABLE III. THD VALUES AND ESTIMATION ERRORS WITH A RANDOM PHASE SHIFT INJECTED ON CONVERTERS' HARMONICS

TABLE IV. SFDR VALUES AND ESTIMATION ERRORS WITH A RANDOM PHASE SHIFT INJECTED ON CONVERTERS' HARMONICS

Analyzing these results, it can be seen that when the converters' harmonics are not affected by a random phase shift, both the original and the improved versions of the ANC-based method produce an accurate measurement of the THD and SFDR parameters, with an estimation error that remains below 0.7dB. However when the converters' harmonics are affected by a random phase shift, the performances of the original ANC-based method degrades with an estimation error that increases up to 4.3dB for the THD parameter of DAC1. In contrast, the improved ANC-based method gives very accurate measurements, with an estimation error lower than 0.2dB. These results clearly validate the efficiency of the improved ANC-based method.

5.3. Validation in a realistic case

The purpose of this validation is to get as close as possible to a realistic case. Let us consider a circuit made of a DAC and a low-pass filter. In case of the impossibility to bypass the filter in the test path, the DAC/filter chain should be tested as one single component. An obvious solution to estimate the harmonic distortions induced by the DAC is to choose the frequency of the test signal in the bandwidth of the filter. Although the presence of the filter has no influence on the amplitude of the in-band signals, it introduces a group delay that can induce some significant phase delays to the resulting signals. This situation is similar to the one addressed by the algorithm previously described. We have a test stimulus, i.e. a sine-wave, affected by harmonics induced by a DAC. The phases of these harmonics are not proportional anymore to the stimulus phase because of the filter.

This case has been simulated considering a 12bit DAC, a 2^{nd} order Bessel filter with a cut-off frequency at 30MHz (Fig. 7), and a test frequency of 4.43MHz.

Figure 7. Bode plot of Bessel low-pass filter

The test configuration is made of two DACs with different non-linearities, followed by a filter. The filter outputs are summed and the result is sent to an ADC (Fig. 8), with no phase delays added.

Figure 8. Simulated test configuration

Simulation results are provided in Tables V and VI. Although the low pass filters introduce phase shifts on the test path, it can be seen that the improved ANC method permits good characterization of DACs with an estimation error below 0.8dB, whereas the original ANC method presents an estimation error ranging from 1.5dB to 2.4dB. Concerning the ADC, we observed similar results with both the original and improved versions of the method.

TABLE V. THD VALUES AND ESTIMATION ERRORS WITH PHASE SHIFT FROM LOW-PASS FILTER

TABLE VI. SFDR VALUES AND ESTIMATION ERRORS WITH PHASE SHIFT FROM LOW-PASS FILTER

5.4. Wide range validation

The purpose of this second simulation set is to validate the approach not only for DACs but also for ADCs and for a wide range of phase variations.

Considering the basic test configuration described in 5.2, made of two DACs and one ADC, we modified the converter models to introduce random phase delays on the harmonics generated by the converters' non linearities. We ran 400 simulations using different phases for each harmonic of each converter. The phases were randomly chosen following a normal distribution. Figure 9 presents the histogram of the phases chosen for the harmonic 2 of DAC2 as an illustration. The standard deviation is $\pi/6$. For each simulation, the THD and SFDR were estimated using both the original and improved ANC algorithms.

Figure 9. Histogram of phase variations applied to harmonic 2 of DAC2

Figure 10 presents the histogram of the 400 THD estimations for DAC2:

- using the original ANC method (light grey bars),
- using the improved version of ANC method (dark grey bars).

The value of the THD, obtained with a usual test method in a stand-alone configuration, is referenced on the histogram (74.4dB).

Figure 10. Histogram of THD estimations with original and improved ANC methods for DAC2

Figure 11 presents the histogram of the 400 SFDR estimations for DAC2:

- using the original ANC method (light grey bars),
- using the improved version of ANC method (dark grey bars).

The value of the SFDR, obtained with a usual test method in a stand-alone configuration, is referenced on the histogram (76.1dB).

Figure 11. Histogram of SFDR estimations with original and improved ANC methods for DAC2

These histograms enable to give visual conclusions. The estimation of dynamic parameters follows a normal distribution as much as the phase delays distribution. The dynamic parameter estimations are far much spread and consequently the estimation errors are bigger with the original method than with the new version of the method.

Following tables summarize the numerical results. Tables VII and VIII give respectively THD and SFDR estimations for the three converters. In order to have a clear overview of the measurement accuracy against random phase delays, the average, dispersion and maximum error are presented in the tables.

TABLE VII. SUMMARY OF THD ESTIMATIONS FOR RANDOM PHASE DELAYS (STANDARD DEVIATION=π/6)

TABLE VIII. SUMMARY OF SFDR ESTIMATIONS FOR RANDOM PHASE DELAYS (STANDARD DEVIATION=π/6)

The update of the method decreases the dispersion from the range [7.6, 13.1dB] to the range [1.0, 1.8dB] and the maximum error from [5.9, 9.0dB] to [0.6, 1.1dB]. In other words, in case of random phase delays of harmonic induced by tested converters, the updated ANC method ensures low estimation error. A maximum estimation error of 1dB is fully acceptable considering that industrial test repeatability is usually around 2dB.

We repeated the simulations with a higher standard deviation of π, to confirm the accuracy of the new method against phase delays. The simulation results are provided in Tables IX and X.

TABLE IX. SUMMARY OF THD ESTIMATIONS FOR RANDOM PHASE DELAYS (STANDARD DEVIATION=π)

TABLE X. SUMMARY OF THD ESTIMATIONS FOR RANDOM PHASE DELAYS (STANDARD DEVIATION=π)

Despite the increase of phase delays, we still have a significant decrease of dispersions and maximum errors: from range [8.4dB, 20.2dB] to range [0.8dB, 2.6dB] regarding dispersion and from range [6.2dB, 14.4dB] to range [0.5dB, 1.5dB] regarding maximum error. Considering a maximum error lower than 1.5dB, we can conclude that the method is still accurate with high amplitudes of random phase delays.

6. CONCLUSION

In this paper, we have presented an extension of the ANC-based method capable of handling converters with random-phase harmonics. Indeed, the ANC-based method was originally developed under the assumption that the harmonics' phase is proportional to the input phase. Although this assumption is often verified, it is not valid for all converter types of architecture. New mathematical developments based on a general model that includes the harmonics' phase of converters were therefore established. The efficiency of the improved ANC-based test was evaluated through simulations, demonstrating an excellent agreement between the THD and SFDR values measured with a usual test setup and the THD and SFDR values computed with the method.

Compared to the initial ANC-based test method, no additional resources are required, and the number of test configurations and test acquisitions remains the same. Only the size of the independent equations system is different, growing

from 5 to 10. However, it is worth noting that this computation is performed off-chip using the tester digital signal processing resources and has no impact on the cost of the test procedure. These developments therefore offer an efficient generic method to perform the harmonic characterization of a set of data converters using only digital external test equipment, without any assumption on the converter architecture and potential phase shift of the converter harmonics.

The improvement of the extension of the ANC-based method was validated through a number a simulations involving random phase shifts as well as realistic filter phase delays on the harmonic contributions.

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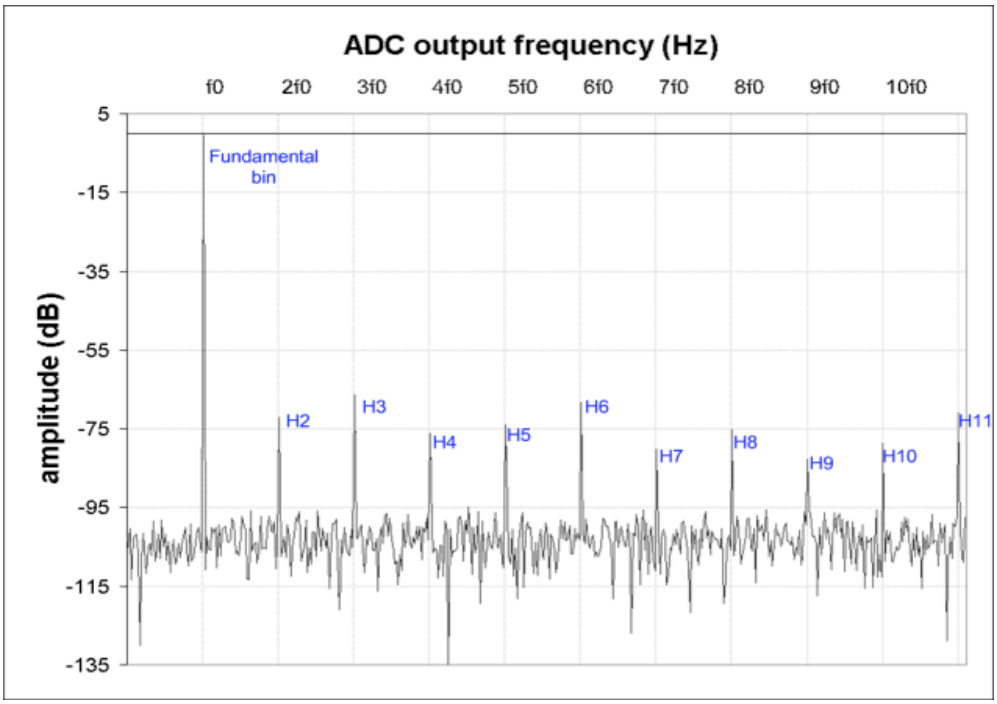

Figure 1: Output spectrum of an ADC under an ideal sine-wave stimulus

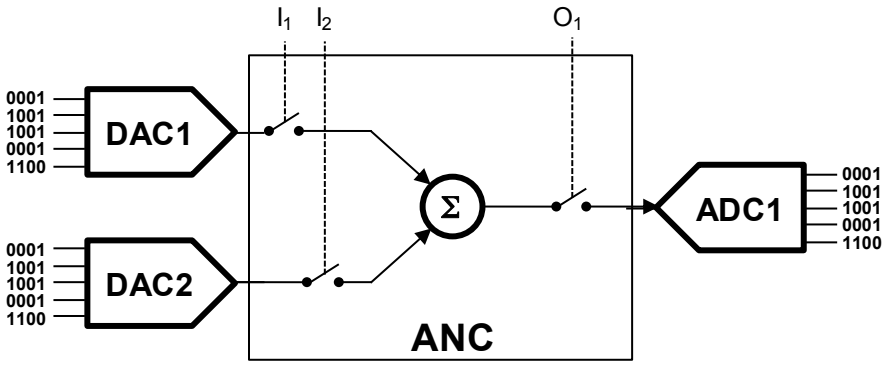

Figure 2: Analogue Network of Converters (ANC) concept

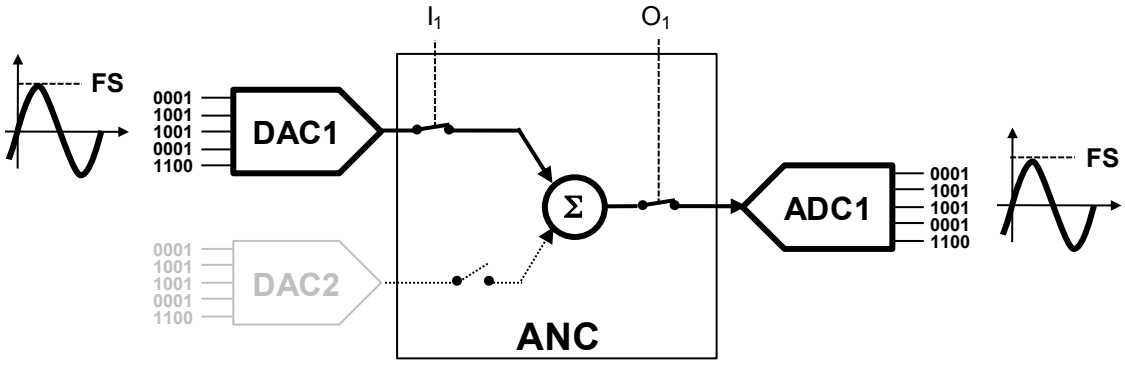

Figure 3: First test configuration, first test setup

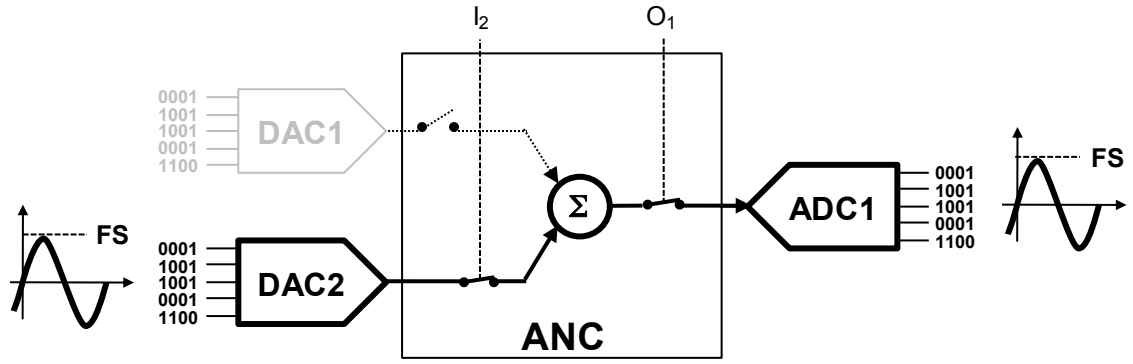

Figure 4: First test configuration, second test setup

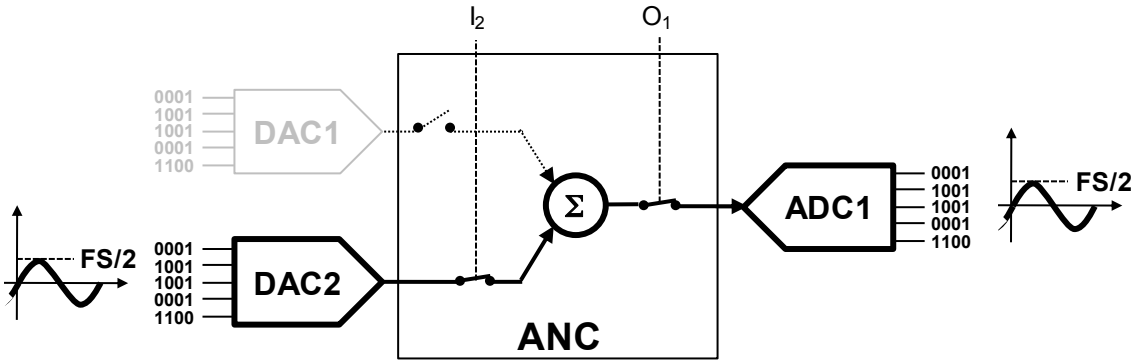

Figure 5: First test configuration, third test setup

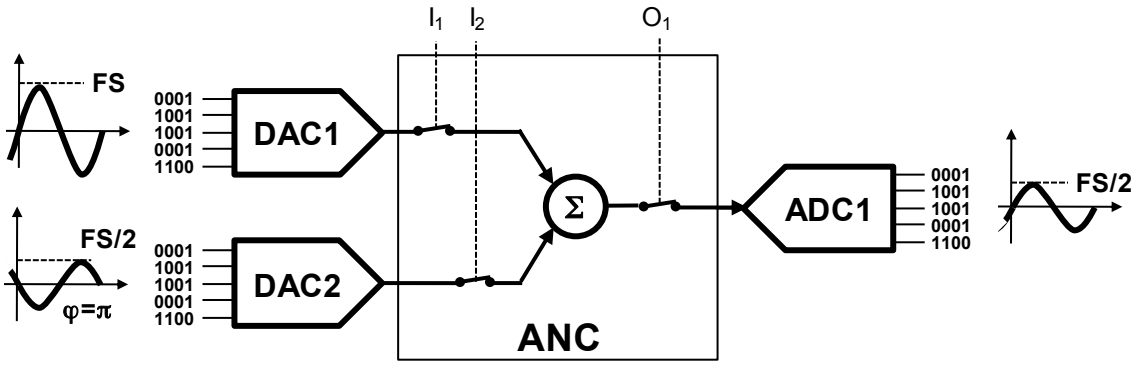

Figure 6: Second test configuration, fourth test setup

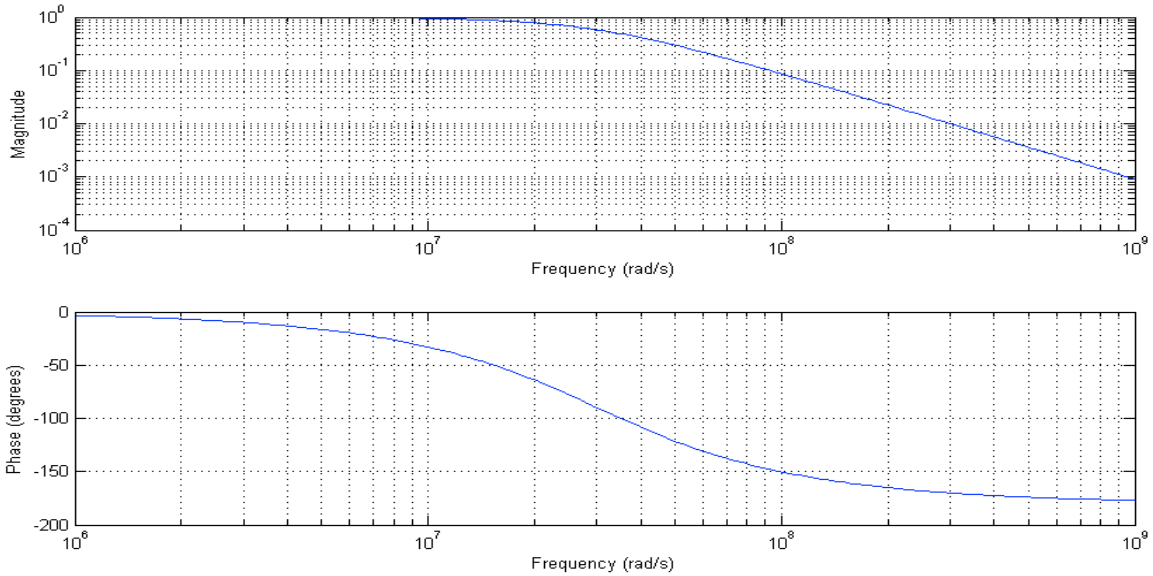

Figure 7: Bessel low-pass filter Bode plot

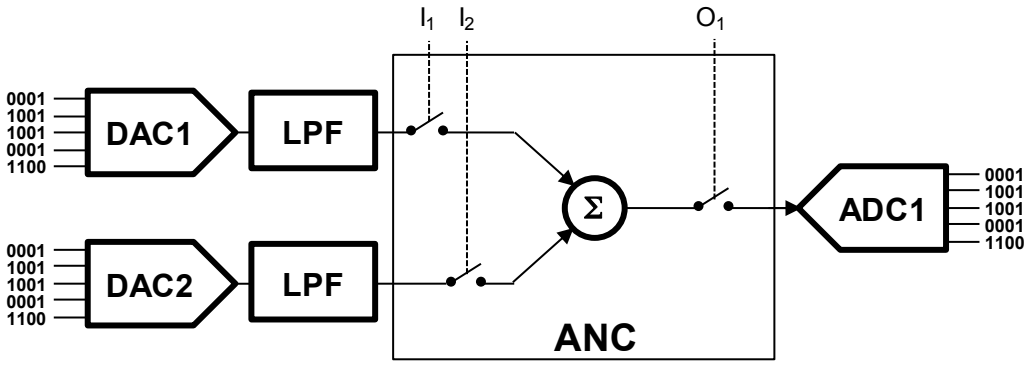

Figure 8: Simulated test configuration

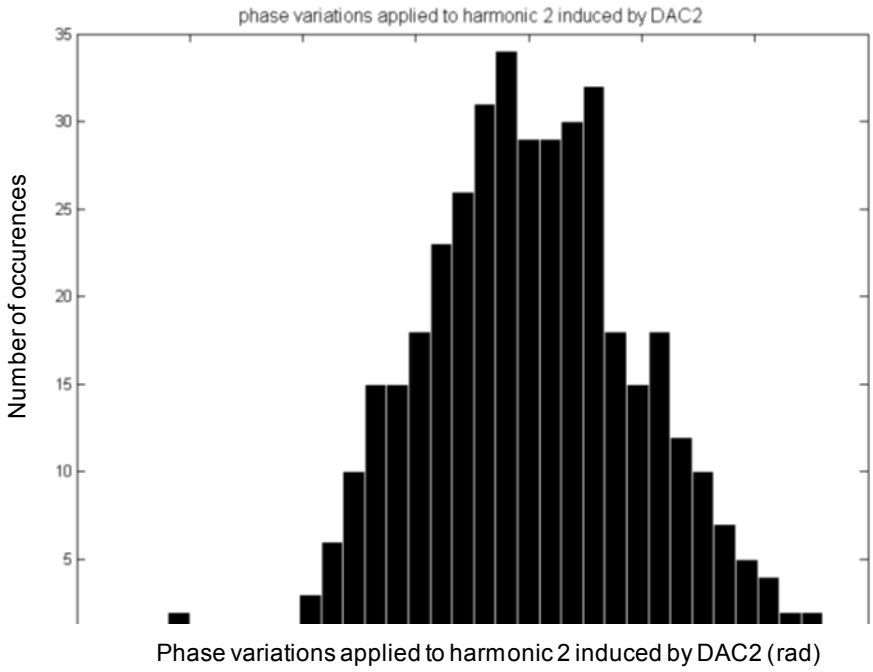

Figure 9: Histogram of phase variations applied to harmonic 2 of DAC2

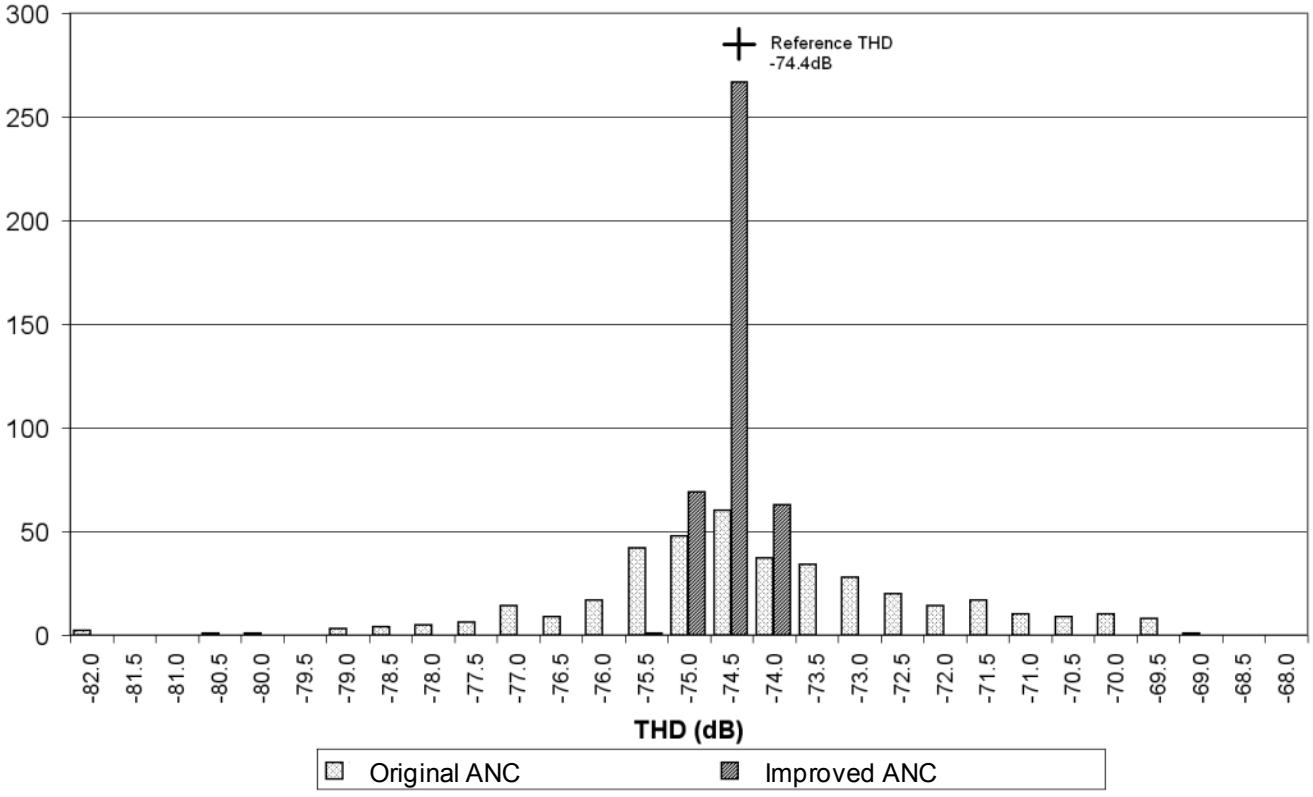

Figure 10: Histogram of THD estimations with original and improved ANC methods for DAC2

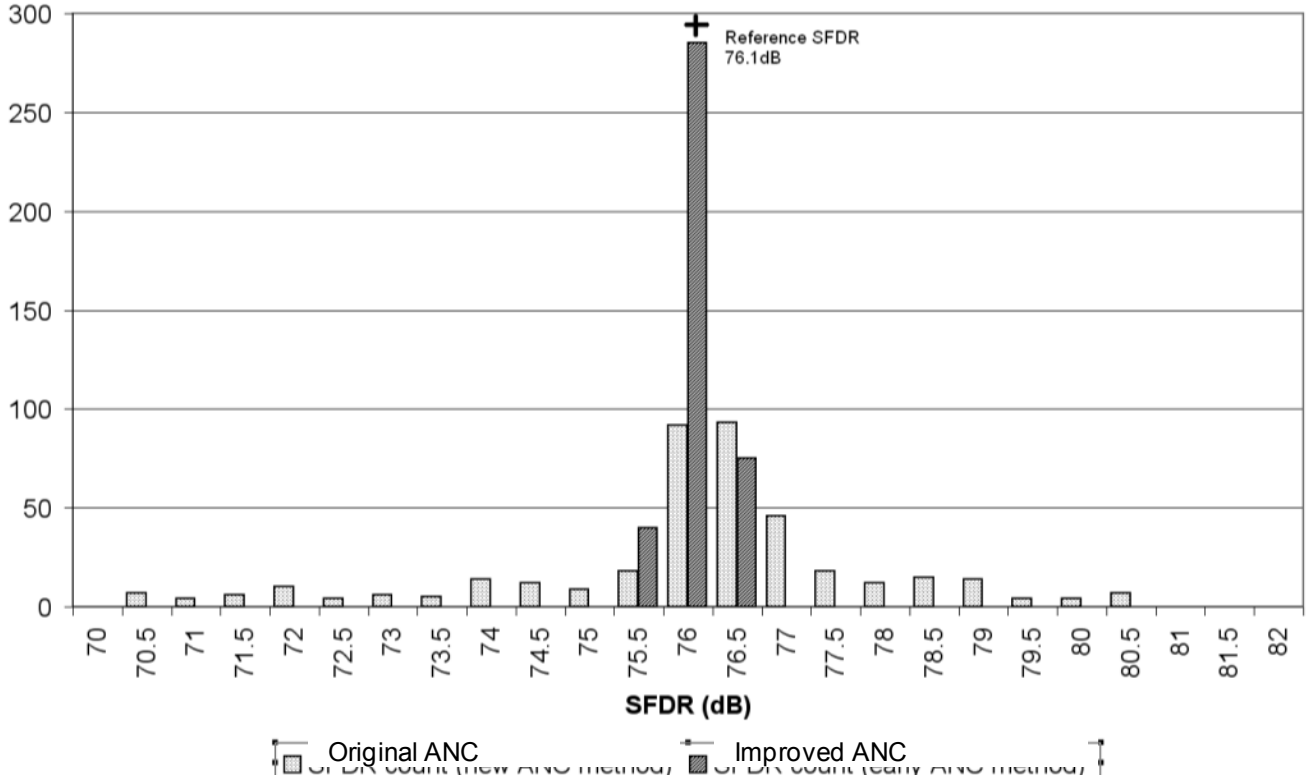

Figure 11: Histogram of SFDR estimations with original and improved ANC methods for DAC2

TABLE I: THD values and estimation errors without phase shift on converters' harmonics

	THD (dB)			Estimation Error (dB)	
	Reference	Original ANC	Improved ANC	Original ANC	Improved ANC
DAC1	-77.9	-77.2	-77.3	0.7	0.6
DAC2	-74.4	-74.1	-74.2	0.3	0.2
ADC	-66.1	-65.8	-65.7	0.3	0.4

TABLE II: SFDR values and estimation errors without phase shift on converters' harmonics

	SFDR (dB)			Estimation Error (dB)	
	Reference	Original ANC	Improved ANC	Original ANC	Improved ANC
DAC1	78.9	79.3	79.3	0.4	0.4
DAC2	76.1	75.6	75.6	0.5	0.5
ADC	70.5	69.8	69.8	0.7	0.7

TABLE III: THD values and estimation errors with a random phase shift injected on converters' harmonics

	THD (dB)			Estimation Error (dB)	
	Reference	Original ANC	Improved ANC	Original ANC	Improved ANC
DAC1	-77.9	-73.6	-77.7	4.3	0.2
DAC2	-74.4	-73.2	-74.4	1.2	0.0
ADC	-66.1	-67.0	-66.2	0.9	0.1

TABLE IV: SFDR values and estimation errors with a random phase shift injected on converters' harmonics

	SFDR (dB)			Estimation Error (dB)	
	Reference	Original ANC	Improved ANC	Original ANC	Improved ANC
DAC1	78.9	76.8	78.8	2.1	0.1
DAC2	76.1	76.6	76.1	0.5	0.0
ADC	70.5	68.5	70.4	2.0	0.1

TABLE V: THD values and estimation errors with phase shift from low-pass filter

	THD (dB)			Estimation Error (dB)	
	Reference	Original ANC	Improved ANC	Original ANC	Improved ANC
DAC1	-82.4	-84.8	-81.6	2.4	0.8
DAC2	-74.4	-76.4	-74.6	2.0	0.2
ADC	-66.1	-65.9	-65.6	0.2	0.5

TABLE VI: SFDR values and estimation errors with phase shift from low-pass filter

	SFDR (dB)			Estimation Error (dB)	
	Reference	Original ANC	Improved ANC	Original ANC	Improved ANC
DAC1	78.4	79.9	78.1	1.5	0.3
DAC2	76.0	78.2	76.0	2.2	0.0
ADC	70.4	69.9	69.7	0.5	0.7

TABLE VII: Summary of THD estimations for random phase delays (standard deviation=π/6)

		Original ANC method			Improved ANC method		
	Ref (dB)	average (dB)	dispersion (dB)	max error (dB)	average (dB)	dispersion (dB)	max error (dB)
DAC1	-77.9	-75.6	10.1	6.7	-77.6	1.8	1.0
DAC2	-74.4	-73.6	13.1	7.9	-74.5	1.3	0.8
ADC	-66.2	-66.9	10.1	9.0	-66.1	1.0	0.6

TABLE VIII: Summary of SFDR estimations for random phase delays (standard deviation=π/6)

		Original ANC method			Improved ANC method		
	Ref (dB)	average (dB)	dispersion (dB)	max error (dB)	average (dB)	dispersion (dB)	max error (dB)
DAC1	78.8	77.8	7.6	6.7	79.0	1.7	1.1
DAC2	76.1	75.9	10.3	5.8	76.0	1.2	0.7
ADC	70.4	70.2	8.2	5.9	70.1	1.5	0.9

TABLE IX: Summary of THD estimations for random phase delays (standard deviation=π)

		Original ANC method			Improved ANC method		
	Ref (dB)	average (dB)	dispersion (dB)	max error (dB)	average (dB)	dispersion (dB)	max error (dB)
DAC1	-77.9	-73.7	16.6	8.9	-77.6	2.6	1.5
DAC2	-74.4	-72.9	20.2	14.4	-74.5	1.3	0.7
ADC	-66.2	-68.0	11.6	10.6	-66.1	0.8	0.5

TABLE X: Summary of SFDR estimations for random phase delays (standard deviation=π)

		Original ANC method			Improved ANC method		
	Ref (dB)	average (dB)	dispersion (dB)	max error (dB)	average (dB)	dispersion (dB)	max error (dB)
DAC1	78.8	75.5	8.4	7.2	78.8	2.2	1.2
DAC2	76.1	75.0	10.5	6.2	76.2	1.3	0.7
ADC	70.4	70.7	10.1	7.4	70.3	1.2	0.6