An Electrical Test Method for MEMS Convective Accelerometers: Development and Evaluation

Ahmed Rekik, Florence Azaïs, Norbert Dumas, Frédérick Mailly, Pascal Nouet

An Electrical Test Method for MEMS Convective Accelerometers: Development and Evaluation

A.A. Rekik[1,2], F. Azaïs[1], N. Dumas[1], F. Mailly[1], P. Nouet[1]

[1] LIRMM - CNRS/Univ. Montpellier 2 - 161 rue Ada, 34392 Montpellier, France
[2] ENIS - University of Sfax - Route Soukra, Cité Elhabib BP W 3052 Sfax, Tunisia

Abstract — **In this paper, an alternative test method for MEMS convective accelerometers is presented. It is first demonstrated that device sensitivity can be determined without the use of physical test stimuli by simple electrical measurements. Using a previously developed behavioral model that allows efficient Monte-Carlo simulations, we have established a good correlation between electrical test parameters and device sensitivity. Proposed test method is finally evaluated for different strategies that privilege yield, fault coverage or test efficiency.**

Keywords: **MEMS testing, convective accelerometer, alternative electrical test**

I.   INTRODUCTION

MEMS testing is a challenging issue due to the multi-domain nature of MEMS devices. They therefore require the application of physical test stimuli to verify their specifications. As a result, MEMS testing requires specific and sophisticated test equipment that is more expensive than standard ATE. An interesting approach is to develop alternative electrical-only test procedures, and numerous solutions have been proposed in the last decade for various types of MEMS such as accelerometers [1-5], magnetic field sensors [6], pressure sensors [7]…

In this paper, we focus on MEMS convective accelerometers. On the one hand, accelerometer testing requires expensive test equipments with movable test heads and long test sequences due to their ability to detect accelerations only in low frequency ranges. On the other hand, literature reports only methods applicable to capacitive sensors [1-5] where electrostatic actuation can be used to implement alternate electrical tests. It is therefore our objective to propose an alternative electrical test method for MEMS convective accelerometers. More specifically, our goal is to develop a motionless test method that can be applied using only electrical test stimuli and that permits to verify device sensitivity, as it is the most challenging specification to measure without applying a calibrated acceleration.

The paper is organized as follows. In section II, we describe the convective accelerometer together with its behavioral model and we introduce a list of parametric faults (mainly due to process scattering) that can affect the device sensitivity. The alternative electrical test method, its implementation and its evaluation are presented in section III and IV, respectively. Finally, evaluation results are discussed in section V.

II.   DEVICE UNDER TEST

A. Device Overview

The device under test is a convective accelerometer obtained by Front-Side Bulk Micromachining (FSBM) of a CMOS die fabricated in a 0.8 µm technology from Austria Microsystems® (Fig.1). Three thin bridges, composed of the CMOS process back-end layers (oxide, polysilicon, aluminum, and nitride), are suspended over a silicon etched cavity and polysilicon is used to embed resistors, for both heating (R_H) and temperature sensing (R_{D1}, R_{D2}). The heater R_H (i.e. central bridge) is biased with an electrical voltage (U_H) to create a hot bubble confined in the bottom (i.e. etched silicon) and top (i.e. package) cavities: the temperature is then maximum at the heater location and minimum at the cavities boundaries. Main lateral dimensions are the half-width of both the heater beam (r_1) and the cavity (r_2), and the distance between the heater and one detector (d).
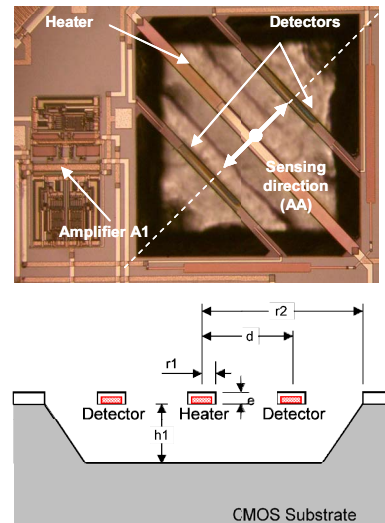

Figure 1.   SEM picture of the prototype and corresponding geometrical parameters: r_1=20µm, r_2=350µm, d=175µm, h_1=270µm, e=5.2µm

In absence of acceleration along the sensor sensitive axis, the temperature of detectors (i.e. lateral bridges: R_{D1}, R_{D2}) are identical for symmetry reasons. Under acceleration along the sensitive axis (AA'), the hot bubble deforms due to free convection and a differential temperature appears between both detectors. Thanks to the Temperature Coefficient of Resistance (*TCR*) of polysilicon, this differential thermal signal implies a

differential resistance variation that converts into a voltage when temperature sensors are arranged in a Wheatstone bridge. This voltage is directly proportional to the acceleration and device sensitivity. For more details on sensor modeling, manufacturing and characterization please refer to previous works from some of the authors [8-10].

B. Device Modeling

For system-level and electronic interface circuit design, a behavioral model of the sensor was developed and implemented in Matlab/Simulink® [10]. This model was further extended in [11] to include the influence of the cavity depth (h_1). It is based on simple equations from fluid physics.
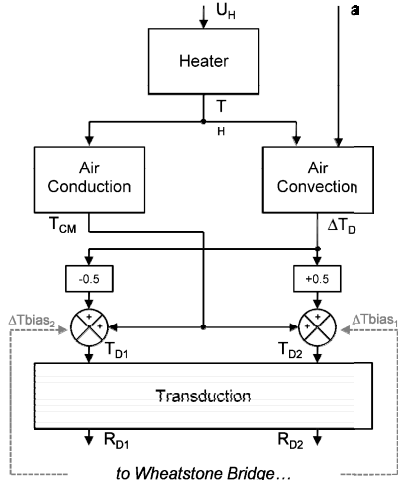

Figure 2. Block diagram of the sensor model

This model, illustrated in Figure 2 is composed of four main blocks:

- First, heater temperature (T_H) is calculated from the external power supply (U_H). The temperature mainly depends on both electrical and thermal resistances of the heater. An analytical expression of the thermal resistance has been derived by solving the Fourier law for heat conduction under the assumption of a radial heat flow in a cylindrical geometry. This expression involves some sensor geometrical dimensions (r_1, r_2, e and h_1), an equivalent radius of the hot bubble, and some physical constants such as air conductivity and its variation with temperature.

- Then, the common mode temperature of detectors, T_{CM} (i.e. temperature measured by detectors without acceleration), is governed by fluid conduction. It is computed from T_H based on same assumption of a radial heat flow in a cylindrical geometry.

- Differential temperature of detectors (ΔT_D) results from fluid convection under an acceleration (a). It is calculated with a semi-empirical expression that involves the heater temperature (T_H) and some geometrical dimensions of the sensor (r_1, r_2, d and h_1). Indeed, the differential temperature resulting from an acceleration is due to free convection and is governed by three coupled differential equations established from

the principle of momentum conservation, mass conservation and energy conservation respectively. This set of equations can be analytically solved only for very simple geometries.

- Finally, regarding electrical transduction, both detector resistances (R_{Di}) are computed from common mode temperature (T_{CM}), differential temperature (ΔT_D), and self-heating (ΔT_{bias}) due to joule effect. Obtained expression involves polysilicon TCR, detectors' electrical resistance at reference temperature (R_{Di0}), and detectors' thermal resistance (Rth_D). Although detectors' thermal resistance depends on detectors and heater temperatures, a fixed value is considered since the self-heating impact on the variation of detectors' temperature is small due to the high value of the detectors' electrical resistance of 50kΩ.

This model has been calibrated with respect to real silicon device and FEM simulations. Model parameters are listed in Table I together with their nominal values. Note that this model is intended to represent the static behavior of the sensor. For dynamic simulations, additional parameters, not given in the table, have been determined: heater and detector thermal capacitances and convection time constant.

TABLE I.   LIST OF MODEL PARAMETERS AND NOMINAL VALUES

Symbol	Nominal parameter values		
	Description	Value	Unit
R_{H0}	Heater electrical resistance	0.35	kΩ
R_{D0}	Detector electrical resistance	50	kΩ
TCR	Resistance temperature coefficient	9×10^{-4}	1/°C
Rth_D	Detector thermal resistance	23,470	K/W
D	Distance between heater and detectors	175	µm
r_1	Heater beam half-length	20	µm
r_2	Distance between heater and cavity border	350	µm
E	Heater beam thickness	5.2	µm
h_1	Cavity depth	270	µm

C. Fault Model

Sensor behavioral model can be efficiently used to perform fault simulation. In particular, effect of process scattering can be implemented through dispersions on model parameters. Note that the effect of catastrophic defects, such as a broken structure, can also be easily included in the model. It can be simply modeled as an open circuit on the corresponding detector or heater, which is classically represented by a resistance of very high value (more than 1MΩ).

In this work, we focus only on parametric faults due to process scattering. Indeed, catastrophic faults are easy to detect. Moreover, we have shown in [12] that, under single fault assumption, most of the parametric faults can be detected by simple electrical test measurements. However, assuming a single parametric fault is not a realistic. Therefore, we consider multiple faults with the following dispersions on model parameters:

- A Gaussian distribution with 3σ=20% for electrical resistances, i.e. the heater resistance R_{H0}, the detectors'

resistance R_{Di0}, and the reference resistances R_{REFi}. This distribution corresponds to typical uncertainties given by the foundry and is a global variation, i.e. it affects all resistances in the same amount.

- A Gaussian distribution with $3\sigma=2\mu m$ for geometrical parameters related to horizontal dimensions, i.e. the heater half-width r_1 and the distance r_2 between the heater and the boundary of the cavity. Indeed, lateral dimensions are parameters that are rather well controlled during the manufacturing process and, therefore, they exhibit a low dispersion. Note that the distance d between the heater and the detectors is not subject to process variations as this distance is set by a single mask and thus not subject to mask misalignments.
- A Gaussian distribution with $3\sigma=10\%$ for *TCR* has been chosen as it is well-known that this parameter is quite sensitive to doping fluctuations.
- A random uniform variation of cavity depth h_1 between $35\mu m$ and $490\mu m$. Indeed, contrary to lateral dimensions, the cavity depth is a parameter that is very difficult to control. In particular, it is very sensitive to the etching post-process (etching solution composition, etching time and etching solution movements). As the optical control is not an easy task during etching, the cavity depth is likely to be reduce if ideal conditions are not met during etching.

Possible asymmetries have also been introduced in the model. In particular, a mismatch error with $3\sigma=2\%$ has been considered for the nominal value of detectors' electrical resistance R_{Di0} and for reference resistance R_{REFi}.

III. ALTERNATIVE ELECTRICAL TEST METHOD

A. Analysis of sensor physical behavior

To establish an alternate test, we need to identify a test parameter, strongly correlated with device sensitivity, which can be electrically measured. In this objective, a preliminary analysis of sensor physical behavior is worth of interest.

Sensor operating principle relies on the biasing of the heater, which creates a hot bubble within the cavity due to air conduction. Due to free convection, the hot bubble deforms under the application of a given acceleration along the sensitive axis. So clearly, the temperature, size and shape of the hot bubble have a direct influence on device sensitivity. Heater temperature depends on power dissipation, whereas both size and shape of the hot bubble depend on both size and shape of the cavity. Lateral dimensions of the cavity are fixed by design and are well controlled during manufacturing. In contrast, cavity depth depends on the etching post-process, which is much more difficult to control. Consequently, we can expect that the cavity depth is the key parameter that will influence device sensitivity.

In this context, it is interesting to analyze the effect of the cavity depth on both conductive and convective behaviors of the device. Figure 3 reports differential temperature $\Delta T_D/2$ and common mode temperature T_{CM} of detectors versus cavity depth h_1, for a fixed heater temperature $T_H=550K$. Results are given for an acceleration of 1g along the sensitive axis and for the nominal distance $d=175\mu m$.
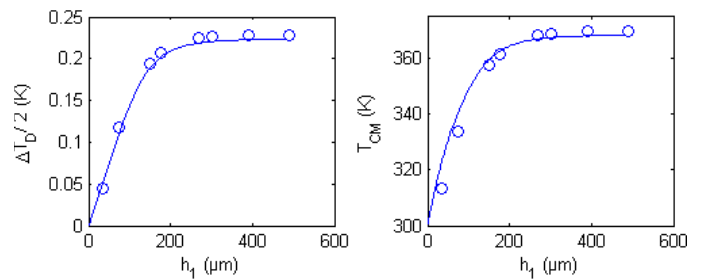

Figure 3. Differential temperature $\Delta T_D/2$ and common mode temperature T_{CM} vs. cavity depth (solid line: model, dots: FEM)

In both cases, two regions can be distinguished: (i) for high values of cavity depth, both differential and common mode temperatures are almost constant, and (ii) for low values of cavity depth, both differential and common mode temperatures reduce when the cavity depth decreases. The transition between both regions occurs around $h_1=175\mu m$. This phenomenon can be explained by analyzing the impact of h_1 on the hot bubble size. When the cavity depth is high enough, the lateral silicon walls of the cavity limit the size of the hot bubble which is therefore not affected by the value of the cavity depth. In contrast, for low values of the cavity depth, this parameter becomes the limiting factor and the size of the hot bubble tends to reduce, thus reducing both differential and common mode temperatures.

The interesting point of this analysis is that differential and common mode temperatures present very similar behaviors with respect to variations of cavity depth. As illustrated in figure 4, it exits a strong correlation between both temperatures [11]. This is really worthy of interest in the objective of an alternate electrical test method. Indeed, the only way to measure a detectors' differential temperature is to apply a given acceleration. In contrast, it is just necessary to bias a device to obtain a common mode temperature. Therefore, verifying the common mode temperature in absence of acceleration may be a way to verify device sensitivity to a given acceleration.
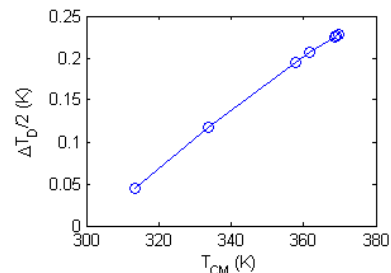

Figure 4. Differential temperature ($\Delta T_D/2$) due to a 1g acceleration vs. common mode temperature (T_{CM}) for different depth of the cavity

B. Electrical test parameters

The objective is to determine a set of electrical test parameters that are correlated with detectors' common mode temperature. The correlation of common mode temperature with device sensitivity will then allow to calibrate tested accelerometers. One obvious parameter is the equivalent impedance of the Wheatstone bridge. It can be easily measured with simple I/V measurements. However, as illustrated in figure 5, Monte-Carlo simulation (performed on 5,000 runs)

shows that there is no correlation between the equivalent impedance of the Wheatstone bridge and device sensitivity.
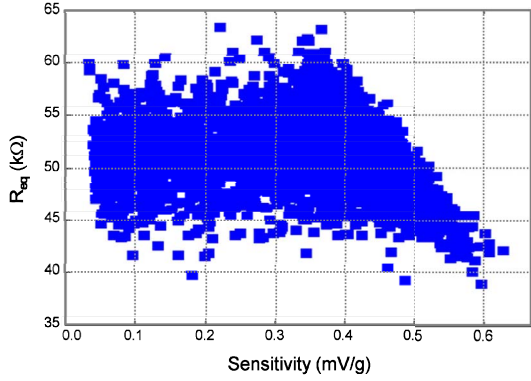

Figure 5.   Equivalent impedance of the Wheatstone bridge (R_{eq}) vs. device sensitivity

This can be easily explained by studying the impact of the common mode temperature of detectors, T_{CM}, on the equivalent impedance of the Wheatstone bridge that can be expressed as:

$$R_{eq} = \frac{(R_{D1} + R_{REF1}) * (R_{D2} + R_{REF2})}{(R_{D1} + R_{REF1}) + (R_{D2} + R_{REF2})} \quad (1)$$

Neglecting process variations and mismatch in a first approximation ($R_{Di0} = R_{REFi0} = R_{D0}$), we can introduce the temperature sensitivity of detectors' resistance as $R_{Di} = R_{D0}(1 + TCR.\Delta T_{CM})$ where TCR is the resistance temperature coefficient and ΔT_{CM} is the difference between T_{CM} and reference resistors' temperature, i.e. substrate temperature or ambient temperature. Eq. (1) can then be re-arranged as:

$$R_{eq} = R_{D0}\left(1 + \frac{1}{2} \cdot TCR \cdot \Delta T_{CM}\right) \quad (2)$$

Taking into account the temperature sensitivity of polysilicon $TCR = 0.9 \ 10^{-3} \, K^{-1}$, we can calculate, from equation (2), an increase of 0.45% of the equivalent resistance of the Wheatstone bridge for a 10K increase of the common mode temperature. This variation is obviously negligible compared to the dispersion of resistors' nominal value R_{D0} which induces an uncertainty on Wheatstone bridge equivalent impedance ($3\sigma = 20\%$). Therefore, the equivalent impedance must be considered as a differential signal. The idea is to evaluate the relative deviation of the equivalent impedance of the Wheatstone bridge for two different biasing conditions. More precisely, we propose to first measure the equivalent impedance of the Wheatstone bridge for a nominal biasing of the heater resistance ($U_H = 2V$), and then at reference temperature ($U_H = 0V$). In the latter case, equivalent impedance of the Wheatstone bridge R_{eq0} is directly equal to the detector electrical resistance R_{D0} (neglecting again mismatch). The relative deviation of Wheatstone bridge equivalent impedance $\Delta R_{eq}/R_{eq0}$ is therefore given by:

$$\frac{\Delta R_{eq}}{R_{eq0}} = \frac{R_{D0}\left(1 + \frac{1}{2} \cdot TCR \cdot \Delta T_{CM}\right) - R_{D0}}{R_{D0}} = \frac{1}{2} \cdot TCR \cdot \Delta T_{CM} \quad (3)$$

From equation (3), it is obvious that process variations that affect nominal value of the polysilicon resistance will not impact the differential measurement of equivalent impedance. It could be also demonstrated that mismatches that affect the four resistors independently only have a small impact on the differential Wheatstone bridge's impedance variation. As analytical expressions are rather complex, this is demonstrated through Monte-Carlo simulations, as illustrated in figure 6 where a quite good correlation is observed between relative deviation of the Wheatstone bridge equivalent impedance and device sensitivity.
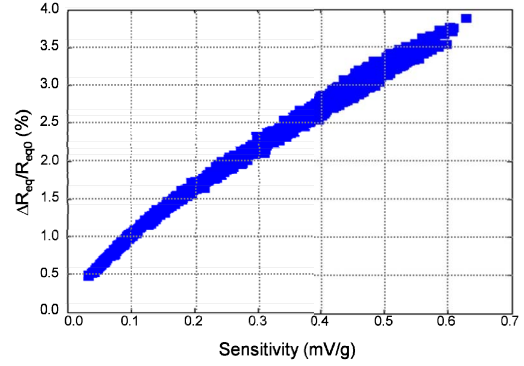

Figure 6.   Relative deviation of Wheatstone bridge's equivalent impedance ($\Delta R_{eq}/R_{eq0}$) vs. device sensitivity

C. Electrical test procedure

From previous analysis, relative deviation of the Wheatstone bridge's equivalent impedance arises as an interesting alternative Test Parameter (TP) in the objective of a low-cost electrical test solution. Moreover, measurement of this test parameter is very simple, for instance from measurement of the current flowing through the Wheatstone bridge.
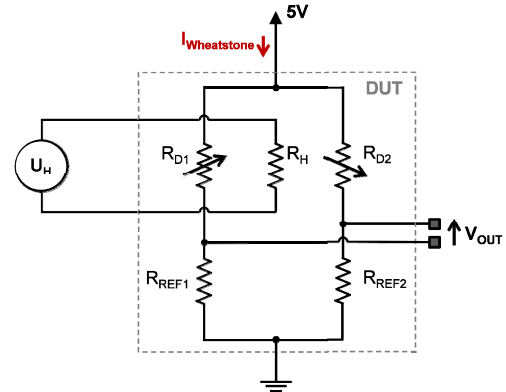

Figure 7.   Electrical test setup

Consequently, we propose an alternative test procedure that can be implemented with a very simple electrical test setup (see figure 7), which involves three steps:

1.   Measure $I_{Wheatstone}$ for $U_H = 2V$, I_{W1}

2. Measure $I_{Wheatstone}$ for U_H=0V, I_{W0}

3. Compute $\Delta R_{eq}/R_{eq0} = (I_{W0}/I_{W1}-1)$ and compare with predefined Tolerance Limits (*TL*) to classify tested device as a fault-free or a faulty one.

IV. TEST IMPLEMENTATION & EVALUATION

Overall quality of alternate tests strongly depends on the accuracy of tolerance limits applied to test parameters. A possible approach to determine tolerance limits *TL* is to use Monte-Carlo simulations as previously proposed in the literature [13]. In an ideal situation, fault-free and faulty circuits would exhibit clearly separated distributions with respect to test parameters (Figure 8.a). It is then very easy to define tolerance limits; however, it is more likely to appear that both distributions overlap (Figure 8.b). In this realistic case, five different zones can be defined:

- Zone 1 that contains only bad circuits: $TP < TL_{minA}$,
- Zone 2 that contains both bad and good circuits: $TL_{minA} < TP < TL_{minB}$,
- Zone 3 that contains only good circuits: $TL_{minB} < TP < TL_{maxB}$,
- Zone 4 that contains both bad and good circuits: $TL_{maxB} < TP < TL_{maxA}$,
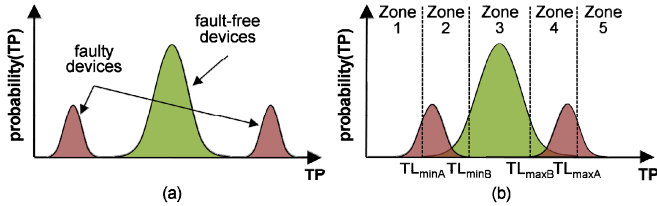- Zone 5 that contains only bad circuits: $TP > TL_{maxA}$.

Figure 8. Distribution of fault-free and faulty devices verus test parameters (a) ideal case (b) realistic situation

Obviously, tolerance limits TL_{min} and TL_{max} have to be set between TL_{minA} and TL_{minB}, and TL_{maxB} and TL_{maxA}, respectively. Three different strategies may be considered:

- Strategy #1: Reject all faulty circuits at the price of some yield loss. This approach privileges fault coverage. In this case $TL_{min}=TL_{minB}$ and $TL_{max}=TL_{maxB}$.
- Strategy #2: Accept all good circuits at the price of faulty circuit acceptance (test escape). This approach privileges yield. In this case $TL_{min}=TL_{minA}$ and $TL_{max}=TL_{maxA}$.
- Strategy #3: A compromise between both previous options. In this case TL_{min} can be chosen between TL_{minA} and TL_{minB}, and TL_{max} can be chosen between TL_{maxB} and TL_{maxA}. This approach is used to optimize test efficiency.

The performances of these different options can be evaluated trough Monte-Carlo simulations considering following metrics:

- Fault Coverage (*FC*): number of faulty circuits correctly rejected by alternate tests relatively to the total number of faulty circuits,

- Yield Loss (*YL*): number of good circuits erroneously rejected by alternate tests relatively to the total number of good circuits,

- Test Efficiency (*Eff*): number of good decisions taken relatively to the total number of circuits in the considered population.

V. EVALUATION RESULTS

The proposed alternative test method has been evaluated with respects to the previously defined metrics. Tolerance limits have been determined by studying a population of 5,000 devices generated with Monte-Carlo simulations considering the dispersions defined in section II.C.

We have defined acceptable devices as those with a sensitivity in a range of ±10% around the nominal sensitivity of the studied design (S_{nom}=0.43mV/g). Consequently, 50% of the generated devices are fault-free (Figure 9.a). Regarding the distribution of alternate test parameter (Figure 9.b), as expected, there is an overlap between the distribution of fault-free and faulty circuits. From this overlap, we obtain TL_{minA}=0.0254, TL_{minB}=0.0273, TL_{maxB}=0.0297 and TL_{maxA}=0.0322.
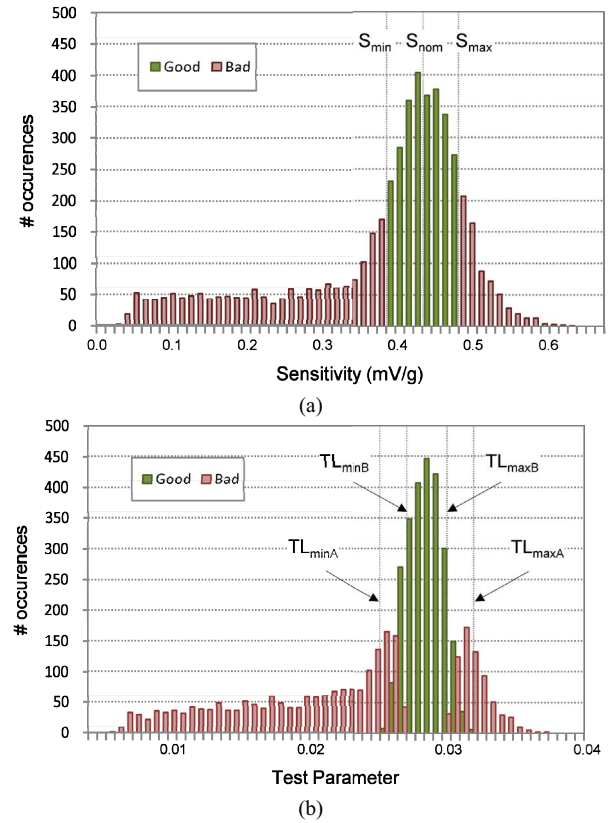

Figure 9. Distribution of (a) device sensitivity and (b) alternate test parameter for a population of 5,000 devices.

We have then evaluated *FC*, *YL* and *Eff* for the three different strategies previously reported to set tolerance limits (Figure 10). For strategy #3, minimum and maximum values of tolerance limits have been set independently to maximize *Eff* as follows. To determine TL_{min}, the tolerance limit TL_{max} is first set to any value between TL_{maxB} and TL_{maxA}. TL_{min} is then swept

between TL_{minA} and TL_{minB} and TL_{min} is set to the value that maximizes the number of good decisions (TL_{min}=0.0264 in our case). Applying a similar procedure for TL_{max}, we obtained TL_{max}=0.0310.
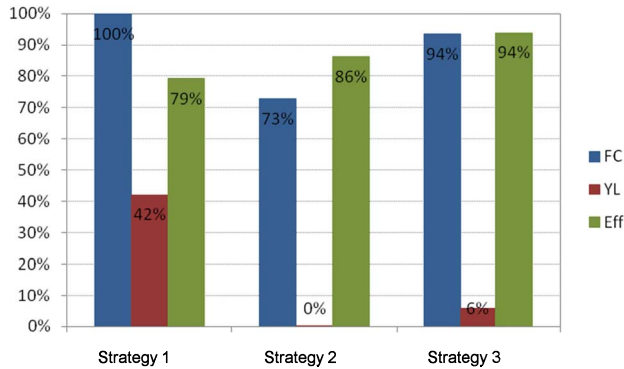

Figure 10. Alternative Test Method Metrics

Analyzing these results, it appears that Strategy #1 that privileges fault coverage is not really a viable option. Indeed, despite a rather good test efficiency of 79%, a high number of good circuits are rejected. The maximum fault coverage of 100% is therefore achieved at the price of a prohibitive yield loss of 42%. Strategy #2 that privileges production yield presents better performances. In this case all good circuits are accepted, which means no yield loss, and 73% of the faulty circuits are rejected. Finally, Strategy #3 that maximizes the number of good decisions of the alternative electrical method also leads to interesting results, with a test efficiency that increases up to 94%. This option leads to good fault coverage up to 94% while only 6% of good circuits are rejected.

From previous results, we can define two global test approaches with respect to targeted product quality:

- For low-end products, where test costs may be prohibitive for the market, Strategy #2 or Strategy #3 could be used to select elementary dies on a wafer that would go to packaging (depending on the relative cost of packaging with respect to the cost of a naked die). After packaging, a final test with a tilting table can then be used to verify ±1g output signal since it was demonstrated that final device performances depend on the package [14].

- For high-end products, where product quality is important, Strategy #3 should be preferred and associated with a more expensive final test using a shaker to verify the full range of the sensor.

VI. CONCLUSION

In this paper, we have proposed an alternative electrical test solution for MEMS convective accelerometers. It is based on measurement of the relative deviation of the Wheatstone bridge equivalent impedance for two different biasing conditions of heater resistance. The electrical test setup and the associated test procedure are extremely simple, therefore offering a low-cost test solution. Performances of the technique have been evaluated through Monte-Carlo simulations considering three

metrics: fault coverage, yield loss and test efficiency. Depending on tolerance limits, different tradeoffs are achieved between test coverage, yield loss or test efficiency.

It should be noted that results presented in this paper have been obtained through Monte-Carlo simulations considering arbitrary process dispersions. In this case, the generated population may not be completely realistic, and consequently fault coverage and yield loss numbers should not be considered as absolute figures, but just as an indicator on how to set tolerance limits for the test parameter to optimize test efficiency with respect to the targeted product quality. Indeed, studied accelerometer is not currently fabricated in large volume and thus silicon data are not available at that time. If this test strategy is applied in the future to a real product, silicon data would be used to improve tolerance limits towards better test efficiency.

Future work concerns the detailed analysis of faulty circuits that escape the alternate test procedure in strategy #2 and #3 to identify additional electrical test parameters that would permit to improve test efficiency without degrading yield loss.

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