Calibrating Bulk Built-in Current Sensors for Detecting Transient Faults

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***Abstract* – This work presents a novel circuit for detecting transient faults in combinational and sequential logic. The detection mechanism features a built-in current sensor connected to the bulks of the monitored logic. The proposed circuit was optimized in terms of power consumption and enhanced with low-power sleep-mode. In addition, a calibration method for bulk built-in current sensors is presented. Overhead results indicate an increase of only 15% in power consumption which represents an improvement of almost factor 6 compared to similar existing sensor.**

Keywords – built-in current sensors; transient faults; soft errors; fault attacks; concurrent error dectection schemes

I. INTRODUCTION

Higher error resilience is expected from an increasing number of integrated systems while, at the same time, ultra-deep submicron technologies make these systems more and more sensitive to natural aging processes or environment sources like radiations from cosmic origin or every day material [1]. In addition to these natural phenomena, malicious fault-based attacks can be used to bypass security mechanisms of secure systems and extracting information on confidential data [2]. Both these natural or malicious phenomena on integrated circuits can induce transient effects that provoke bit-flips of stored results during the system lifetime.

Until the early 2000's, researches on transient faults focused essentially on memory elements, which were considered the system's most vulnerable circuits. Many concurrent error detection and/or correction mechanisms were proposed to mitigate soft errors induced by transient faults in memory cells. In the last decade, however, more sensitive deep-submicron technologies as well as the increasing demand in terms of digital security have also pushed for the development of countermeasures against transient faults in combinational parts of the circuits. These faults indeed can propagate up to storage elements and thus cause soft errors as well. On the other hand, if the transient fault does not induce any error due to an electrical, logical or latching-window masking effect, its detection is crucial all the same in secure applications since the fault itself reveals an attempt of attack.

Coping with transient faults by using mitigation techniques at different abstraction levels of the design is today the trend in order to efficiently protect integrated systems [3][4]. The idea behind is the avoidance of costly fault-tolerance mechanisms like tripe modular redundancy, taking advantage of cheaper mitigation techniques that ensure satisfactory soft-error coverage for the system's most recurrent operations. This modern strategy is exemplified through system's recovery schemes fired in function of the indication of concurrent error detection (CED) circuitries.

CED mechanisms designed at transistor or gate level guarantee an early detection, as soon as the faults happens, preventing more critical failure scenarios such as the induction and propagation of multiple errors to other clock cycles, stages, or parts of the system. In case of misbehavior, the generated error flag is able to activate, for instance, recovery machines already implemented in modern systems for dealing with branch misprediction [3][4]. Thereby, faulty operation can be repeated in fault-free conditions, adapting the system to perform again its normal computational sequence.

This paper proposes a new low-cost CED scheme that efficiently identifies transient faults. The proposed circuit monitors transistors' bulks of system's blocks such as similar existing bulk built-in current sensor (BBICS) [5][6]. Our solution, though, is optimized to satisfy today's need for low-power transient-fault robust systems. More precisely, to the best of our knowledge, the innovative contributions of this paper are: (1) an optimization of the original BBICS's circuitry [5][6] to achieve reasonable overheads in power consumption; (2) the introduction of the sleep-mode for BBICS that allows additionally energy savings when the system is on standby; (3) a calibration method defined at design time for BBICS detecting a minimum profile of transient fault.

II. BUILT-IN CURRENT SENSORS DETECTING TRANSIENT FAULTS

Built-in current sensors (BICS) were initially proposed as a mechanism for detecting large increases in the current I_{DDQ} consumed by a CMOS circuit during its quiescent state, i.e. when the circuit is not switching. The mechanism allows thus testing CMOS circuits against permanent faults [7]. Further, BICS were also adapted for detecting transient faults in memory cells (i.e. bit-flips) [8][9][10][11]. Recently, efforts were made for monitoring transient faults in combinational logic as well [12]. All these techniques connect BICS to the power lines (V_{DD} and GND) of the monitored circuit in order to distinguish anomalous transient currents from normal currents. The today's problem is that the amplitude of transient currents induced by radiation effects or fault attacks can have the same order of currents normally generated by switching activities in combinational logic circuits. Hence, schemes monitoring power lines are very limited for detecting just small range of transient faults.

On the other hand, BICS connected to the bulks of the

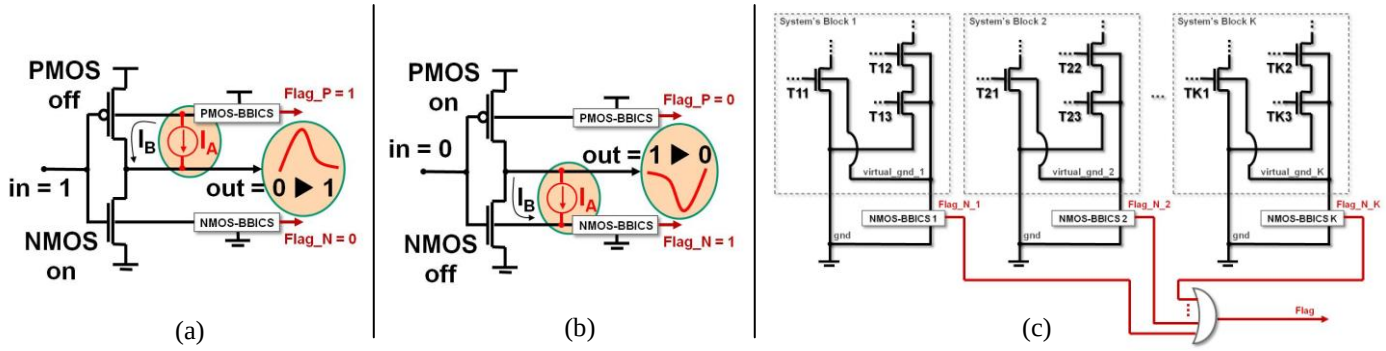

Figure 1. The two cases of transient faults in a CMOS inverter perturbed by an anomalous current "I_A" in (a) and (b), and "K" blocks of a system protected by "K" BBICS in (c)

monitored circuit's transistors are able to detect a wide range of transient faults [5][6][13]. As Fig. 1 (a) and (b) illustrate, Bulk-BICS (BBICS) identify anomalous transient currents I_A flowing through the junction between a bulk and a reversely-biased drain of a perturbed transistor (MOSFETs "off" in Fig. 1). BBICS indeed take advantage of two facts:

(1) In fault-free scenarios (i.e. $I_A = 0$) the bulk-to-drain (or drain-to-bulk) current I_B is negligible even if the MOSFET is switching in function of new input stimuli; and

(2) During transient-fault scenarios, I_A is much higher than the leakage current flowing through the junction.

The range of detectable transient faults is easily adjustable by calibrating the size of the transistors that constitute the BBICS. Hence, schemes based on BBICS can be designed to latch a flag of fault indication for abnormal currents within a defined range that represents a risk of resulting in soft errors.

Fig. 1 (c) summarizes the strategy for protecting system's blocks against transient faults in pull-down network by using BBICS. Equivalent strategy must be taken for detecting transient faults in pull-up network as well. Note that in such a strategy the connection between the monitored circuit (e.g. system's block 1) and the BBICS's circuitry (e.g. NMOS-BBICS 1) is done via metal – from the body-ties of each monitored transistor (e.g. T11, T12, and T13) up to the input of the BBICS's circuitry. Thereby, the peak of the anomalous transient current (i.e. the transient fault) is almost not attenuated, ensuring thus an efficient detection [13]. In fact, this very small attenuation is a function of the local distance between the struck zone of the monitored transistor and its body-tie.

The work in [3] show that area overheads imposed by BBICS's mechanisms for protecting adder circuits can be up to 13.4 % without impact on the system's operating frequency. The costs therefore are considerably smaller than the ones due to classic CED schemes [14]. Moreover, BBICS approach is much more efficient for dealing with transient faults of long duration and multiple faults. Nevertheless, the negative issue of existing BBICS is the elevated power consumption to provide high detection sensitivity in ultra-deep submicron technologies [5][6][15].

III. THE PROPOSED BBICS CIRCUIT

The circuit of our sleep-mode improved bulk built-in current sensor is presented in Fig. 2 (a). If the mode of operation is identical to the original BBICS's circuit [6] shown in Fig. 2 (b), our structure is optimized in such a way that the power consumption could be largely reduced.

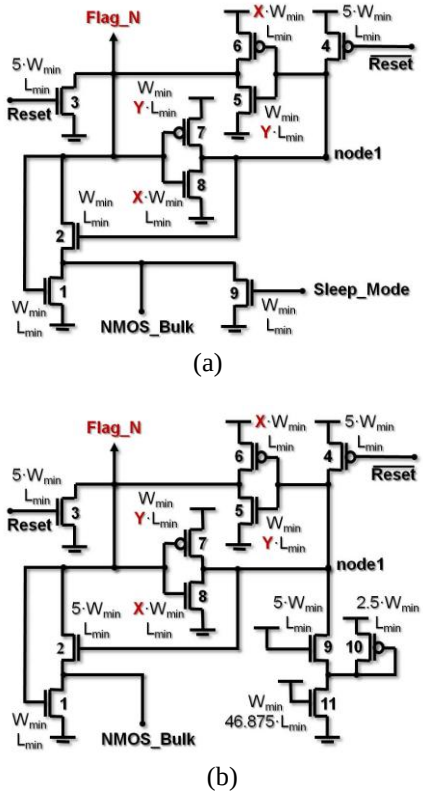

Figure 2. The proposed NMOS sleep-mode improved BBICS's circuit "sibbics_esref2012" in (a) and the original NMOS-BBICS version "bbics_tns2008" [6] in (b)

The NMOS-BBICS's basic structure in Fig. 2 is composed of a latch (transistors 5, 6, 7, and 8) that is responsible for amplifying the anomalous transient currents coming from the bulk "NMOS_Bulk" of the monitored block (e.g. "virtual_gnd_1" of system's block 1 in Fig. 1 (c)). Higher gain of amplification is obtained by increasing design factors X and Y, hence higher BBICS's sensitivity in detecting transient faults is also determined in terms of these design factors.

BBICS's latch has, moreover, the function of memorizing a flag in case of a transient fault within a defined current range – i.e. "Flag_N" in Fig. 2 keeping V_{DD} level. On the other hand, as

soon as the flag of fault is processed by higher instances of the system, BBICS's latch must be reset (through the input "Reset" in Fig. 2) in order to detect other transient faults.

Our solution for reducing the static power consumption is introducing transistor 9 such as illustrated in Fig. 2 (a). It allows the utilization of a sleep-mode when the system is left on standby. Transistor 9 is, in this case, set "on", making a less resistive path between the node "NMOS_bulk" and GND. Consequently, the gate-source voltages of transistors 6 and 8 approach to zero, the sub-threshold leakage currents becomes much lower, and thus the static power consumption is drastically reduced. Furthermore, based on simulation experiments, we identified that the costly transistors 9, 10, and 11 from original BBICS in Fig. 2 (b) are not necessary to efficiently and quickly detect short and long duration transient faults in a 32-nm CMOS technology [16].

IV. METHOD FOR CALIBRATING BBICS

Previous section defines the two factors named X and Y in Fig. 2 that allows calibrating the amplification of the anomalous transient current, and thus, adjusting the BBICS's sensitivity in detecting transient faults. This section defines a calibration method that searches, at design time and in function of X, for the smallest and the largest Y able to detect a minimum transient-fault profile.

In order to discover these factors Y_{max} and Y_{min}, several electrical-level simulations under a single-transient fault injection are performed. After the set of simulations, if the sensor is designed with a Y lesser than Y_{min}, a flag is not able to be latched, and then a transient fault cannot be detected. Otherwise, if the sensor is designed with a Y greater than Y_{max}, a flag is always latched, and thus a transient fault or any other event is not capable to be identified. This calibration method, therefore, allows finding, for any technology, the optimal BBICS's design factors within a range between Y_{max} and Y_{min}.

V. RESULTS AND CONCLUSIONS

Transistor-level simulations were performed for comparing our Sleep-mode Improved BBICS named "sibbics_esref2012" with the previous BBICS labelled as "bbics_tns2008". The circuit versions were designed with VDD of 0.9V and in nominal conditions of a 32-nm CMOS technology based on the Predictive Technology Model (PTM) [16].

Fig. 3 shows the increase in power consumption of a case-study circuit (10 chains of 10 inverters) in which all its transistors are monitored by BBICS. The 200 transistors of the chains were designed with minimum size to analyze the technology's smallest capacitances, which represent the most sensitive nodes. Thus, this case-study circuit allows inducing the smallest profiles of transient fault as well as evaluating the minimum sensitivities of the BBICS. We can conclude from Fig. 3 that "bbics_tns2008" versions present large power consumption overhead for any value of X. On the contrary, the proposed "sibbics_esref2012" versions have very lower power consumption, which is additionally reduced during sleep-mode. Note that the results allow defining the minimum and maximum increases since our calibration method searches for the smallest and the largest possible Y.

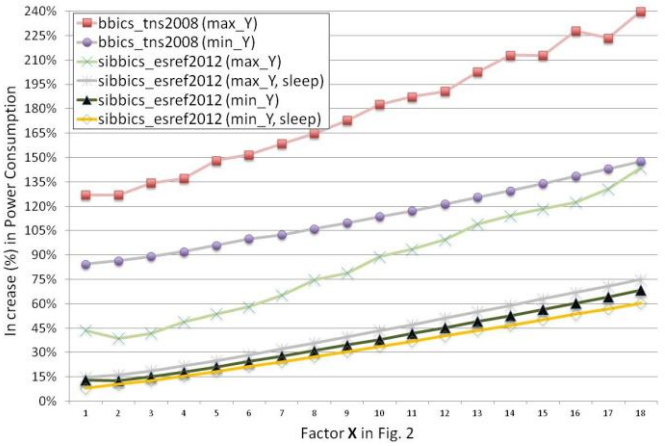

Figure 3. Increase in power consumption due to the implementation of NMOS-BICS and PMOS-BICS versions for monitoring a case-study circuit composed of 100 NMOS and 100 PMOS

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