tLIFTING: A Multi-level Delay-annotated Fault Simulator for Digital Circuits
Giorgio Di Natale, Marie-Lise Flottes, Feng Lu, Bruno Rouzeyre

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**tLIFTING**  
*A Multi-level Delay-annotated Fault Simulator for Digital Circuits*

**Characteristics**
- Mixed-mode multi-level simulation:  
  - 0-delay gate-level  
  - delay-annotated gate-level  
  - transistor-level  
- Fault types:  
  - Single/Multiple Event Transient (SET/MET)  
  - Single Event Upset (SEU) / Multiple Bit Upset (MBU)  
- Stuck-at  
- Electrical behavior modeling

**Applications**
- Fault simulation:  
  - Single/Multiple Event Transient (SET/MET)  
  - Single Event Upset (SEU) / Multiple Bit Upset (MBU)  
- Stuck-at  
- Secure circuits: fault attacks  
- Fault attacks (Laser, EM, ...)  
- Evaluation of countermeasures  
- Reliability evaluation

**ARCHITECTURE of tLIFTING FAULT SIMULATOR**

**MULTIPLE LEVEL FAULT SIMULATION PROCESS**

1. **With delay**
   - Step 1: **Whole circuit**  
     Logic-level simulation without delay from start to the first rising edge before fault injection
   - Step 2: **Whole circuit**  
     Logic-level simulation with delay from the first rising edge before fault injection to the first rising edge after fault injection
   - Step 3: **Sub-circuit**  
     Transistor-level fault simulation with fault model
   - Step 4: **Whole circuit**  
     Logic-level fault simulation with delay
   - Step 5: **Whole circuit**  
     Logic-level simulation without delay for the remaining time

2. **Without delay**
   - Step 1: **Whole circuit**  
     Logic-level simulation without delay from start to the first rising edge before fault injection

**CONTACTS:** giorgio.dinatale@lirmm.fr; flottes@lirmm.fr; feng.lu@lirmm.fr; rouzeyre@lirmm.fr