tLIFTING : A Multi-level Delay-annotated Fault Simulator for Digital Circuits

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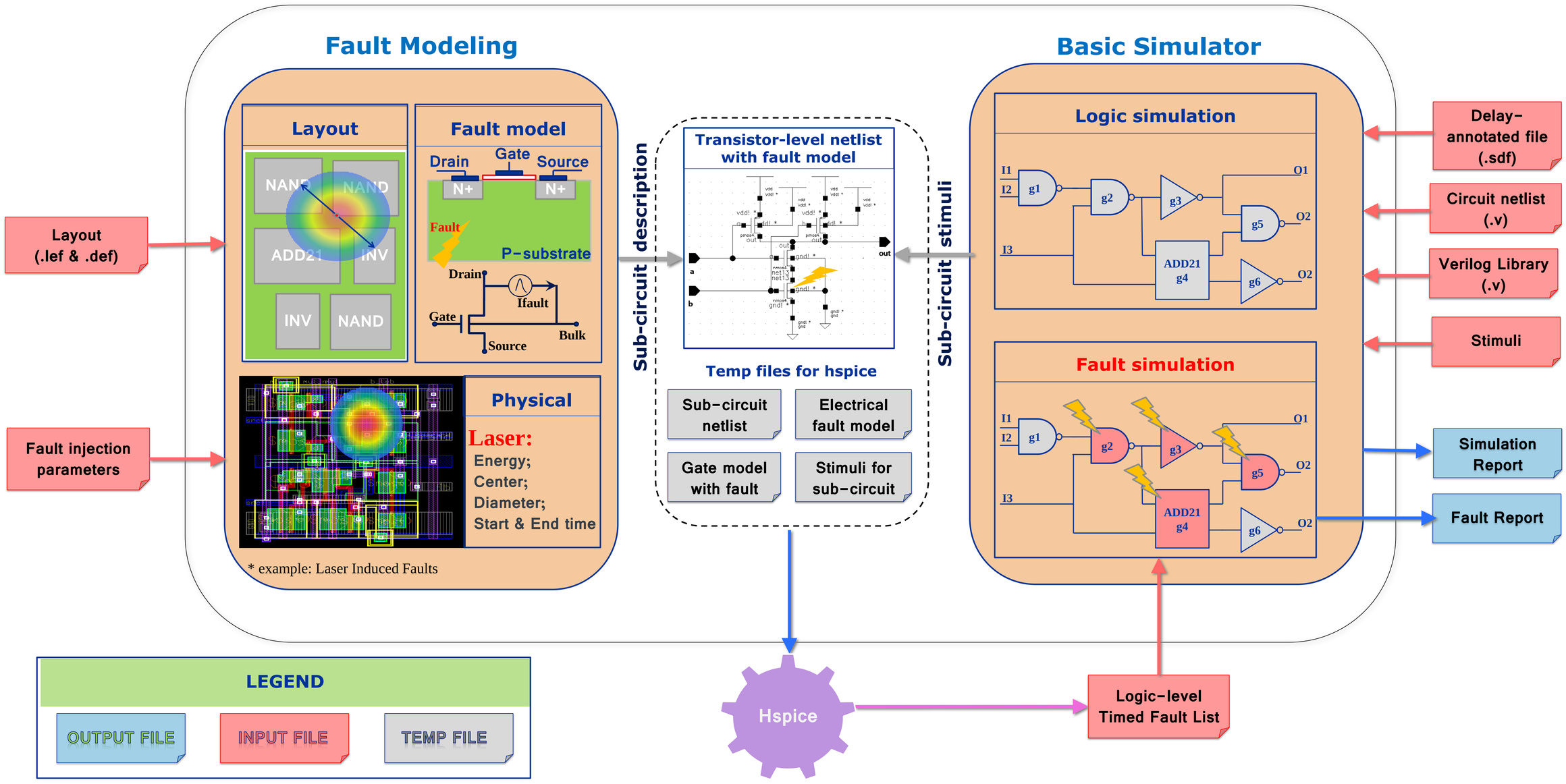
Characteristics

- **Mixed-mode multi-level simulation:**
  - **0-delay gate-level**
  - **delay-annotated gate-level**
  - **transistor-level**
- **Fault types:**
  - **Single/Multiple Event Transient (SET/MET)**
  - **Single Event Upset (SEU) / Multiple Bit Upset (MBU)**
  - **Stuck-at**
- **Electrical behavior modeling**

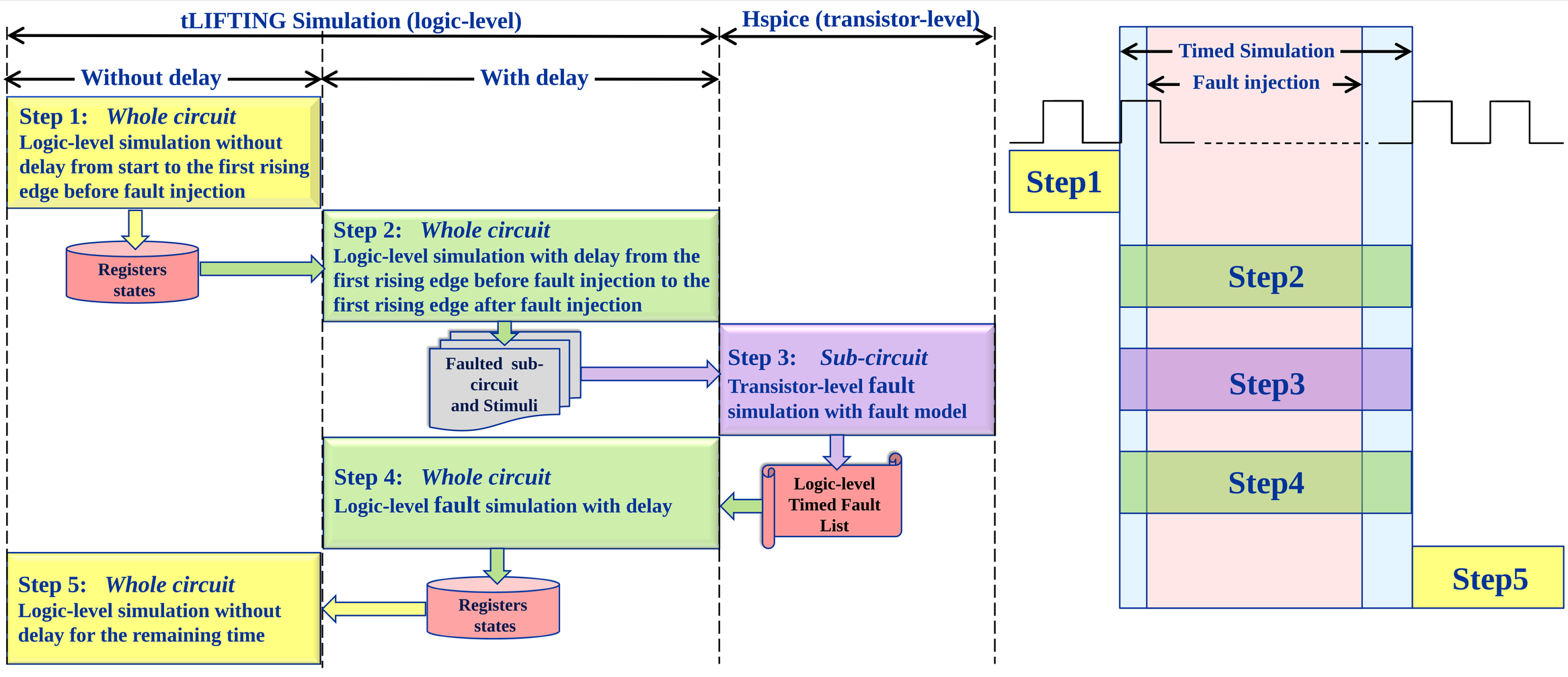
Applications

- **Fault simulation:**
  - **Single/Multiple Event Transient (SET/MET)**
  - **Single Event Upset (SEU) / Multiple Bit Upset (MBU)**
  - **Stuck-at**
- **Secure circuits: fault attacks**
  - **Fault attacks (Laser, EM, ...)**
  - **Evaluation of countermeasures**
- **Reliability evaluation**

ARCHITECTURE of tLIFTING FAULT SIMULATOR



MULTIPLE LEVEL FAULT SIMULATION PROCESS



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