



HAL
open science

tLIFTING : A Multi-level Delay-annotated Fault Simulator for Digital Circuits

Giorgio Di Natale, Marie-Lise Flottes, Feng Lu, Bruno Rouzeyre

► **To cite this version:**

Giorgio Di Natale, Marie-Lise Flottes, Feng Lu, Bruno Rouzeyre. tLIFTING : A Multi-level Delay-annotated Fault Simulator for Digital Circuits. DCIS 2012 - 27th Conference on Design of Circuits and Integrated Systems, Nov 2012, Avignon, France. , 2012. lirmm-00799892

HAL Id: lirmm-00799892

<https://hal-lirmm.ccsd.cnrs.fr/lirmm-00799892>

Submitted on 12 Mar 2013

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

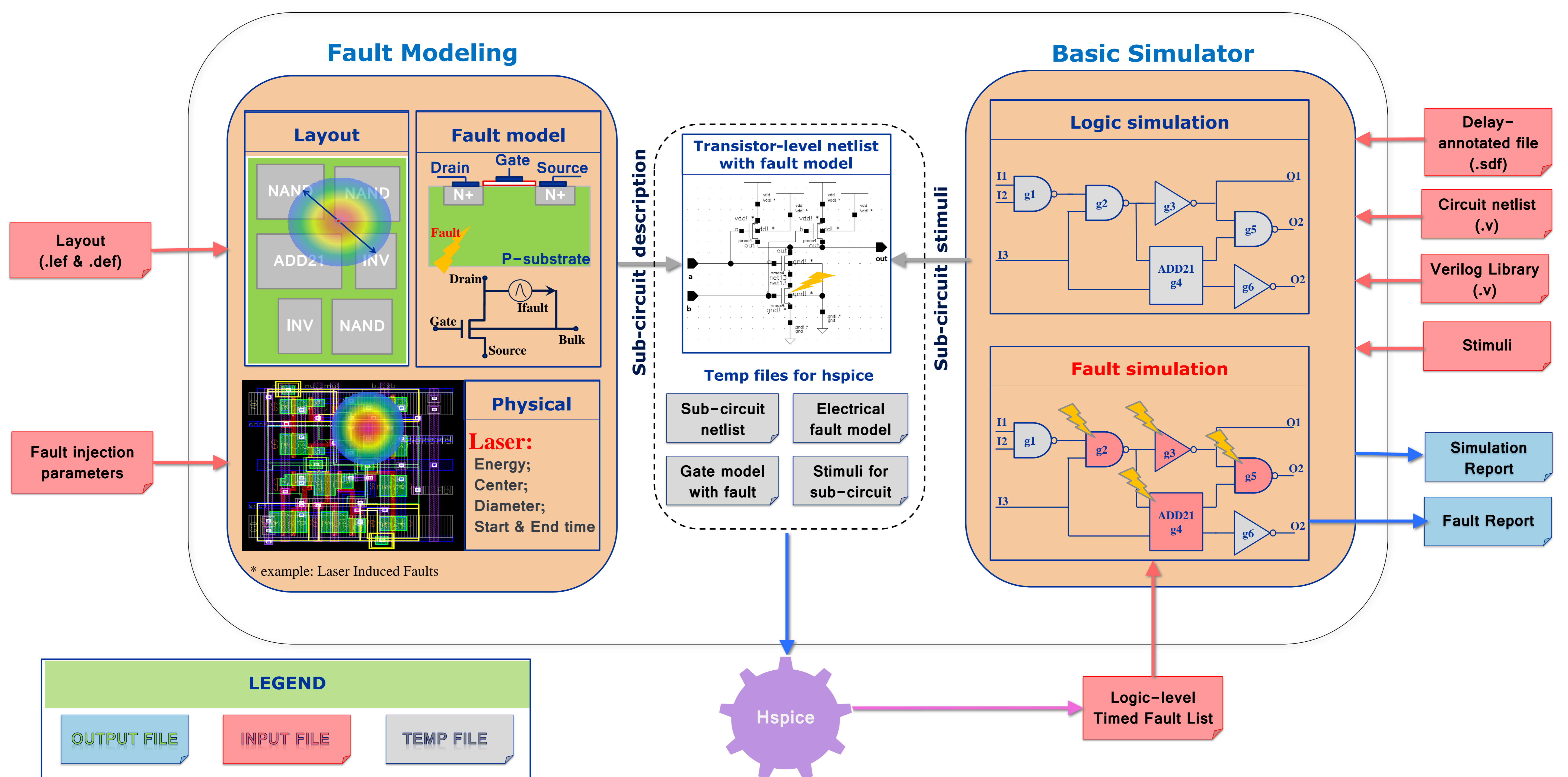
Characteristics

- **Mixed-mode multi-level simulation:**
 - 0-delay gate-level
 - delay-annotated gate-level
 - transistor-level
- **Fault types:**
 - Single/Multiple Event Transient (SET/MET)
 - Single Event Upset (SEU) / Multiple Bit Upset (MBU)
 - Stuck-at
- **Electrical behavior modeling**

Applications

- **Fault simulation:**
 - Single/Multiple Event Transient (SET/MET)
 - Single Event Upset (SEU) / Multiple Bit Upset (MBU)
 - Stuck-at
- **Secure circuits: fault attacks**
 - Fault attacks (Laser, EM, ...)
 - Evaluation of countermeasures
- **Reliability evaluation**

ARCHITECTURE of tLIFTING FAULT SIMULATOR



MULTIPLE LEVEL FAULT SIMULATION PROCESS

