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An IR-Drop Simulation Principle Oriented to Delay Testing

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Abstract- This paper deals with delay fault simulation of logic circuits in the context of IR-drop induced delay. An original algorithm is proposed allowing to perform a per-cycle delay simulation of the logic Block Under Test (BUT) while taking into account the whole chip IR-drop impact on the simulated block. The simulation is based on a realistic resistive model of the Power Distribution Network (PDN).

Keywords- Digital CMOS IC; Test; Power Noise; IR-drop; Simulation.

I. INTRODUCTION

As technology scales into the nanometric range, aggressive voltage scaling reduces significantly the noise margin. On the other hand, the ultra-high transistor density and rising frequency lead to a power density problem that requires a large amount of current to be delivered to, increasing power supply noise [1]. Excessive noise can significantly affect the circuit performance and cause problem such as signal integrity [2] or additional delay [3].

Power supply noise refers to some kind of fluctuations (drop) in the power and ground voltages due to currents (I) flowing through the parasitic elements of on-chip and package supply networks. The on-chip Power Distribution Network (PDN) is predominantly resistive and mainly produces noise due to IR-drop, while package interconnect has a higher parasitic inductance and so its noise is generated primarily by L.di/dt effects. In this paper, we focus only on fluctuations in the power and ground voltages produced by IR-drop.

As a consequence of these fluctuations, logic gates can be powered with lower-than-normal Vdd or higher-than-normal Gnd or both, reducing the gate swing and translating to logic gates with increased delay. Moreover the sensitivity of the gate delay to power supply noise increases with technology scaling. It has been reported that fluctuations of 10% in power/ground supply voltage increase gate delay by 8% in 180nm technology [4], fluctuations of 10% can cause up to 30% in gate delay in 130nm technology [5] and a 1% change in power supply voltage cause nearly 4% change in gate delay in 90nm technology [6]. The impact of power supply noise has therefore become a critical concern, both for design and test aspects.

In this paper we focus on the test aspect and we propose an original algorithm for accurate simulation of IR-Drop induced excessive delay in a logic Block Under Test (BUT) while taking into account the whole chip IR-drop impact on the simulated block.

This paper is organized as follows. Section II provides background on power supply noise induced by IR-drop and motivates our contribution with respect to previous works. Section III introduces the fundamental principles of the simulation algorithm we propose. Section IV details the pre-characterization procedure for both the gate library and the power distribution network. Finally, section V concludes the paper.

II. PROBLEM STATEMENT

IR-drop has been studied and analyzed in the past few years from different perspectives by both the design and test engineers. For example, the commercial design flows handle IR-drop through an appropriate power network design or improved margin design. In the design phase, the objective is obviously to reduce as much as possible the whole IR-drop effects at the chip level. In this context, a number of studies have been performed to propose different supply network and circuit models for the estimation of power supply noise due to IR-drop [7-10]. These models can be used to identify critical areas of the chip and provide information that helps the designer to make tradeoffs in the various parameters of the power distribution network. Most of these works are based on a vectorless approach and primarily target the spatial effect of IR-drop.

Regarding the test aspect, the problematic is somehow different since the goal is to verify that the chip does not present functional problems related to excessive delay due to IR-drop. In this case, not only the spatial effect should be taken into account but also the temporal effect, i.e. the impact of the vector test sequence. In other words, power supply voltage analysis has to be addressed through a vector-based approach. In addition, different objectives can be under consideration:

- Because the design tools cannot completely guarantee a 100% IR-drop free solution, the chip may still manifest IR-drop originated functional problems. In

this case, the test objective is to target the IR-drop originated delay fault and to generate a delay test sequence able to exacerbate the IR-drop phenomena [11-13].

- Because structural test vectors, DFT and BIST result in much higher power density and in so much higher IR-drop than in functional mode, a chip may fail the test due to excessive delays induced by test mode IR-drop. In this case, the test objective will be to minimize the IR-drop phenomena while generating a test sequence for some kind of defined fault models, or during scan-test [14-18].

Regardless of maximizing or minimizing its impact, IR-drop phenomenon has to be considered, predicted and evaluated in the test phase. This means that test preparation requires an accurate simulation tool to evaluate the IR-drop produced by a given input sequence of vectors and to predict the induced gate delays. The challenge here comes from two strong limitations:

- Chip logic level: IR-drop is a global phenomenon that must be considered at the chip level but accurate vector-dependent simulation at the chip level is not feasible. In particular, accurate models developed in the context of PDN design optimization cannot be used for vector-dependent simulation due to prohibitive simulation cost.
- Block electrical level: IR-drop is an electrical phenomenon that implies currents and resistances but, here again, electrical transistor-level simulation (SPICE-like simulation) at the block level is not feasible due to prohibitive simulation cost.

In this context, our approach to cope with these issues is:

- At chip level: Most of the works published in the literature use a very simplified model of the PDN that permits to perform vector-dependent simulation but is not representative of the whole chip IR-drop impact. Our objective is to propose a more refined model of the PDN that permits to take into account the whole chip IR-drop impact with a reasonable simulation cost.
- At block level: A number of works published in the literature use gate-level simulation with Standard Delay Formulation (SDF) annotation. Our idea is to use a similar approach based on event-driven simulation at gate level with annotation not only on gate delay but also on current injected in PDN.

III. SIMULATION PRINCIPLES

In this section, the fundamental principles of the simulation are defined knowing that the objective is to evaluate the excessive delays induced by the IR-drop phenomena in the context of a test generation process.

A. Transient simulation principle

Being in the context of a test generation process, a logic simulation is performed at the block level with a sequence of input vectors. The event-driven simulation algorithm considers a logic domain and an electrical domain where it computes both:

- In the logic domain, the logic signals with the corresponding delays on the logic lines of the block under test,
- In the electrical domain, the transient electrical signals in the resistances of a realistic PDN model and the corresponding drop events.

In other words, given the logic description of the block and a pair of input vectors, the algorithm first initializes each logic line to the good simulation value and inserts in the event queue the switching inputs. Then, for each event in the queue, logic signals in the logic block are simulated and the electrical signals in the PDN are computed, as illustrated in Figure 1.

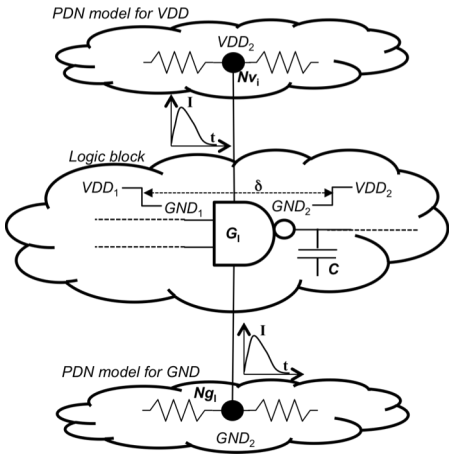


Figure 1: Two domain simulation principle

The above figure illustrates the simulation concept. Given a gate Gi connected in the PDN to node Nvi for the power supply and node Ngi for the ground, when a gate input switches at time t, the algorithm:

- computes the swing V_{swing1} of the input signal with:

$$V_{swing1}(t)=VDD_1(t)-GND_1(t) \quad (1)$$

- computes the drop V(Nvi) at node Nvi taking into account all resistances and all currents in the PDN model for VDD,

- computes the drop V(Ngi) at node Ngi taking into account all resistances and all currents in the PDN model for GND,

- computes the swing V_{swing2} at time t with:

$$V_{swing2}(t)=VDD_2(t)-GND_2(t)=V(Nvi)-V(Ngi) \quad (2)$$

- deduces from pre-computed tables T_{delay_gate} the corresponding delay δ of gate Gi as a function of V_{swing1}, V_{swing2} and the load capacitance C_{load}:

$$\delta(Gi) = f\,(V_{swing1}, V_{swing2}, C_{load}) \quad (3)$$

- computes the gate output signal with delay δ(Gi),

- deduces from pre-computed tables $T_{current_gate}$ the corresponding current I_{Nvi} in the power supply node Nvi and the current I_{Ngi} in the ground node Ngi as a function of V_{swing1}, V_{swing2} and the load capacitance C_{load}:

$$I_{Nvi} = f_1\,(V_{swing1}, V_{swing2}, C_{load}) \quad (4)$$

$$I_{Ngi} = f_2\,(V_{swing1}, V_{swing2}, C_{load}) \quad (5)$$

- injects these currents into the PDN realistic model.

The above algorithm is based on a PDN realistic model which is described in the next paragraph 'B'. In addition it requires pre-computed tables for the gate delay and currents which are obtained from a pre-characterization of the library. This gate pre-characterization is described with many details in section IV.

B. PDN realistic model

In the electrical domain, the algorithm computes the different current flowing through the PDN assuming a classical physical implementation.

In the top metallization level of the chip, a level n is composed of horizontal metal lines while level n-1 is composed of vertical lines. Note that it may be possible to repeat this alternated horizontal and vertical lines configuration with levels n-2 and n-3… The horizontal lines in level n are connected through vias to the vertical lines in level n-1. The whole set of connected lines creates a two-dimensional Distribution Network as represented in Figure 2. Usually, in a given level, every other line is dedicated to VDD and every other line to GND; In this way, it is possible to create a two-dimensional network for VDD and another two-dimensional network for GND. Figure 2 illustrates one of the networks, let us say, for example, the Power Distribution Network for VDD.

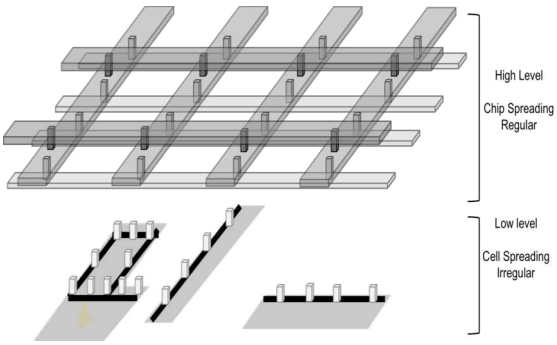
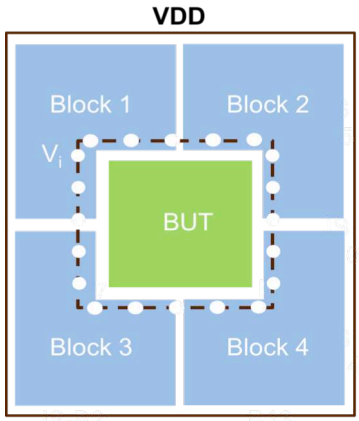


Figure 2: Physical PDN implementation

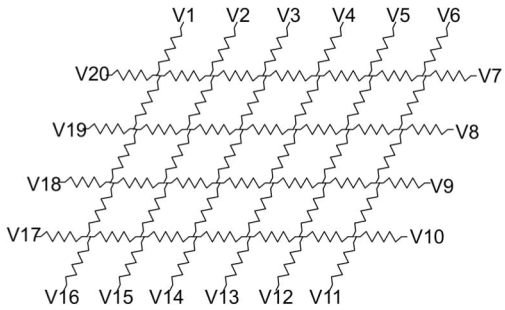
In the bottom metallization level of the chip, metal 2 is commonly used for the VDD and GND lines. In Figure 2, the grey polygons represent mega-cell or logic block with VDD lines (in black) connected through via to the upper two-dimensional network. The VDD and GND lines in the metal 2 level have typically a small length corresponding to the mega-cell they feed. In addition they have multiple parallel via connections to the two-dimensional network. For these reasons, the parasitic resistance of this level is neglected in the model.

The VDD and GND lines in the top level of the chip are very long corresponding to the whole chip size. For this reason the parasitic resistances of the two-dimensional network are considered and modeled as a two-dimensional grid of parasitic resistances as illustrated in Figure 3.b.

In this electrical model of the PDN, it is assumed that the grid border is connected to different Vi voltages as illustrated in Figure 3. In the design phase of the chip, the whole grid is optimized in order to minimize the IR-drop phenomena using different design tools: i) some grip optimization tools compute a whole static IR-drop assuming a static current consumption in each block, ii) some other tools perform a vectorless dynamic simulation. In any case, the resulting voltages Vi on the BUT borders (Fig. 3.a) are obtained from the design phase and used in the simulation (Fig. 3.b) allowing to take into account the whole chip impact on the IR-drop phenomena.



a) Chip impact BUT



b) PDN electrical model

Figure 3: Electrical model of the PDN with whole chip impact

IV. PRE-CHARACTERIZATION

As explained in the previous section, at each time step, the simulator computes the current draw of the switching gates and propagates this current in the PDN in order to estimate the voltage drop on PDN nodes and the resulting delay of the switching gates. This computation requires a pre-characterization of the gates in terms of current draw and delay (library construction), as well as a pre-characterization of the current distribution in the PDN (distribution factor). In this section, we detail these two pre-characterization steps. Spice simulations are performed in a standard 45nm CMOS technology. It should be highlighted that the pre-characterization of the gates has to be done only once for a given technology and so the required time is not considered as critical.

A. Library

When a gate switches, it draws a current from the power supplies, VDD and GND, during the switching activity of the gate. This current draw is transient. The amplitude and duration of the current draw is highly dependent on the technology. Therefore, a pre-characterization of the standard gates in the technology of the BUT is necessary in order to compute the nominal current draw of each gate. Similarly, the nominal delay of a standard gate, which also depends on the technology, requires a pre-characterization.

Moreover, the current draw and delay of a switching gate depend on the power supply levels, which are likely to be affected by IR-drop induced by neighboring gates, and on the load capacitance of the gate. As a consequence, the actual current draw and delay must be computed taking the gate environment into account. Subsection IV.A.1 presents the variable parameters that should be considered for this computation and subsection IV.A.2 details the computation of the actual current draw and delay for a gate in a given simulation environment.

1) *Variable parameters*

The current draw from the power supplies, VDD and GND, and delay of a gate depend on:

- **Edge:** Input transition of the gate (rising or falling);
- **Supply and input swings:** As mentioned previously, the gate can be affected by voltage drop on the power and/or the ground supplies, which impacts the current draw and delay. It must be considered that the upstream gate may also be affected by voltage drop, which also impacts the behavior of the considered gate. In order to determine the library elements, we take into account the voltage swings of the upstream gate (V_{swing1} or input swing) and the considered gate (V_{swing2} or supply swing), defined by equations (1) and (2) where $VDD_1(t)$ and $GND_1(t)$ (resp. $VDD_2(t)$ and $GND_2(t)$) are the power supply and ground supply levels of the upstream gate (resp. considered gate), as illustrated on Figure 4.
- **Capacitance load:** Equivalent capacitance of the downstream gates connected to the considered gate (i.e. fanout of the gate).

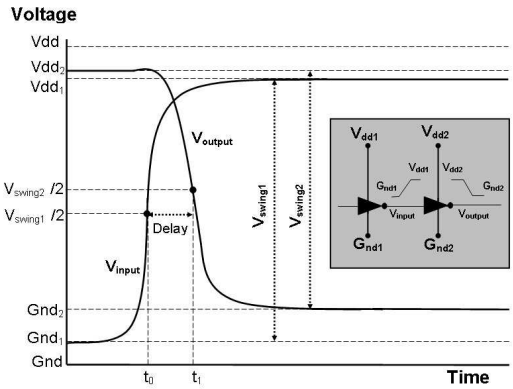


Figure 4: Library parameter definition

2) *Library element models*

Spice simulations are performed to pre-characterize the current draw and delay of the gates under all possible conditions that are likely to be a realistic environment for the gates in the simulation context. To this aim, all combinations of voltage swings between 100% and 80% of the nominal power supply swings for V_{swing1} and V_{swing2} have been simulated, for load capacitance values from one to five times the elementary equivalent capacitance of an inverter, for positive and negative transition edges and for all standard gates. A model was derived from the electrical simulations for the computation of the gate delay and current draw of the gates as a function of the variable parameters listed previously. We present hereafter the models derived for an inverter.

a) *Delay:*

The propagation delay δ is defined as the duration between the time t_0 at which the input signal of the gate crosses half its excursion ($V_{swing1}/2$) and the time t_1 at which the output signal of the gate crosses half its excursion ($V_{swing2}/2$), as illustrated in Fig.4. The nominal delay δ_{nom} of a gate, obtained with ideal voltage supplies and minimal load capacitance C_{min}, is a minimum. In our case of study (45nm), δ_{nom}=4.903ps.

The delay increases linearly when the supply swing of the gate, V_{swing2}, decreases (the other variable parameters being constant at nominal value), as illustrated in Fig.5.b in case of a positive transition on the input. It also increases when the input swing of the gate, V_{swing1}, decreases. This latter dependence is a bit less linear than the previous one, but it can reasonably be approximated by a straight line, with an average error inferior to 0.5%, as illustrated in Fig.5.a. Although the variation of the delay in function of the load capacitance describes an exponential curve, this curve can be approximated by a linear function if the load capacitance variation is small (from one to five times C_{min}), as shown by Fig.5.c.

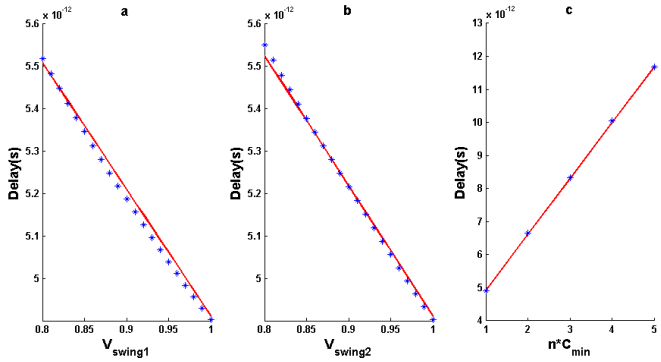


Figure 5: Variation of the inverter delay as a function of:
a) the input swing; b) the power swing; c) the load capacitance.

The three variable parameters are independent and the resulting function of the three variables is therefore a product of the above three linear functions, i.e. a polynomial of the first order for each variable parameter and of all combinations of the variables. We have established the polynomial equation of the delay as a function of V_{swing1}, V_{swing2} and the load capacitance C_{load}. This polynomial depends on the input edge (rising or falling) and the gate type (inverter, NAND2...). As a consequence, two sets of 8 polynomial coefficients are provided to the simulator for the computation of the delay for each gate type, as shown by equations 6 and 7. The two sets of coefficients associated to the inverter are given in Table 1 (T_{delay_inv}).

$$\delta_{0_1}(inv)=a_0+b_0.V_{swing1}+c_0.V_{swing2}+d_0.C+e_0.(V_{swing1}.V_{swing2}) +f_0.(V_{swing1}.C)+g_0.(V_{swing2}.C)+h_0.(V_{swing1}.V_{swing2}.C) \quad (6)$$

$$\delta_{1_0}(inv)=a_1+b_1.V_{swing1}+c_1.V_{swing2}+d_1.C+e_1.(V_{swing1}.V_{swing2}) +f_1.(V_{swing1}.C)+g_1.(V_{swing2}.C)+h_1.(V_{swing1}.V_{swing2}.C) \quad (7)$$

Table 1: Polynomial coefficients for the delay computation of an inverter.

	a_i	b_i	c_i	d_i	e_i	f_i	g_i	h_i
δ_{0_1} (x 10^{-12})	14.295	-9.656	-8.160	5.999	6.746	-2.750	-4.162	2.600
δ_{1_0} (x 10^{-12})	13.479	-9.337	-6.427	5.583	5.185	-3.395	-4.203	3.113

Figure 6 shows the variation of the delay of an inverter excited by a positive input transition as a function of the input and power swings with minimal capacitance load obtained from Spice simulation on the one hand (left) and from our polynomial model on the other hand (right). The average error on the estimation of the delay in this case is 0.56%. Over all cases, including variations of the load capacitance, the average error is as low as 0.35%. This average error looks very satisfying with respect to other works on the topic [19].

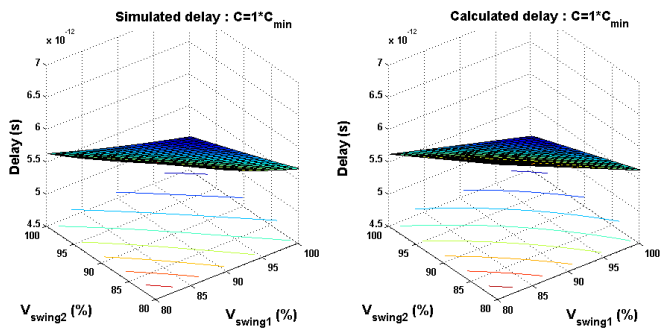


Figure 6: Variation of the delay as a function of V_{swing1} and V_{swing2} with C_{min} obtained from Spice simulation (left) and computed from polynomials (rigth).

b) Current draw:

As mentioned previously, the current drawn by a switching gate from the power and ground supplies is a time variant function. Hence, the model provided for simulation cannot be a single value. A function of time is not convenient to handle during the logic fault simulation. As a consequence, we chose to store a reference current draw as an array of 100 current amplitude values with picosecond resolution and to compute, from this reference, the actual current draw according to the environmental conditions. The first point of the array corresponds to t_0 (Fig.4). Considering 100ps duration, we can be sure that the current draw falls again down to zero by the end of the array. For given conditions, the current drawn from VDD, I_{Nvi}, is different from the one drawn from GND, I_{Ngi}, and two reference arrays must therefore be stored. As for the delay, a reference is valid for a given gate type and a given input edge.

Figure 7 shows the transient current drawn from the ground supply during the switch of an inverter excited by a positive transition for different values of the gate power swing V_{swing2} (a), of the input swing V_{swing1} (b) and the load capacitance C (c), obtained by Spice simulation. For each case of varying parameter, the two other variable parameters are constant at the nominal value ($V_{swing1,2}$=100% of VDD and C=C_{min}). The impact of the gate power swing V_{swing2} on the transient current draw appears to be a simple reduction of amplitude values. Hence, a single multiplying factor is enough to derive the array of current values from the reference array in this case. A similar effect of amplitude factor can be observed on the current draw when the input swing V_{swing1} varies, but it is then associated to a shift in time. It is thus possible, in order to derive the actual current values from the reference one, to first shift the values in the array and then apply a multiplying factor. The impact of the load capacitance on the current draw is much more difficult to model. Indeed, no simple factor can be found to compute all other curves from a reference one. As only five different values of the load capacitance are considered, we can simply store the corresponding five arrays of current values for nominal input and power swings.

Note that the results and conclusions regarding the power supply current draw for GND are similar to the ones presented above for VDD.

B. Distribution factor

As previously mentioned, when a gate is switching the corresponding current given by the above pre-characterization phase has to be injected in the two-dimensional grid. Obviously, this gate current flows from the border voltages Vi to the switching gate through the whole grid. In other words, the original current is distributed in the two-dimensional grid of resistances, i.e. a fraction DF_{ij} of the original current appears in each resistance R_{ij}. This set of current fractions DF_{ij} is called here the Distribution Factors, which are determined through a SPICE pre-simulation.

For this pre-characterization of the Distribution Factors, a DC unity current source I is simply connected to the central point of a 100x100 grid of resistances. The simulation gives the values I_{ij} of the current in every resistance R_{ij}, each current I_{ij} being a fraction of the original unity current: this set of I_{ij} values directly corresponds to the DF_{ij}. Figure 8 gives the results of the Spice simulation for the horizontal resistances; a similar plot can be obtained for the vertical resistances.

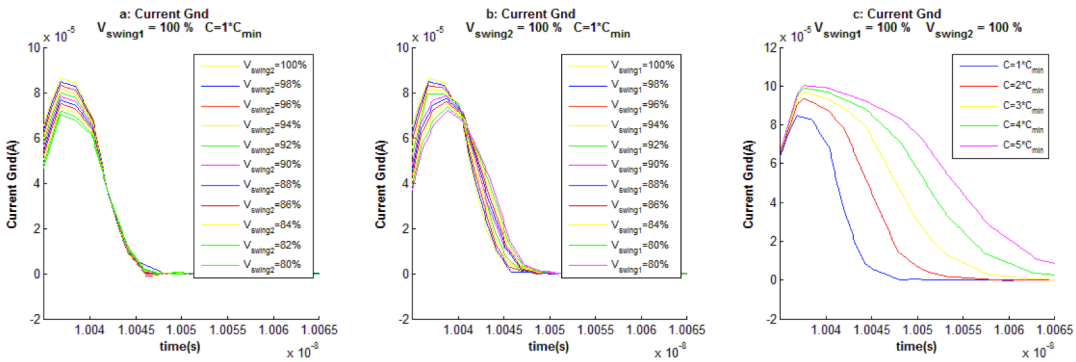


Figure 7: Variation of the transient current draw for different values of: a) the power swing; b) the input swing; c) the load capacitance.

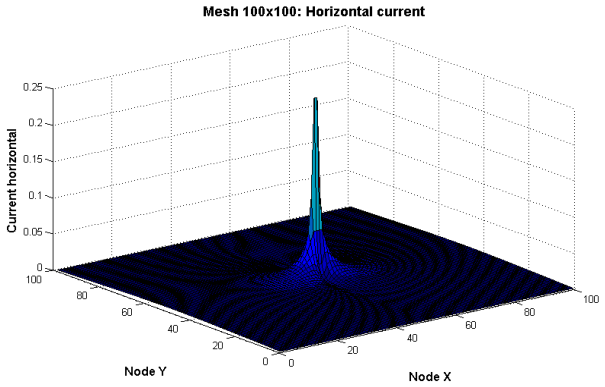


Figure 8: A unity current distribution in the resistive PDN

V. CONCLUSION

In this paper, an original algorithm has been proposed for delay fault simulation of logic circuits in the context of IR-Drop induced delay. The algorithm concurrently performs an event driven logic simulation of the logic block and computes the current flowing into the PDN electrical network. From the currents flowing into the PDN the voltage swing of the switching gates are computed and the corresponding delay are determined. The proposed algorithm takes into account the whole chip impact on the BUT obtained from the design phase. A pre-characterization of the gate delay and current allow a very precise determination of the delays.

ACKNOWLEDGEMENT

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