Test Solution for Data Retention Faults in Low-Power SRAMs

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***Abstract*—Low-power SRAMs embed mechanisms for reducing static power consumption. When the SRAM is not accessed during a long period, it switches into an intermediate low-power mode. In this mode, a voltage regulator is used to reduce the voltage supplied to the core-cells as low as possible without data loss. Thus, faulty-free behavior of the voltage regulator is crucial for ensuring data retention in core-cells when the SRAM is in low-power mode. This paper investigates the root cause of data retention faults due to voltage regulator malfunctions. This analysis is done under realistic conditions (i.e., industrial core-cells affected by process variations). Based on this analysis, we propose an efficient test flow for detecting data retention faults in low-power SRAMs.**

Keywords—SRAM, low-power design, test algorithm, memory test.

I. INTRODUCTION

With the growing demand of high performance, multi-functional and hand-held devices, power consumption has emerged as a major design concern. Simultaneously, technology scaling is shrinking device features as well as lowering the power supply and threshold voltages, which cause a significant increase of leakage currents. Power consumption due to leakage currents (static power) has become a major contributor to the total power consumption in CMOS circuits [1-2].

With technology advancements, System-On-Chips (SOCs) allow to embed, in a single chip, all components and functions that historically were placed on a printed-circuit board. Within SOCs, embedded memories are the densest components, accounting for up to 90% of chip area [3]. Hence, embedded memories are arising as the main contributor to the overall SOC static power consumption. Moreover, their dense core-cell array structure prompts them to be vulnerable to physical defects. It is therefore imperative to understand failure mechanisms and to develop effective test solutions for such devices.

Various techniques have been proposed to reduce SRAMs static power consumption [4-5]. At architectural level, power gating mechanisms and voltage regulation systems allow power modes on SRAMs. Before a long period of inactivity, the SRAM can be turned into an intermediate low-power mode, called **deep-sleep**, such that the power supply voltage of the peripheral circuitry of the memory is gated-off, while a voltage regulator is used to reduce the supply voltage of the core-cell array at a level that allows data retention [6-7].

In case the core-cell array is supplied at voltage level that is lower than the data retention voltage of the SRAM, data loss may occur [8]. Hence, malfunctions of the voltage regulator can lead to data retention faults in low-power SRAMs. Although many works have been done in the area of memory test, notably [9-11], only few publications target test of low power SRAMs [12-13].

This paper investigates the root cause of data retention faults due to voltage regulator malfunctions. This analysis is done under realistic conditions (i.e., industrial core-cells affected by process variations). We first analyze the impact of process variations on the stability of core-cells, and its connection to the data retention voltage of an SRAM. This analysis can lead us to determine the worst-case data retention voltage in deep-sleep mode. Then, we study defects in the voltage regulator that may lead to data retention faults when the SRAM is in deep-sleep mode. Finally, we propose an optimized test flow for the detection of data retention faults.

The main contributions of our work can be summarized as follows:

- A complete methodology is presented to investigate the root cause of data retention faults in low-power SRAMs.
- An efficient March test [10] solution is presented.
- An optimized test flow based on the proposed March test is generated. This test flow exploits the information coming from the core-cell process variation analysis in order to determine the best test conditions. This increases the test coverage while lowering the overall test time.
- Presented results are based on an industrial low-power SRAM architecture from Intel. Nevertheless, the adopted methodology can be applied to any similar low-power SRAM design.

The remainder of this paper is organized as follows. Section II describes the architecture and functioning of the low-power SRAM used in this work. Section III describes how variations of the *threshold voltage* (*Vth*) inside core-cells impact the data retention voltage of the SRAM, in deep-sleep mode. In Section IV, we describe all experiments that have been performed to characterize resistive-open defects injected in the voltage regulator, whereas Section V presents an efficient test solution targeting the identified faulty behaviors. Concluding remarks are given in Section VI.

II. LOW-POWER SRAM: ARCHITECTURE AND FUNCTIONING

Figure 1 depicts a conceptual view of the studied low-power SRAM. It is a single-port word-oriented SRAM, designed by Intel with a 40nm low-power process technology. A reference 4Kx64 memory block has been considered, organized as a core-cell array of 6T core-cells composed of 512 *bit lines* (BLs) and 512 *word lines* (WLs).

This low-power SRAM embeds power gating facilities, which are implemented using *power switch* (PS) blocks connected to both the core-cell array and the peripheral circuitry (I/O circuitry, control block and address decoder).

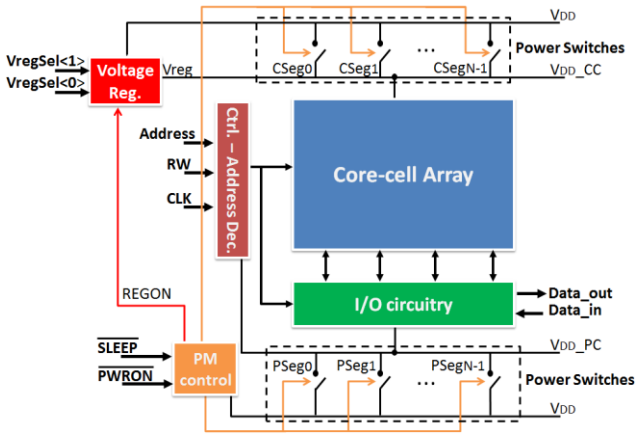

Fig. 1 Low-power SRAM architecture

The PSs of both core-cell array and peripheral circuitry are implemented through a network of PMOS transistors structured in *N* segments (refer to [12-13] for details). Such PSs, along with a voltage regulation system, enable power modes on the SRAM by varying the supply voltage applied to the core-cell array and peripheral circuitry internal supply lines (V_{DD}_CC and V_{DD}_PC in Fig. 1, respectively).

A. Power Modes

For the given memory, three power modes can be distinguished: (1) **active mode**, (2) **deep-sleep mode**, and (3) **power-off mode**.

In *active* (ACT) mode, all PSs are activated, which allows both V_{DD}_CC and V_{DD}_PC to be driven by the main supply rail V_{DD}. Hence, both core-cell array and peripheral circuitry are powered by nominal V_{DD} and the SRAM can perform read and write operations. Note that the voltage regulator is switched off (signal *REGON* is set to logic '0') in ACT mode.

In both *deep-sleep* (DS) and *power-off* (PO) modes, all PSs are deactivated, thus, V_{DD}_CC and V_{DD}_PC are no longer connected to V_{DD}. In DS mode, the voltage regulator is switched on (signal *REGON* is set to logic '1') to generate a fixed voltage level (*Vreg* in Fig. 1), lower than nominal V_{DD}, to be provided to the core-cell array through V_{DD}_CC, whereas V_{DD}_PC discharges to 0V. The voltage *Vreg*, which must guarantee data retention [6-7], drastically reduces static power consumption. In DS mode, no operation is allowed to be performed, since peripheral circuitry is switched off.

In PO mode, the embedded voltage regulator is switched off, hence both lines V_{DD}_CC and V_{DD}_PC discharge to 0V. Core-cells are no longer able to retain data in PO mode.

Control signals driving PSs and the control signal *REGON* are generated by the *power mode control* (PM control) logic, based on primary inputs $\overline{SLEEP}$ and $\overline{PWRON}$. Such primary inputs allow switching among different power modes. Note that PM control logic is always supplied by the main supply rail V_{DD} to be able to switch among the various power modes.

In this paper, we focus our analysis on the voltage regulator, which generates the regulated voltage *Vreg* that supplies the core-cell array in DS mode.

B. Voltage Regulator

Figure 2 illustrates the circuit blocks that compose the voltage regulator. The voltage regulator is an error amplifier connected to an output stage PMOS transistor (*MPreg1* in Fig. 2) that generates *Vreg* based on a reference voltage (*Vref* in Fig. 2). Note that *Vreg* must be equal to *Vref*. A voltage source generates four voltage levels that can be provided to

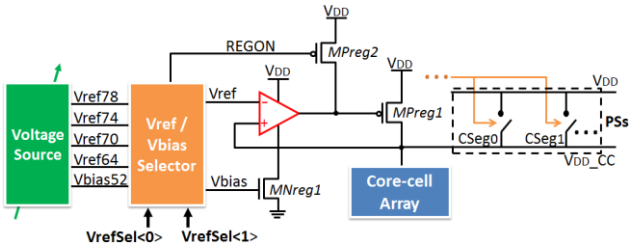

Fig. 2 Voltage regulator top view

the error amplifier as reference voltage. Such four voltage levels are $0.78*V_{DD}$, $0.74*V_{DD}$, $0.70*V_{DD}$ and $0.64*V_{DD}$, which are available in nodes *Vref78*, *Vref74*, *Vref70* and *Vref64*, respectively. Furthermore, the voltage source generates a bias voltage (*Vbias* in Fig. 2) that controls NMOS transistor *MNreg1* for error amplifier biasing. Only one voltage level ($0.52*V_{DD}$) is generated by the voltage source for biasing. This voltage level is available in node *Vbias52* and has been chosen such that the specified maximum budget for voltage regulator power consumption is never exceeded. When the regulator is active, the block *Vref/Vbias selector* assigns one of the four voltage levels generated by the voltage source to *Vref*, according to primary inputs *VrefSel<0>* and *VrefSel<1>*. Moreover, it sets *Vbias* to $0.52*V_{DD}$. The logic value on primary inputs that sets *Vref* to different levels is considered not relevant for the study. However, when the regulator is switched off, *Vref/Vbias selector* internally sets *Vbias* to 0V and *Vref* to V_{DD}, regardless of primary input signals. Furthermore, a pull-up transistor (*MPreg2* in Fig. 2) sets the gate of the output stage transistor *Mpreg1* to V_{DD}, deactivating it.

III. Data Retention Voltage

Despite maximizing static power savings, lowering the core-cell array supply voltage too far, in DS mode, may result in *data retention faults* (DRFs) [8]. Therefore, a question remains on the lower bound of the voltage level at V_{DD}_CC, in DS mode, that still ensures data retention in all core-cells of the array, which is referred to as *data retention voltage in DS mode* (DRV_{DS}).

A. Relation between DRV_{DS} and Static Noise Margin

The stability of an SRAM 6T core-cell, whose schematic is shown in Fig. 3, is usually defined by the *static noise margin* (SNM) [14]. SNM of a core-cell is measured through the butterfly plot that is made of the *voltage transfer curves* (VTCs) of core-cell's cross-coupled inverters.

In [6] authors show that, when the supply voltage of a core-cell scales down, the VTCs of the internal cross-coupled inverters degrade, which reduces the SNM of the core-cell. Furthermore, it is shown that the supply voltage can be scaled down up to the level in which the SNM of the core-cell equals zero, while still ensuring data retention. If the supply voltage is further reduced, the cross-coupled inverters

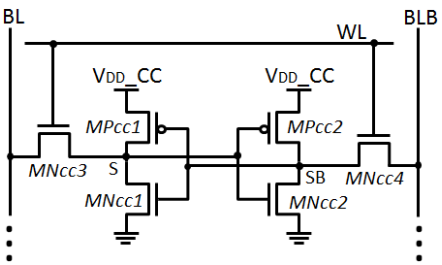

Fig. 3 6T SRAM core-cell

flip to the state determined by the deteriorated VTCs and loose the capability to retain data.

In this subsection, we define SNM_{DS1} and SNM_{DS0} as the maximum amount of voltage noise that a core-cell can tolerate, without loosing stored logic '1' and logic '0', respectively, when the SRAM is in DS mode. Note that SNM, in this case, is measured with V_{DD}_CC lowered at *Vreg* and with WLs and BL pairs set to 0V, as peripheral circuitry is switched off.

Based on the previous observations, we also define DRV_{DS1} and DRV_{DS0} as the voltage levels applied to V_{DD}_CC, in DS mode, such that the lower bound of SNM_{DS1} and SNM_{DS0}, respectively, considering all core-cells in the array, is zero. In other words, DRV_{DS1} and DRV_{DS0} are the lower bounds of core-cell array supply voltage that still ensure retention of logic '1' and logic '0', respectively, in all core-cells, when the SRAM is in DS mode. The DRV_{DS} of the SRAM is the maximum value between DRV_{DS1} and DRV_{DS0}.

Within-die process variations result in mismatches of electrical parameters (e.g. V_{th}) in identically designed transistors inside a core-cell. This results in several asymmetric core-cells in the array, with different stabilities, which results in the increase of the DRV_{DS} of the SRAM. In this case, DRV_{DS} is determined by the least stable core-cell of the array.

B. Impact of V_{th} Variations on DRV_{DS}

In this subsection, we analyze the impact of process variability on DRV_{DS} by introducing V_{th} variations in a single core-cell of the array (all other core-cells are symmetric).

Figure 4 shows the simulated effects on DRV_{DS1} (Fig. 4.a) and DRV_{DS0} (Fig. 4.b) when a single transistor of the studied core-cell has V_{th} variations. For measuring DRV_{DS1} and DRV_{DS0}, in each case, the supply voltage of the affected core-cell has been scaled down until SNM_{DS1} and SNM_{DS0} equals zero, respectively. All combinations of process corner (slow, typical, fast, fast NMOS/slow PMOS, slow NMOS/fast PMOS) and temperature (-30˚C, 25˚C, 125˚C) have been simulated, for each transistor. Data shown in Fig. 4 correspond to the combination of process corner and temperature that maximizes DRV_{DS1} and DRV_{DS0}, for each affected transistor. We observe that negative *Vth* variations on transistors that compose the inverter driving logic '1' (*MPcc1*/*MNcc1*, when *S*='1', and *MPcc2*/*MNcc2*, when *S*='0') lead to higher DRV_{DS1} and DRV_{DS0} compared to the case where the transistors of the other inverter are affected. Furthermore, we verify that *Vth* variations on pass transistors (*MNcc3* and *MNcc4*) have less impact on data retention, which cannot be neglected, however. When all core-cells are symmetric (zero *Vth* variations in all transistors), Fig. 4 shows that DRV_{DS1} and DRV_{DS0} are over 60mV.

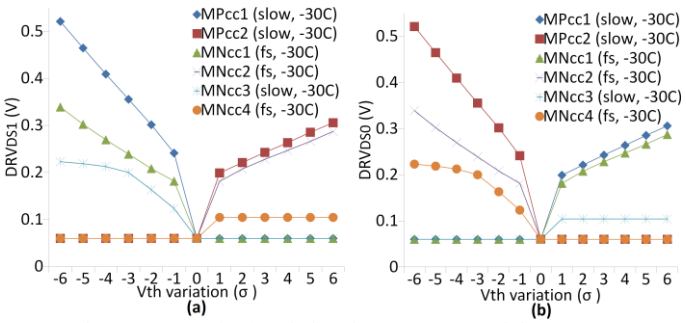

Fig. 4 Impact of *Vth* variations in (a) DRV_{DS1} and (b) DRV_{DS0}

From the experiments depicted in Fig. 4, we can draw the following observations:

1. DRV_{DS1} increases when there are core-cells in the array such that *Vth* variations in *MPcc1*, *MNcc1* and *MNcc3* are negative and *Vth* variations in *MPcc2*, *MNcc2* and *MNcc4* are positive.
2. DRV_{DS0} increases when there are core-cells in the array such that *Vth* variations in *MPcc1*, *MNcc1* and *MNcc3* are positive and *Vth* variations in *MPcc2*, *MNcc2* and *MNcc4* are negative.

From observations 1 and 2, we can conclude that DRV_{DS1} and DRV_{DS0} are maximized (defining DRV_{DS}, as a consequence) when there is at least one core-cell in the array such that all transistors have 6σ of *Vth* variations, with signs specified as discussed above. Despite such combinations have a low probability of occurrence, they can be defined as a theoretical case study that leads to the worst-case DRV_{DS}.

IV. Analysis of Defects in the Voltage Regulator

Figure 5 presents in detail the internal structure of the embedded voltage regulator described in Section II.B. The voltage source is a voltage divider composed of polysilicon resistors in series (*R1* to *R6*), whereas the error amplifier is composed of a current mirror (transistors *MPreg3* and *MPreg4*) connected to a differential pair (transistors *MNreg2* and *MNreg3*). Figure 5 also illustrates all 32 resistive-open defects that have been injected on the voltage regulator. Defects *Df1* to *Df6* affect the voltage source, while *Df7* to *Df32* affect the error amplifier.

In this section, we describe electrical simulations that have been performed to characterize the SRAM behavior in presence of these defects. As described in the following subsections, such experiments have been performed with different scenarios of *Vth* variations inside core-cells in order to verify the impact of each defect for different values of DRV_{DS}.

A. Experimental Setup

For characterizing each defect, we execute electrical simulations considering five *case studies* (CSs) of V_{th} variations inside core-cells, as described in Table I. CS_1 to CS_4 refer to scenarios where a single core-cell is affected by V_{th} variations. CS_1 corresponds to the scenario that leads to the worst-case DRV_{DS}, as described in Section III.B. CS_2 and CS_3 are scenarios that lead to intermediate values of DRV_{DS}. In CS_4, the core-cell is affected by small variations, thus DRV_{DS} is closer to the value obtained when all core-cells are symmetric. Finally, CS_5 corresponds to the case where 64 core-cells (out of 256K) are affected by the same variations as in CS_2. The goal of CS_5 is to evaluate the impact of each

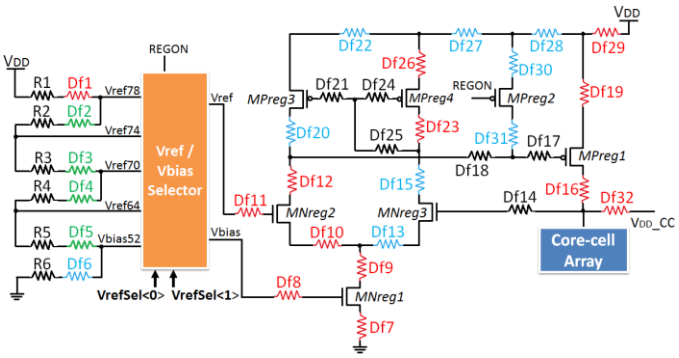

Fig. 5 Resistive-open defects injected in the voltage regulator

TABLE I. *CASE STUDIES FOR V_{TH} VARIATIONS INSIDE CORE-CELLS*

Case study	*#cells*	*MPcc1*	*MNcc1*	*MPcc2*	*MNcc2*	*MNcc3*	*MNcc4*	*DRV_{DS0} (mV)*	*DRV_{DS1} (mV)*	*DRV_{DS} (mV)*
CS_1-1	1	-6σ	-6σ	+6σ	+6σ	-6σ	+6σ	≈60	730	730
CS_1-0	1	+6σ	+6σ	-6σ	-6σ	+6σ	-6σ	730	≈60	730
CS_2-1	1	-3σ	-3σ	0	0	0	0	≈60	686	686
CS_2-0	1	0	0	-3σ	-3σ	0	0	686	≈60	686
CS_3-1	1	0	0	+3σ	+3σ	0	0	≈60	570	570
CS_3-0	1	+3σ	+3σ	0	0	0	0	570	≈60	570
CS_4-1	1	0	0	+0.1σ	+0.1σ	0	0	≈60	110	110
CS_4-0	1	+0.1σ	+0.1σ	0	0	0	0	110	≈60	110
CS_5-1	64	-3σ	-3σ	0	0	0	0	≈60	686	686
CS_5-0	64	0	0	-3σ	-3σ	0	0	686	≈60	686

defect on SRAM normal behavior when 64 core-cells (1 core-cell each 8 BLs) have asymmetries and compare to results obtained in CS_2, where a single core-cell is affected.

Each case study CS_x, $x \in [1, 5]$, is divided in two categories, as follows:

- **CS_x-1**: in such CSs, SNM_{DS1} of the affected core-cells is degraded, which increases the DRV_{DS1} of the SRAM.
- **CS_x-0**: in such CSs, SNM_{DS0} of the affected core-cells is degraded, which increases the DRV_{DS0} of the SRAM.

Table I also shows the maximum DRV_{DS} measured, for each CS, when varying PVT (process corner, supply voltage and temperature) conditions. We observe that each pair CS_x-1/CS_x-0 represents scenarios that result in the same value of DRV_{DS}. The difference is that for all CS_x-1, DRV_{DS} is set by DRV_{DS1}, while for all CS_x-0, DRV_{DS} is set by DRV_{DS0}. Therefore, if a defect in the regulator causes *Vreg* to be lower than DRV_{DS} for case studies CS_x-1, than the core-cells affected by variations loose stored logic '1'. Similarly, logic '0' is lost by the affected core-cells in CS_x-0 if a defect in the voltage regulator causes *Vreg* to be lower than DRV_{DS}. Hence, for case studies CS_x-1 and CS_x-0, electrical simulations have been performed with core-cells affected by *Vth* variations storing logic '1' and logic '0', respectively.

All electrical simulations have been performed using an Intel Spice model corresponding to the SRAM described in Section II. The whole set of PVT conditions considered during the electrical simulations has been selected according to the SRAM specifications. Hence, for each defect and for each considered CS, we propose a set of simulations that have been performed by varying the following parameters:

- **Process corner**: slow, typical, fast, fast NMOS/slow PMOS, slow NMOS/fast PMOS.
- **Supply voltage (V_{DD})**: 1.0V, 1.1V (nominal V_{DD}), 1.2V.
- **Temperature**: -30˚C, 25˚C, 125˚C.
- **Injected defect**: resistance values have been chosen from a few Ωs up to several MΩ in order to provide a complete view of the studied phenomena.

We set the voltage regulator input signals *VrefSel<0>* and *VrefSel<1>* such that *Vreg* is expected to be as close as possible to (but not lower than) the worst-case DRV_{DS} (730mV). Therefore, the voltage regulator is configured such that, for V_{DD} equals to 1.2V, 1.1V and 1.0V, it is expected to generate $0.64*V_{DD}$, $0.70*V_{DD}$ and $0.74*V_{DD}$, respectively, to supply the core-cell array in DS mode.

Each analysis has been performed in presence of only one defect, since the occurrence of multiple defects has a low probability to occur in a small circuit (compared to the whole SRAM) such as the voltage regulator.

B. Simulation Results

In this subsection, we present experimental results that characterize the impacts of resistive-open defects injected on the voltage regulator for all CSs previously presented. In all simulations, the SRAM is initialized and then turned into DS mode for 1ms. During this period of time, we verify if data retention is being guaranteed and we also measure static power consumption of the SRAM.

First, we observed that the effects of *Df14*, *Df17*, *Df18*, *Df21*, *Df24* and *Df25* can be neglected. Such defects affect the gate of transistors inside the error amplifier. The current in such lines is always approximately zero, then the impact of such defects is minimal. Next, based on the impact on SRAM normal behavior, we classified the other defects in the following three categories:

1. *Defects that cause increased static power consumption*:

In presence of such defects (highlighted in blue in Fig. 5), *Vreg* is set to a higher level than expected in DS mode. The worst-case situation occurs when the defect causes *Vreg* to be equal to V_{DD}. In such case, we observed that static power consumption is still reduced over 30%, in the worst-case PVT condition, compared to the case where the SRAM is not being accessed in ACT mode. It means that switching off the peripheral circuitry is already sufficient to achieve important power consumption savings. Defects that cause increased static power consumption in DS mode will be studied in detail in our next work.

2. *Defects that cause DRFs*:

In presence of such defects (highlighted in red in Fig. 5), *Vreg* is set to a lower level than expected, which may cause DRFs in DS mode if *Vreg* is lower than DRV_{DS} of the SRAM.

3. *Defects that cause both increased static power consumption and DRFs*:

This category concerns *Df2*, *Df3*, *Df4* and *Df5*, which affect the voltage source (highlighted in green in Fig. 5). Such defects may lead to both DRFs and increased static power consumption, depending on the resistance value of the defect and on the chosen voltage level of *Vref*. For example, *Df3* reduces the voltage levels at nodes *Vref70*, *Vref64* and *Vbias52*, and increases the voltage level at *Vref78* and *Vref74*. If the regulator is setup such that *Vref* is supposed to be set to $0.78*V_{DD}$ or $0.74*V_{DD}$, then *Df3* may cause DRFs only if its resistance value is high enough to reduce the error amplifier bias current to approximately zero. Otherwise, *Df3* leads to increased static power consumption. However, if *Vref* is supposed to be set to either $0.70*V_{DD}$ or $0.64*V_{DD}$, then *Df3* leads to reduced *Vref* and *Vbias*, which degrades *Vreg* even for low resistance values of defect. This condition maximizes DRF occurrence due to *Df3*. A similar analysis shows that occurrence of DRFs due to *Df2* is maximized if *Vref* is expected to be at $0.74*V_{DD}$, $0.70*V_{DD}$ or $0.64*V_{DD}$, while the impact of *Df4* is maximized if *Vref* is expected to be at $0.64*V_{DD}$. *Df5* causes DRFs only for high resistance values, which impact error amplifier bias current. Otherwise, it increases static power consumption in DS mode.

In Table II, we present a summary of injected defects that cause DRFs in DS mode (defects in categories 2 and 3), as well as the PVT conditions that require the minimal resistance value, for each defect and for each CS, to cause such faulty behavior. We consider resistance values higher than 500MΩ as actual open lines (refer to notation > 500M,

TABLE III. *SUMMARY OF EXPERIMENTS PERFORMED IN PRESENCE OF DEFECTS IN THE VOLTAGE REGULATOR THAT CAUSE DATA RETENTION FAULTS*

	CS_1-1 / CS_1-0		CS_2-1 / CS_2-0		CS_3-1 / CS_3-0		CS_4-1 / CS_4-0		CS_5-1 / CS_5-0		
Def.	***Min. Res. (Ω)***	***PVT***	***Min. Res. (Ω)***	***PVT***	***Min. Res. (Ω)***	***PVT***	***Min. Res. (Ω)***	***PVT***	***Min. Res. (Ω)***	***PVT***	***Description***
Df1	9.76K	fs, 1.0V, 125°C	97.65K	fs, 1.0V, 125°C	390.62K	sf, 1.0V, -30°C	10.25M	fs, 1.0V, -30°C	91.79K	fs, 1.0V, 125°C	Reduces voltage at *Vref78*, *Vref74*, *Vref70*, *Vref64* and *Vbias52*. Thus, *Vref* and *Vbias* are always lower than expected, which degrades *Vreg*.
Df2	9.76K	fs, 1.0V, 125°C	97.65K	fs, 1.0V, 125°C	390.62K	sf, 1.0V, -30°C	10.25M	fs, 1.0V, -30°C	91.79K	fs, 1.0V, 125°C	Reduces the voltage at *Vref74*, *Vref70*, *Vref64* and *Vbias52*, and increases the voltage at *Vref78*. The impact is maximized when the regulator is setup such that *Vref* is supposed to be at 0.74*V_{DD}, 0.70*V_{DD} or 0.64*V_{DD}. Thus, *Vref* and *Vbias* are reduced more than expected, degrading *Vreg*.
Df3	19.53K	fs, 1.1V/ 1.2V, 125°C	195.31K	fs, 1.1V/ 1.2V, 125°C	488.28K	sf, 1.1V/ 1.2V, -30°C	33.20M	fs, 1.2V, 25°C	191.40K	fs, 1.1V/1.2V, 125°C	Reduces the voltage at *Vref70*, *Vref64* and *Vbias52*, and increases the voltage at *Vref78* and *Vref74*. The impact is maximized when the regulator is setup such that *Vref* is supposed to be at 0.70*V_{DD} or 0.64*V_{DD}. Thus, both *Vref* and *Vbias* are reduced more than expected, which degrades *Vreg*.
Df4	19.53K	fs, 1.2V, 125°C	195.31K	fs, 1.2V, 125°C	488.28K	sf, 1.2V, -30°C	33.20M	fs, 1.2V, 25°C	190.31K	fs, 1.2V, 125°C	Reduces the voltage at *Vref64* and *Vbias52*, and increases the voltage at *Vref78*, *Vref74* and *Vref70*. The impact is maximized when the regulator is setup such that *Vref* is supposed to be at 0.64*V_{DD}. In this case, both *Vref* and *Vbias* are reduced more than expected, which degrades *Vreg*.
Df5	2.36M	fs, 1.0V, 125°C	3.26M	fs, 1.0V, 125°C	3.41M	sf, 1.0V, -30°C	97.65M	fs, 1.0V, 125°C	2.48M	fs, 1.0V, 125°C	Reduces only the voltage at *Vbias52* and increases all others. High resistance values impact error amplifier bias current, which degrades *Vreg*.
Df7	976.56K	fs, 1.0V, 125°C	3.90M	fs, 1.0V, 125°C	33.20M	fast, 1.0V, 125°C	> 500M	-	2.21M	fs, 1.0V, 125°C	Reduces error amplifier bias current as long the regulator is activated. As a consequence, the voltage level at the gate of output stage transistor *MPreg1* is higher than normally, which degrades *Vreg*.
Df8	29.78M	fs, 1.0V, 125°C	257.81M	fs, 1.0V, 125°C	> 500M	-	> 500M	-	153.51M	fs, 1.0V, 125°C	Introduces a delay in the activation of biasing transistor *MNreg1*, which is necessary to activate the voltage regulator. If PSs are switched off and the regulator is remain deactivated, then *Vreg* may degrade to 0V.
Df9	976.56K	fs, 1.0V, 125°C	7.81M	fs, 1.0V, 125°C	50.78M	fast, 1.0V, 125°C	> 500M	-	4.64M	fs, 1.0V, 125°C	The effect is similar to the one observed in presence of *Df7*.
Df10	2.92K	fs, 1.0V, 125°C	78.12K	fs, 1.0V/1.2V, 125°C	253.90K	fast, 1.2V, -30°C	6.83M	fs, 1.0V/1.2 V, 25°C	61.52K	fs, 1.0V/1.2V, 125°C	Sets the voltage at the gate of the output stage transistor transistor *MPreg1* to a level that is higher than expected, which degrades *Vreg*.
Df11	3.90K	fs, 1.0V, 125°C	59.57M	fs, 1.0V, 125°C	> 500M	-	> 500M	-	39.23M	fs, 1.0V, 125°C	Introduces an undershoot on the gate of transistor *MNreg2*, which stabilizes at *Vref* after a time interval. Such undershoot increases momentarily the voltage at the gate of *MPreg1*, which degrades *Vreg*.
Df12	45.99K	fs, 1.0V, 125°C	58.59K	fs, 1.0V, 125°C	839.84K	fast, 1.0V, 125°C	> 500M	-	49.01K	fs, 1.0V, 125°C	The effect is similar to the one observed in presence of *Df10*.
Df16	976.56	fs, 1.0V, 125°C	19.53K	fs/fast, all V_{DD}, 125°C	19.53K	all corners, all V_{DD}, 125°C	> 500M	-	2.92K	fs/fast, all V_{DD}, 125°C	Introduce an undesired voltage drop on output stage transistor *MPreg1*, which sets *Vreg* to a voltage level that is lower than normally.
Df19	195.31	fs, 1.0V, 125°C	19.53K	fs/fast, all V_{DD}, 125°C	19.53K	all corners, all V_{DD}, 125°C	> 500M	-	1.02K	fs/fast, all V_{DD}, 125°C	The effect is similar to the one observed in presence of *Df16*.
Df23	121.09K	fs, 1.0V, 125°C	859.37K	fs, 1.2V, 125°C	3.20M	sf, 1.2V, 125°C	62.01M	fs, 1.2V, 125°C	850.28K	fs, 1.2V, 125°C	Reduces the voltage level at the gate of transistors *MPreg3* and *MPreg4*. This increases the conductivity of such transistors, which also sets the voltage level at the gate of output stage transistor *MPreg1* to a higher level than the expected one, degrading *Vreg*.
Df26	3.41K	fs, 1.0V, 125°C	97.65K	fs, 1.0V, 125°C	1.21M	sf, 1.2V, 125°C	65.91M	fs, 1.2V, 125°C	86.36K	fs, 1.0V, 125°C	The effect is similar to the one observed in presence of *Df23*.
Df29	488.28	fs, 1.0V, 125°C	19.53K	all corners, all V_{DD}, 125°C	19.53K	fs/fast, 1.0V, 125°C	> 500M	-	1.17K	all corners, all V_{DD}, 125°C	Reduces the voltage supplied to both error amplifier and output stage transistor *MPreg1*. As a consequence, *Vreg* is necessarily lower than expected.
Df32	4.88K	fast, 1.2V, 125°C	21.68K	fast, 1.2V, 125°C	26.90K	fast, 1.2V, 125°C	> 500M	-	15.43K	fast, 1.2V, 125°C	Introduces a voltage drop on line V_{DD}_CC, in DS mode. Such voltage drop is caused by leakage currents in the core-cell array.

in Table II). Moreover, Table II presents a short description on how the voltage regulator is affected by the considered defects.

For defects injected in the error amplifier, we observe that minimal resistance values of defects occur always at high temperatures. This is because leakage currents in the core-cell array increase at high temperatures, which slightly reduces *Vreg* when compared to low temperatures. Therefore, at high temperatures, lower resistance values are required to degrade *Vreg* to a level that causes DRFs.

We can also observe that *Df16*, *Df19* and *Df29* are the most critical defects in the error amplifier, as they provoke DRFs for lower resistance values compared to other defects. Furthermore, we can verify that minimal resistance values causing DRFs, for each defect, are lower in CS_5 compared to CS_2, regardless of the fact that both CSs lead to the same DRV_{DS}. This occurs because in CS_5 more core-cells start flipping when *Vreg* approaches DRV_{DS}. This extra current demanded from the voltage regulator increases the degradation of *Vreg*.

It is important to note that, if we consider other implementations of the voltage regulator, malfunctions always lead to a regulated voltage that is either higher or lower than expected, which can either increase the static power consumption in DS mode or cause DRFs, respectively. Therefore, malfunctions of a voltage regulator will always impact the SRAM in the same two ways as observed in this work, regardless of voltage regulator design.

V. FAULT MODELING AND TEST SOLUTION

In this section, we first adapt the definition of data retention faults [10] to the case observed in low-power SRAMs, as follows:

Data retention fault in DS mode **(DRF_{DS})**: in DS mode, the regulated voltage *Vreg* is reduced to a level such that the core-cell array supply voltage is lower than DRV_{DS} of the SRAM. As a consequence, one or more core-cells in the array loose the stored data.

A DRF_{DS} can be classified as a dynamic fault, since its sensitization requires three operations. First, the SRAM must be switched from ACT to DS mode. Secondly, the SRAM must be switched back to ACT mode, which is referred to as wake-up phase, and finally a read operation must be executed in all core-cells to verify if data previously stored have been retained in DS mode.

Now, we propose a new March test [10], called March m-LZ, targeting the sensitization and detection of DRF_{DS}. The structure of March m-LZ is the following:

March m-LZ = { ↕(w_1); *DSM*; *WUP*; ↑(r_1, w_0, r_0); *ME1* *ME2* *ME3* *ME4*

DSM; *WUP*; ↑(r_0) } *ME5* *ME6* *ME7*

It is an extended version of March LZ [13], which has been proposed to detect faulty behaviors induced by malfunctions of peripheral circuitry power gating. In March m-LZ, notation *DSM* represents the operation of switching from ACT to DS mode, whereas notation *WUP* refers to the wake-up phase. Considering *DSM* and *WUP* as operations of complexity 1, March m-LZ has a length of 5*N*+4, where *N* is the size of the SRAM in bits or words.

March element ME1 initializes the core-cell array with logic '1', while ME2 switches the SRAM from ACT to DS mode. Next, *WUP* turns the SRAM back into ACT mode, so that ME4 is applied. The r_1 operation in ME4 verifies if logic '1' has been retained in all core-cells during the period of time when the SRAM was in DS mode. Operations w_0 and r_0 in ME4 refer to the sensitization and detection of faulty behaviors associated to peripheral circuitry power gating [13]. When the execution of ME4 finishes, all core-cells are expected to hold logic '0'. The SRAM is then turned into DS mode (ME5), followed by wake-up phase (ME6). Finally, operation *r0* in ME7 verifies if logic '0' has been retained in all core-cells when the SRAM was in DS mode.

Normally, the proposed test should be applied for all 12 possible combinations of V_{DD} (1.0V, 1.1V, 1.2V) and *Vref* (four voltage levels). Despite the high test time, such test flow is efficient to test all studied defects in the voltage regulator. However, test time can be drastically reduced if we determine a test flow that can also detect all studied defects, but executing the proposed algorithm less than 12 times.

Table III presents an optimized test flow that we propose in this paper. This flow involves executing March m-LZ only 3 times. Columns 3 to 6 describe the test conditions for each iteration. First, we configure the voltage regulator such that *Vreg* is expected to be as close as possible to the worst-case DRV_{DS} (730mV), in each iteration. Hence, a small variation on *Vreg*, which can cause a DRF_{DS}, is immediately detected by the test. Secondly, our test flow also considers some particularities discussed in Section IV.B. For some defects injected in the voltage source, we have shown that DRF_{DS} occurrence can be maximized depending on the chosen value of *Vref*. For example, we have shown that lower resistance values of *Df3* are required to cause DRF_{DS} if the voltage regulator is configured such that *Vref* is expected to be either $0.70*V_{DD}$ or $0.64*V_{DD}$. Hence, such condition maximizes the possibility of detecting *Df3*. In our test flow, we have chosen values for *Vref* such that the conditions to maximize the detection of each defect are met at least once at the end of all 3 iterations. The 1st iteration of our flow maximizes the detection of the most part of defects (as highlighted in Table III). The 2nd and 3rd iterations are mainly devoted to detect *Df3* and *Df4*, respectively. We also recommend executing the proposed test flow at high temperatures, since it maximizes the possibility of detecting the most part of studies defects.

The proposed test flow also considers the period of time during which the SRAM is kept in DS mode. When the core-cell array is supplied at a voltage level that is close to the DRV_{DS}, the internal nodes of less stable core-cells that store logic '1' discharge slowly due to leakage currents. Therefore, an eventual DRF_{DS} can be detected only if the SRAM remains in DS mode for a period of time that is sufficient for the core-cell to flip its contents. Thus, the period of time the SRAM stays in DS mode is an important parameter of the test that must be maximized, without critical test time penalties. In our test flow, we suggest to keep the SRAM in DS mode for at least 1ms (refer to column *DS time* in Table III), which is the amount of time we used in our experiments.

TABLE III. *OPTIMIZED TEST FLOW*

		Test Conditions			
Iteration	***Tested Defects***	V_{DD}	*Vref*	*Vreg*	**DS time**
1	***Df1*, *Df2*** and ***Df5* to *Df32***	1.0V	$0.74*V_{DD}$	0.740V	1ms
2	*Df1*, *Df2*, ***Df3*** and *Df5* to *Df32*	1.1V	$0.70*V_{DD}$	0.770V	1ms
3	*Df1*, *Df2*, *Df3*, ***Df4*** and *Df5* to *Df32*	1.2V	$0.64*V_{DD}$	0.768V	1ms

As a final remark, we observe that the proposed test flow can detect the presence of all studied defects by executing March m-LZ only 3 times, whereas 12 iterations are required without test optimization. Therefore, our method can reduce the overall test time by 75%.

VI. CONCLUSION

In this paper we investigated the root cause of data retention faults due to voltage regulator malfunctions. This analysis has been done in presence of core-cells affected by *Vth* variations. Based on the previous analysis, we generated an optimized test flow targeting data retention faults in low-power SRAMs. The adopted methodology can be applied to any similar low-power SRAM design.

REFERENCES

[1] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage current mechanism and leakage reduction techniques in deep-submicrometer CMOS circuits", Proc. of IEEE, vol. 91, pp. 305-327, 2003.

[2] A. Agarwal, S. Mukhopadhyay, C. H. Kim, A. Raychowdhury and K. Roy, "Leakage power analysis and reduction: models, estimation and tools", Computers and Digital Techniques, vol. 152, pp. 353-368, 2005.

[3] Semiconductor Industry Association (SIA), "International Technology Roadmap for Semiconductors (ITRS)", 2011 edition.

[4] S. Narendra and A. Chandrakasan, "Memory Leakage Reduction: SRAM and DRAM specific leakage reduction techniques", in *Leakage in Nanometer CMOS Technologies*, ISBN: 0387257373, Springer, 2005.

[5] K. Flautner et al, "Drowsy caches: simple techniques for reducing leakage power", Proc. of ISCAS, pp. 148-157, 2002.

[6] J. Wang et al, "Statistical modeling for the minimum standby supply voltage of a full SRAM array", in 33rd European Solid State Circuits Conference, 2007.

[7] A. Kumar et al., "Fundamental data retention limits in SRAM standby experimental results", in Quality Electronic Design, 2008.

[8] S. Mukhopadhyay, H. Mahmoodi-Meimand, K. Ray, "Modeling and estimation of failure probability due to parameter variations in nanoscale SRAMs for yield enhancement", Proc. of IEEE Symposium on VLSI Circuits, pp 64-67, Jun. 2004.

[9] A. Bosio et al., "Advanced Test Methods for SRAMs Effective Solutions for Dynamic Fault Detection in Nanoscale Technologies", ISBN: 978-1-4419-0937-4, Springer, 2009.

[10] A. J. van de Goor, "Testing Semiconductor Memories: Theory and Practice", John Wiley & Sons, Chichester, England, 1991.

[11] S. Hamdioui et al, "March SS: a test for all static simple RAM faults", Proc. of IEEE MTDT, pp. 95-100, 2002.

[12] L. B. Zordan et al., "Failure analyzis and test solutions for low-power SRAMs", Proc. of IEEE Asian Test Symposium, pp. 459-460, 2011.

[13] L. B. Zordan et al., "Low-power SRAMs power mode control logic: failure analysis and test solutions", IEEE International Test Conference, CDRom Proceedings, paper 14.3, 2012.

[14] E. Seevinck, F.List, J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells", IEEE Journal of Solid State Circuits, Vol. 22, No. 5, pp. 748 – 754, 1987.