Uncorrelated Power Supply Noise and Ground Bounce Consideration for Test Pattern Generation

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HAL Id: lirmm-00806774
https://hal-lirmm.ccsd.cnrs.fr/lirmm-00806774v1

Uncorrelated Power Supply Noise and Ground Bounce Consideration for Test Pattern Generation

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Abstract—Power supply noise and ground bounce can cause considerable path delay variations. Capturing the worst case power supply noise at a gate level is not a sufficient indicator for measuring the worst case path delay. Furthermore, path delay variations depend on multiple parameters such as input stimuli, cell placement, switching frequency, and available decoupling capacitors. All these variables obscure the rapport between supply noise and path delay and make the selection of stimuli for worst case path delay a difficult task during test pattern generation. In this paper, we utilize power supply noise and ground bounce distribution along with physical design data to generate test patterns for capturing worst case path delay. We propose accurate close-form mathematical models for capturing the effect of power supply noise and ground bounce on path delay. These models are based on modified nodal analysis formulation of power and ground networks, where current waveforms are obtained from levelized simulation and cell library characterization. The proposed test pattern generation flow is a simulated-annealing-based iterative process, which utilizes mathematical models for capturing the impact of supply noise on path delay for a given input pattern. We perform experiments on ITC'99 benchmarks and show that path delay variation can be considerable if test patterns are not properly selected.

Index Terms—Automatic test pattern generation (ATPG), deep submicrometer, delay test, ground bounce, pattern selection, power supply noise, timing analysis.

I. Introduction

THE ONGOING miniaturization of circuits at the nanometer regime has introduced significant changes on the device's parasitics and behavior. Circuit densities increase with each nanotechnology generation because of smaller devices and larger dies, and, consequently, current density and total current consumption increase accordingly. Simultaneously, circuits with high switching frequencies impose faster current transients on power and ground distribution networks. Transient currents increase exponentially with each technology node and cause significant deviations on the voltage distribution. Such deviations of the voltage levels from their nominal values are referred to as "power supply noise and ground bounce." Both these conditions are undesirable, as they significantly impact signal propagation. Analysis shows that power supply noise and ground bounce can considerably affect circuit's performance [1]. Furthermore, simulations show that delay can have a speed-up/slow-down effect depending on the noise conditions on the neighboring gates and/or the crosstalk between gates as shown, respectively, by [2] and [3]. We consider the *uncorrelated* behavior of power supply noise and ground bounce (independent noise peaks and frequencies) in order to represent them as realistically as they would occur in an actual design. Gates can be placed in different locations on chip and they do not experience the same power or ground noise due to temporal and spatial switching. Also, power and ground parasitics for each cell can vary because of their proximity to the nearest power and ground pins. Moreover, as all gates share the same power and ground network, there is also noise transfer that occurs from one region to its neighboring regions, which can cause further delay variations. Another important factor that leads to uncorrelated noise is the amount of decoupling capacitance available at a given region. In general, decoupling capacitors are not evenly distributed, resulting in different amounts of generated noise. Owing to the aforementioned reasons, we treat power supply noise and ground bounce as uncorrelated.

Traditionally, the impact of power supply noise on delay was considered at the cell library development step where each cell was characterized for the worst case voltage drop. Such approach assumes that all cells experience the worst case voltage drop, which is unrealistic. Several other approaches have been proposed in the literature which can be grouped into two main areas: 1) power supply noise aware timing analysis methods and 2) power supply noise aware test pattern generation. In the first group, there has been a substantial amount of work on how to estimate power supply noise-induced worst case delay, notably [4]–[9]. In [4], the authors propose a method to compute the upper bound of circuit delay under voltage variations. A vectorless approach is presented in [5] to estimate the maximum delay under power supply noise, and a delay maximization problem is formulated as an optimization problem. Similarly, the authors in [6]–[9] provide a worst case delay analysis taking into account power supply variations. In the second group of works, such as [10]–[14], the authors propose different techniques for test pattern generation while considering the impact of power supply noise. These works target critical path delay maximization under power supply noise while maximizing switching activity using approaches based either on the Monte Carlo

method or on genetic algorithms. These existing delay-testing and timing-analysis techniques capture worst case timing scenarios which might not reflect the worst case circuit delay. This is due to the following: 1) the model is based on simplified logic-level delay fault models, where physical design information such as the $\{R, L, C\}$ parasitics of the circuits, package, power/ground network, and available decoupling capacitor information are ignored; 2) the combined and uncorrelated impact of power supply noise and ground bounce is not considered which can lead to either delay speedup or slowdown; and 3) impact of resonance frequency on path delay is ignored. Power supply noise and ground bounce in the range of resonance frequencies have been shown as the dominant noise component for high-performance microprocessors [15]. For the reasons mentioned above, we believe that test pattern generation in presence of supply noise deserves reexamination and an effort to understand and capture the interdependencies among path delay variations and noise conditions.

In this paper, we propose a pattern generation technique that takes into account combined effect of power supply noise and ground bounce on path delay as a function of applied inputs. Noise impact on delay is highly dependent on the applied input patterns. We provide mathematical models to represent the circuit based on physical extracted data after it has been placed and routed with power/ground grids. We propose close-form mathematical models to capture the impact of input patterns on path delay in the presence of power supply noise and ground bounce. We use a simulated annealing (SA)-based approach to find patterns that maximize critical path delay. Our method generates patterns to cause such power supply noise and ground bounce distribution that leads to maximum path delay. The contributions of this paper are summarized as follows.

1) We propose accurate and close-form mathematical models to derive the impact of input test patterns on path delay in the presence of noise.
2) We propose a path delay calculation method that takes into account the amount of noise on neighboring cells and switching frequency.
3) We propose a test pattern generation flow that takes into account circuit physical design data (i.e., parasitics, pad/pin location, and cell placements) and speed-up/slow-down effects of noise on path delay.
4) The proposed technique is versatile and can be utilized for delay testing and/or timing analysis techniques.

Furthermore, in contrast to previous works which initially aimed to find patterns for maximum supply noise and then compute delay, our method targets directly to find the worst case delay which might not necessarily occur under worst case power supply noise due to path delay speed-up/slow-down phenomena from the noise conditions on neighboring gates.

The rest of this paper is organized as follows. A motivational example is presented in Section II. The delay model considering power supply noise and ground bounce is presented in Section III. In Section IV, we present our test pattern generation flow in the presence of power supply noise and ground
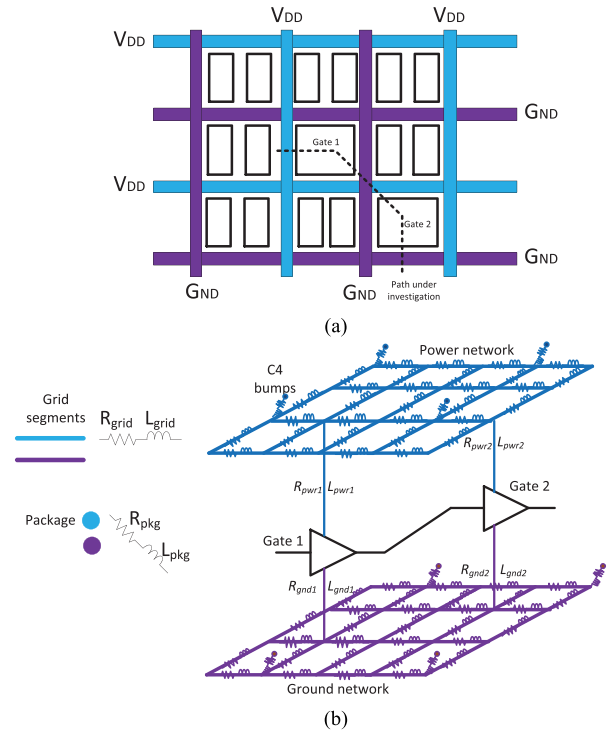

Fig. 1. (a) Illustration of gate placement on chip and (b) representative model for the two-stage buffer circuit used for path delay analysis in the presence of power supply noise and ground bounce.

bounce. Experimental results are presented in Section V. We conclude this paper in Section VI.

II. MOTIVATIONAL EXAMPLE

Power supply noise and ground bounce can cause path delay variations. To highlight the impact of power supply noise and ground bounce on path delay, we provide the analysis of a sample circuit as shown in Fig. 1. A similar analysis was performed in [3] and [5], but we extend such analysis on mesh networks along with decoupling capacitors for capturing the impact of supply noise and resonance frequency on the path delay.

In this paper, we consider on-die power and ground networks along with controlled-collapse chip-connection (C4) package bumps, on-chip decoupling capacitors, and switching circuits. Printed circuit board parasitics are not considered and are beyond the scope of this paper. The sample circuit is a two-stage buffer chain implemented in 90 nm with $V_{DD} = 1$ V. As shown in Fig. 1(a), the buffer gates share the same global power and ground networks, however, they can be placed in different locations and proximities from the power and ground pins. Fig. 1(b) shows the circuit model which we utilize for our analysis. Power and ground networks are represented with their extracted parasitics of resistance R, capacitance C, and self-inductance L. We ignore mutual inductances. The extracted values are based on the dimensions of power/ground tracks as used in [16]. We include package parasitics represented by extracted R and L values as described in [17].

TABLE I
IMPACT OF VOLTAGE DROP ONLY ON DELAY

	Gate 1	Gate 2	Delay Ratio	% Impact
No ground bounce	-0.1V (voltage overshoot)	-0.1V	0.88	23% speed-up
		0V	1.014	1.4% slow-down
		0.1V	1.2	20% speed-up
	0V (no voltage droop)	-0.1V	0.86	14% speed-up
		0V	1	Nominal delay
		0.1V	1.18	18% slow-down
	0.1V (voltage droop)	-0.1V	0.83	17% speed-up
		0V	0.95	5% speed-up
		0.1V	1.16	16% slow-down

TABLE II
IMPACT OF GROUND BOUNCE ONLY ON DELAY

	Gate 1	Gate 2	Delay Ratio	% Impact
No power supply noise	No ground bounce	No ground bounce	1	Nominal delay
	No ground bounce	0.1V ground bounce	0.98	0.2% speed-up
	0.1V ground bounce	No ground bounce	1.074	7.4% slow-down
	0.1V ground bounce	0.1V ground bounce	1.042	4.2% slow-down

Fig. 2.   Path delay variation in presence of power supply noise.

Fig. 3.   Path delay map as a function of ground bounce only.

We perform HSPICE transient analysis on the sample circuit and measure delay variations as a function of power supply noise and ground bounce. In the following subsections, we report on path delay variations by performing: 1) stand-alone power supply noise analysis; 2) stand-alone ground bounce analysis; and 3) combined power and ground noise analysis with respect to resonance frequency.

A. PSN Impact on Delay Variations

In this experiment, to capture the impact of power supply noise only, the ground network is considered ideal. Delay is plotted as a function of measured maximum power supply noise (represented as voltage drop) on each gate, as shown in Fig. 2. Delay variations are plotted as delay ratios with respect to nominal delay with no noise on the circuit. Negative (positive) values on the x- and y-axis present the measured voltage overshoot (undershoot) from V_{DD}. Table I presents the percentages of delay variations. Two observations from this experiment can be made. 1) Depending on the noise conditions on each gate, path delay can increase/decrease. 2) The worst case voltage droop on both gates does not lead to worst path delay.

B. Ground Bounce Impact on Delay Variations

The same circuit is used to analyze the impact of ground bounce on delay. Fig. 3 shows the path delay map as a function of measured ground bounce on each gate. Table II shows the percentages of path delay variations. The main observation from this analysis is that the worst path delay does not occur when both gates experience worst case ground bounce. As shown in Fig. 3, the worst case path delay is on lower right-hand corner of the map, when gate 1 has the largest ground bounce and gate 2 has no ground bounce.
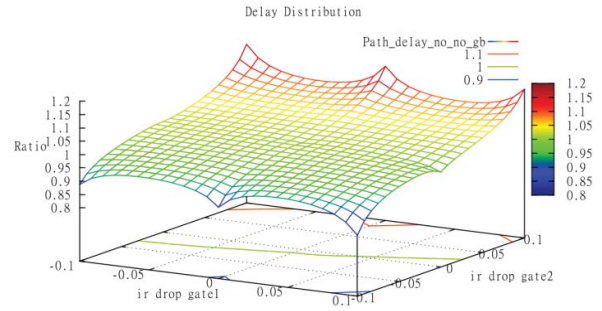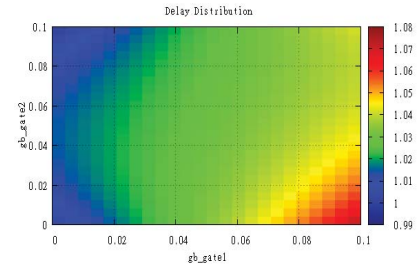
C. Uncorrelated PSN and Ground Bounce Impact on Path Delay

In this experiment, we perform path delay analysis with both power supply noise and ground bounce. We use the same two-buffer circuit. Figs. 4 and 5 show different path delay variations with respect to power supply noise and ground bounce. The delays are represented as ratios with respect to nominal delay with no noise.

Path delay variations are plotted for four cases: 1) both gates have no ground bounce [Fig. 4(a)]; 2) only gate 2 experiences ground bounce [Fig. 4(b)]; 3) only gate 1 experiences ground bounce [Fig. 4(c)]; and 4) both gates experience ground bounce [Fig. 4(d)]. We observe that considering uncorrelated power and ground noise introduces further delay variations. For example, there is a decrease on path delay when gate 2 suffers from ground bounce versus the case when both gates have no ground bounce as shown in Fig. 5(a). In Fig. 5(a), there are two delay distribution layers where one layer shows delay distribution with no ground bounce on both gates (red layer) and the other layer shows delay distribution with ground bounce on gate 2 only (green layer). Their overlap shows the delay speed-up effect that occurs when gate 2 has ground bounce. In the case when only gate 1 has ground bounce, there is a slow-down effect as shown in Fig. 5(b).

We repeat the above experiments with varying input signal switching frequency between 150 MHz to 1 GHz in order to capture path delay variations with resonance frequency. Resonance frequency on chip is created due to large package inductance L and on-chip capacitance C, which together create a series LC tank. The LC tank creates an oscillator where energy is being transferred between the inductance and capacitor leading to excessive voltage harmonics on power and ground networks. Moreover, as power and ground networks
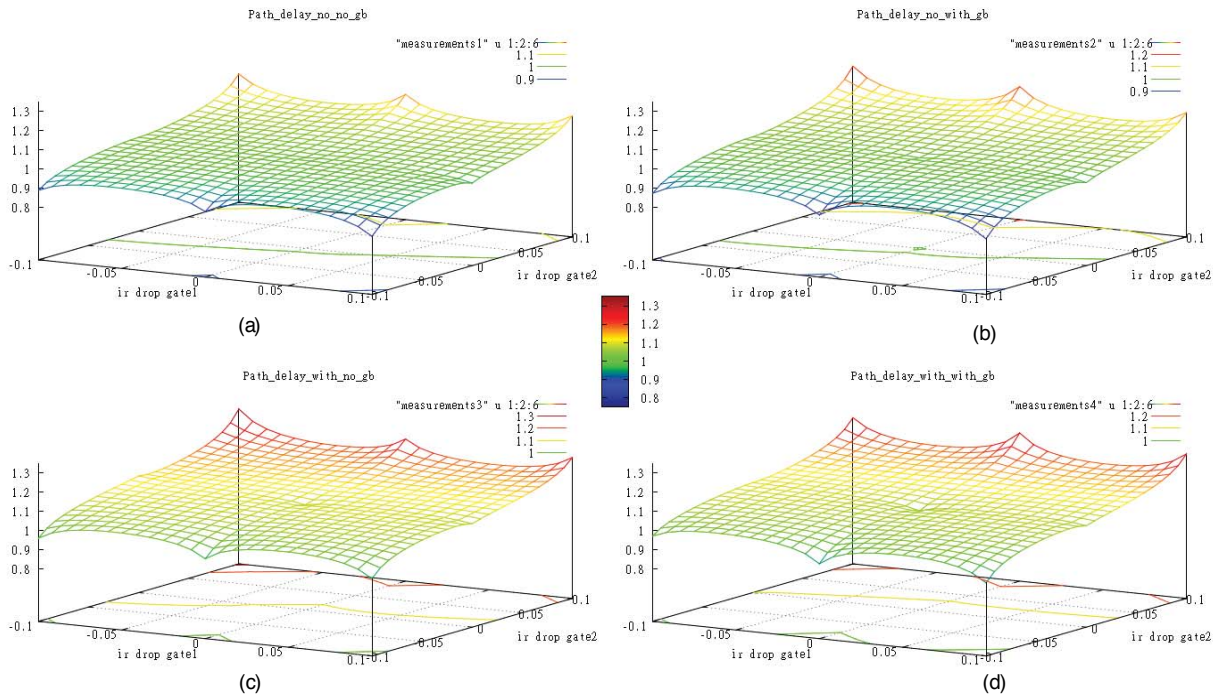
Fig. 4. Path delay variations as a function of power supply noise on both gates. (a) No ground bounce on any of the gates. (b) Ground bounce only on gate 1. (c) Ground bounce only on gate 2. (d) Ground bounce on both gates.
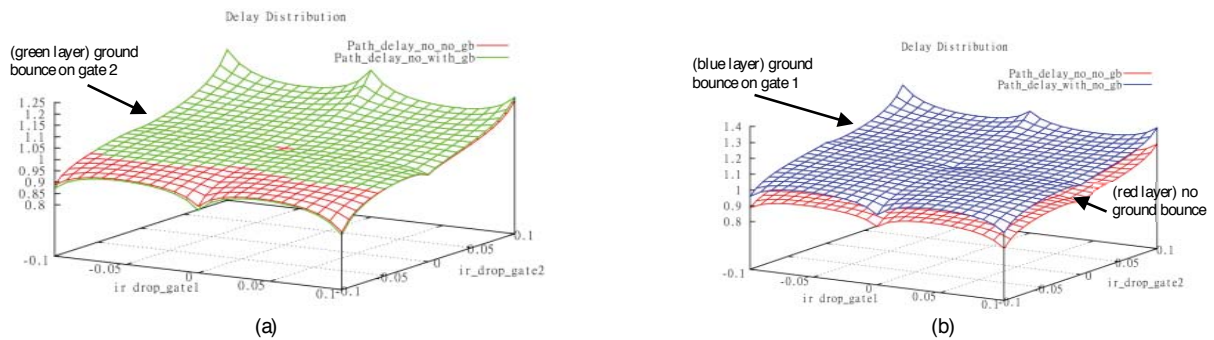

Fig. 5. Path variations with power and ground supply noise showing speedup and slowdown. (a) Ground bounce injected on gate 2. (b) Slowdown when ground bounce injected on gate 1.

cover a significant on-chip area, they provide a large amount of parasitic resistance (R), inductance (jwL) and capacitance ($1/jwC$), which are sensitive to frequency (w) variations and can considerably change network impedance $Z = R + jwL + 1/jwC$. Consequently, power and ground network impedance increases with resonance frequency which further increases the supply noise. In [16], the authors have studied the impact of package inductance at different frequencies to estimate the amount of supply noise generated. They have concluded that there are high- and mid/low-frequency supply noises generated. High-frequency noise is a localized phenomenon due to the effect of the neighboring decoupling capacitors. The mid- to low-frequency resonance have a larger and an additive impact on every neighboring gate, further overwhelming each gate's localized high-frequency effects. In our experiment, we measure path delay variations with varying switching frequency.

Power supply noise is derived by integrating the supply voltage over switching period such as $noise = \int_{ts}^{te}(V_{\text{DD}} - V_t)$ where ts and te are the starting and ending switching times. The measured noise represents the area of voltage drop under nominal voltage level. Ground bounce is similarly measured. Fig. 6 depicts the area for representing power supply noise.

In Fig. 7, we show the measured supply noise on each buffer gate as a function of the switching frequency of the input signal. We observe two resonance peaks from each buffer gate. The first gate has a peak on the supply noise around 250 MHz, while the second gate has a peak on supply noise around 500 MHz. This is due to the coupling of the package inductance with capacitance of each gate thereby creating two mid-frequency resonance effects. Fig. 7 also shows the path delay variation as a function of the switching frequency. Resonance frequency further complicates the relationship between supply noise and delay and makes the selection of stimuli for
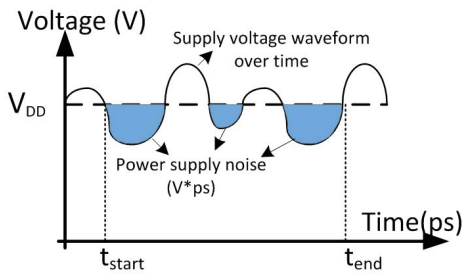
Fig. 6.   Illustration of power supply noise measurement.

Fig. 7.   Supply noise and path delay variations with switching frequency.

the worst case path delay a difficult task during test pattern generation.

From these experiments, we observe the effect of uncorrelated power supply noise and ground bounce on path delay as follows: 1) performance degradation due to reduced voltage level between power and ground; 2) delay increase/decrease due to noise conditions on a gate and its neighboring gates; and 3) augmented supply noise and increased path delays due to the resonance frequency.

Thus, path delay variations are dependent on multiple variables such as input stimuli, physical placement, package parasitics, resonance frequency, and available decoupling capacitors. Hence, capturing the worst case delay by considering all these variables is a complicated task. In the following section, we describe our models and pattern generation method in the presence of power supply noise and ground bounce.

III. DELAY MODEL FOR POWER SUPPLY NOISE AND GROUND BOUNCE

In this section, we present our approach for modeling the effect of power supply noise and ground bounce on path delay. Our approach consists of two main parts: 1) current derivation process and 2) path delay circuit analysis. Pattern generation flow iterates between these two processes to identify the input stimuli that generate the worst case path delay in the presence of power supply noise and ground bounce.

A. Current Derivation Process

In this step, we derive the amount of current drawn by switching gates on the circuit. Power supply noise and ground bounce are dependent on the instantaneous currents flowing through power and ground networks and their parasitic impedance values. Accurate current waveforms must be obtained in order to accurately derive the amount of noise on the circuit. The process of deriving the current consumed by each gate is organized in three steps: 1) library characterization; 2) circuit levelization; and 3) current derivation.

1) Library Characterization: Here, we derive the current waveform for each cell in the library as a function of its primary input conditions. SPICE netlist of each cell is simulated and current waveforms with respect input patterns are obtained. We store the current characteristics, i.e., peak current I_p, leakage current I_l, transition time t_r, and peak
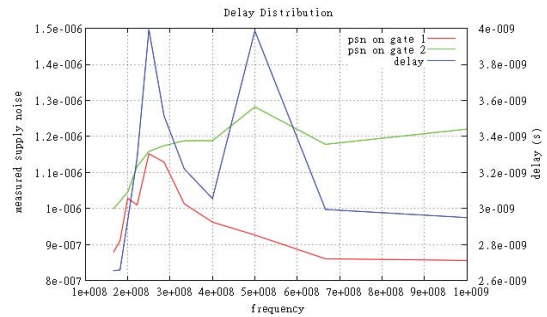
time t_p, for each input condition in a lookup table (LUT). Such characterization allows us to transform each cell into a current source (triangular waveform) model appropriate to its input conditions.

These waveforms are computed only once and are used during the test pattern generation step for identifying the current consumption based on a given input pattern. We note that current waveform characteristics $\{I_p, I_l, t_r, t_p\}$ are obtained for ideal power and ground conditions. These current models are later inserted on the actual power and ground networks for more accurate power and ground network analysis.

2) Circuit Levelization: The objective of this step is to obtain input transitions for each gate on the netlist. We utilize a levelized simulation algorithm in order to propagate the transitions from primary inputs to primary outputs [18], [19]. The algorithm begins with primary inputs that are assigned a level number zero. A level number can be assigned to a gate only if all gate inputs have been assigned level numbers. Similarly, a net can be assigned a level number only if all driving gates have been assigned level numbers. The level assignment process is iterative until all the nets and gates on the netlist have been levelized and primary outputs have been reached. Once the netlist is levelized, we perform levelized simulation where primary input transitions are propagated in an orderly fashion throughout the gates on the netlist.

We note that there exist other methods and commercial tools that perform waveform simulation for a given input pattern [20], [21]. We employ the levelized simulation algorithm which is incorporated in our pattern generation flow.

3) Current Derivation: After the netlist is levelized and input transitions are propagated through each gate, we derive each gate's appropriate current waveform. The idea is to utilize LUTs obtained from library characterization step in order to represent each gate as a current source model.

As we propagate transitions throughout the netlist, there are two main tasks being performed: 1) current modeling based on LUT match-up with input transitions and 2) delay accumulation as transitions are propagated in the levelized netlist. The first task serves to identify the current source $\{I_p, I_l, t_r\}$, while second task serves to identify peak transition time $\{t_p\}$. By keeping track of $\{t_p\}$ for each cell, we ensure that in a given clock cycle all cells are not switching at the same time but rather shifted in time by the accumulated delay for each level of the netlist. The delay of each level of the
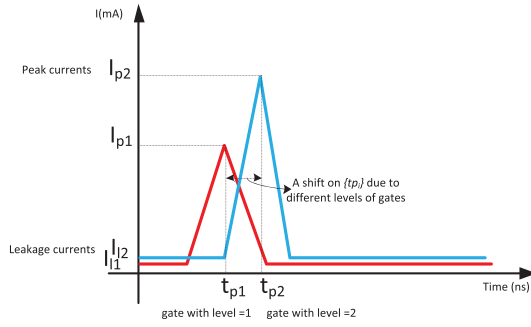
Fig. 8. Illustration of the current source model for different gates on the levelized netlist.

netlist is based on

$$\text{delay}_{\text{level}} = \sum_{i=1}^{nr \text{ of levels}} \text{delay}_{\text{gate}_i}. \tag{1}$$

Fig. 8 illustrates such a concept where the current waveform of the gate with level 1 has peak time $\{tp_1\}$ and the gate with level 2 has peak time $\{tp_2\}$.

In this step, as we still have not derived the actual gate delay, we utilize the gate delay measured with an ideal power and ground network. We note that the levelized delay is simply used for representing realistically the switching times of current sources as they would occur during circuit's operation. Gate delays in the presence of supply noise are derived in the next section.

In summary, our objective is to obtain fast and accurate current source models according to input transitions of the circuit. The derived current source models are a function of input patterns as

$$I = f(\text{patterns}) \tag{2}$$

where *patterns* represent the input conditions and I is the current vector of size $n \times 1$ where n is the total number of nodes on the circuit for both the power and ground networks. We note that not every node has a current source attached to it. In the following subsections, we introduce circuit modeling concept which takes into consideration cell placement.

B. Path Delay Circuit Analysis

The key objective of this paper is to utilize circuit physical design information that is extracted after placement and routing. We devise physical design data in mathematical models for performing accurate power supply noise and ground bounce analysis with respect to applied input patterns. Computed power supply noise and ground bounce are then used to derive each gate's delay while considering noise conditions on its neighboring gates and switching frequency. We develop a flow where path delay is derived with respect to power/ground parasitics and input stimuli are represented as switching current sources and switching frequency.

Path delay circuit analysis is performed in three steps: 1) circuit modeling; 2) power supply noise and ground bounce derivation; and 3) path delay calculation.

1) Circuit Modeling: In this paper, we utilize the circuit netlist that is extracted after the design has been placed and routed and power/ground networks are inserted. The extracted netlist provides R, L, and C parasitic information of the circuit, package, power/ground networks, and pin/cell placements. Power and ground networks are modeled by using the extracted resistance and capacitance parasitics $\{R_{\text{pwr}}, R_{\text{gnd}}, C_{pg}\}$ while package is modeled by its inductance and resistance parasitics $\{R_{\text{pkg}}, L_{\text{pkg}}\}$. Note that we only consider self-inductance and ignore mutual inductance on power/ground networks. While mutual inductance can alter power grid impedance, it also results in excessively large analysis runtimes. As the goal of this paper is to identify quickly and accurately the impact of input patterns on path delay in presence of power supply noise and ground bounce, we ignore mutual inductances.

Current sources inserted between power and ground networks are current models obtained from current derivation process in the previous section. Their locations are derived from cell placement data of the extracted netlist. The initial circuit netlist in verilog and commercial CAD tool (Cadence SoC Encounter[1]) is used for place and route and generate the extracted netlist.

Fig. 9 shows the physical layout design for a sample circuit from ITC'99 benchmarks and a simplified two-cell circuit to represent modeling. We note that, for the circuit sample in Fig. 9, ground and power network is represented as a mesh topology, however, tree topologies can also be extracted depending on the design style.

The goal of the circuit modeling step is to represent physical design information of the circuit in a mathematical model which we can accurately analyze. We utilize the modified nodal analysis (MNA) [22] approach to represent the extracted circuit into a mathematical model using Kirchhoff's law node equations as in (3) and (4)

$$(G_{nxn} + sC_{nxn})V_{nx1} = l_{nx1} \tag{3}$$

$$\left(\begin{bmatrix} G_{11}^p & \cdots & G_{1m}^p & 0 & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ G_{m1}^p & \cdots & G_{mm}^p & 0 & \cdots & 0 \\ 0 & \cdots & 0 & G_{11}^g & \cdots & G_{1m}^g \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & G_{m1}^g & \cdots & G_{mm}^g \end{bmatrix} \right.$$
$$+ s \left. \begin{bmatrix} C_{11} & \cdots & 0 & -C_{11} & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & C_{mm} & 0 & \cdots & -C_{mm} \\ -C_{11} & \cdots & 0 & C_{11} & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & -C_{mm} & 0 & \cdots & C_{mm} \end{bmatrix} \right) \begin{bmatrix} V_1^p \\ \vdots \\ V_m^p \\ V_1^g \\ \vdots \\ V_m^g \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_m \\ -I_1 \\ \vdots \\ -I_m \end{bmatrix} \tag{4}$$

where G_{ij}^p is impedance between nodes i and j in the power network and G_{ij}^g is the impedance between nodes i and j in the ground network. Capacitors between power and ground nodes are represented by C_{ij}. V_j is voltage at node i where the top half of the vector represents power network nodes, V_i^p and bottom half represents ground network nodes, V_i^g where

[1] Available online at http://www.cadence.com/products/di/soc_encounter/pages/default.aspx.
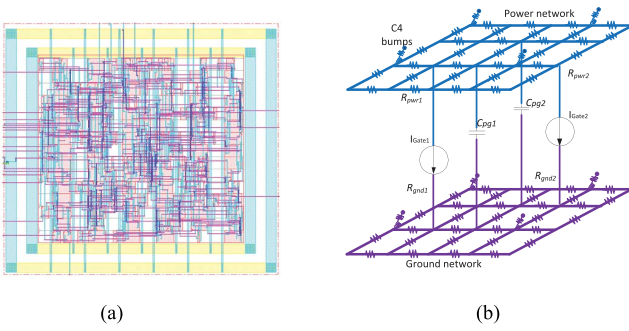
Fig. 9.   (a) Physical design of the circuit. (b) Circuit model representation.

Fig. 10.   Illustration of neighboring cells considered for delay analysis.

$V = [V_i^p, V_i^g]$. Current sources represent the current consumed by the cells connected between power and ground networks, and vector Ii is the current source vector where the top half presents the current sources connected to power network and the bottom half presents the same current source connected to ground grid with opposite current flow. The location of current sources is obtained from cell placement. m is the number of power (ground) nodes where $n = 2 \cdot m$. Some of the nodes on power and ground networks do not have a current source connected to them and these nodes are represented by a zero current source on the I vector. Furthermore, some of the nodes on power and ground networks serve as V_{DD} (G_{ND}) pins, which can be presented by modifying (4) to identify them as voltage sources. We note that mathematical formulation is represented in the frequency domain (s).

2) Power Supply Noise and Ground Bounce Derivation: The mathematical formulation in (4) provides all physical design information of the circuit, where the G and C matrices are obtained from the extracted netlist. Values of the I vector vary according to the applied input stimuli and derived as described in the previous section. Thus, for a given input pattern where G, C, and I are known, the only unknown remains node voltage vector V. Equation (3) is a set of linear equations with n unknowns which can be accurately solved using matrix manipulations. We utilize MATLAB [12] to perform matrix computations where node voltages are expressed as

$$V = (G + sC)^{-1}I. \qquad (5)$$

Node voltages vector V is further used to obtain power supply noise, ground bounce, and supply noise as shown in (6)–(8)

$$PSN_i = \int_{ts}^{te} (V_{DD} - V_i^p)dt \qquad (6)$$

$$GB_i = \int_{ts}^{te} (V_i^g - V_{gnd})dt \qquad (7)$$

$$SN_i = PSN_i + GB_i \qquad (8)$$

where PSNi, GBi, and SNi are the power supply noise, ground bounce, and supply noise for cell i, and t_s, t_e are the starting and ending switching times.

Taking the inverse matrix can be a computationally expensive task, and in this flow we compute inverse matrix only once and utilize it with different I vectors (input patterns) to derive the voltage distribution on power and ground networks.
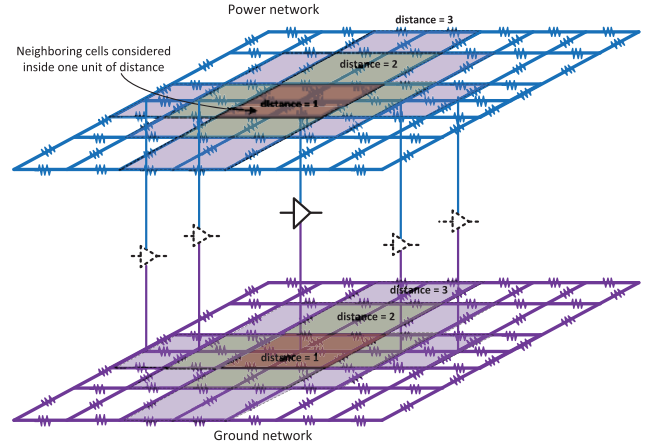
Similarly, computation of power supply noise and ground bounce is performed every time with a new I vector (input pattern). The inverse matrix can be efficiently obtained using various techniques, i.e., model order reduction, exploiting matrix sparsity, multigrid method, etc. It is not the focus of this paper to elaborate on these methods, but there exist efficient solvers for the inverse matrix problem.

3) Delay Characterization: In this step, we aim to capture delay variations as a function of power supply noise and ground bounce on a gate and its neighboring gates. As shown in the motivational example, noise conditions on a cell and its neighboring cells can cause either path delay increase or decrease. Such a phenomenon is further exacerbated in the presence of resonance frequency.

Delay characterization is performed by: 1) deriving the gate delay in presence of power and ground noise, noise impact from neighboring gates, and switching frequency and 2) deriving path delay based on gate delays. We start by characterizing the relationship between gate delay and noise with respect to delay coefficient β_i. For each cell on the library, we perform an HSPICE simulation with different power and ground voltage levels $\{V_i^p, V_i^g\}$ and switching frequency, $\{w\}$ in order to compute its delay variations. These simulations are performed on corner cases, i.e., no, mid- and high-level noise and low, medium, and high switching frequencies. The results obtained are utilized on a regression analysis in order to obtain the *coefficients β_i* that lead to estimate gate delay as in (9)

$$\tau_{cell_i} = \beta_i^p V_i^p + \beta_i^g V_i^g + \sum_{j \in neigh}(\beta_j^p V_j^p + \beta_j^g V_j^g) + \beta_i^w w \quad (9)$$

where β_i^p is delay coefficient from the power node voltage of cell i, β_i^g is delay coefficient from ground node voltage of cell i, β_j^p is delay coefficient from power node voltage of neighboring cell j, β_j^g is the delay coefficient from ground node voltage of neighboring cell j, β_i^w is delay coefficient of cell i for frequency w, and τ_{cell_i} is the delay of cell i.

Neighboring cells are chosen based on the Manhattan distance between them and the cell under investigation. We perform simulation and quantify the impact on path delay from cells located in different Manhattan distances as shown in Fig. 10. Table III provides the experimental results. In this

TABLE III
PROXIMITY OF NEIGHBORING CELLS IMPACT ON CELL DELAY

Neighboring cells included	Delay (s)	% Difference wrt. to actual delay
No neighboring cells	3.22E-10	18.27%
1st distance	3.58E-10	9.14%
1st + 2nd distances	3.65E-10	7.36%
1st+2nd+ 3rd distances (actual delay)	3.94E-10	0%
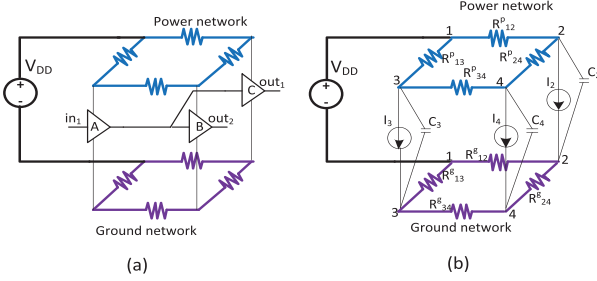
Fig. 11. Sample circuit for illustration of delay analysis with power supply noise and ground bounce.

LUT - INV

Input transitions	Current source model
Low	{0, 0, 0}
High	{0, 0, 0}
Low-to-High	{120uA, 100nA, 0.5n}
High-to-Low	{55uA, 100nA, 0.5n}
Delay coefficients	$\beta_{inv}^p = 8.14e-10$ $\beta_{inv}^g = 9.05e-10$ $\beta_{neighbor}^p = -4.39e-10$ $\beta_{neighbor}^g = -7.16e-10$ $\beta_{inv}^w = 0.0412$

(a)

Circuit netlist

For a given pattern <0,1> (low-to-high)

	Gate A	Gate B	Gate C
level	0	1	1
propagated transitions	low-to-high	high-to-low	high-to-low
tp	1.5n	1.8ns	1.8ns
current source model	{120uA, 100nA, 0.5n}	{55uA, 100nA, 0.5n}	{55uA, 100nA, 0.5n}

(b)

Fig. 12. (a) LUT for INV gate derived from library characterization step. (b) Circuit netlist levelization and current source modeling for each gate.

used to the derive path delay, i.e., the path from cell A to B as shown in (12) by using (9) and (10). We note that $\{\beta\}$ coefficients are already precomputed as described in the previous subsection. The path delay computed from the mathematical equations is 3.9×10^{-10} s versus 4.03×10^{-10} s obtained from HSPICE (3.2% difference). Thus, throughout our flow, we need to compute the inverse of $(G+sC)^{-1}$ only once while vector I will change with respect to the input pattern

$$(G + sC)V = I$$

$$
(11)
$$

experiment, neighboring cells have a slow-down effect on path delay. There is a 22% percentage difference on path delay when no neighboring cells are included versus when all neighboring cells are included. For this experiment, the actual path delay is measurement when first, second, and third unit distance neighboring cells are considered. In the case when only the first distance neighboring cells are considered, we obtain less than 10% path delay difference. In our analyzes, we consider neighboring cells located within one Manhattan distance from the cell under investigation, as shown in Fig. 10.

The *delay coefficients* are derived by solving the linear least square regression. Such mathematical formulation allows us to capture delay speedup/slowdown due to the noise conditions on the current cell and its neighboring cells as a function of the switching frequency. Once regression analysis is performed, the path delay is computed as

$$\tau_{\text{path}} = \sum_{\text{cell}_i \epsilon \text{path}} \tau_{\text{cell}_i}. \tag{10}$$

Here, we provide a sample circuit in which we perform all the aforementioned steps in order to exemplify our flow. Fig. 11 shows a sample model of a three-gate circuit.

The sample circuit has three inverter gates. The current characterization LUT for the inverter is shown in Fig. 12(a). The sample circuit has one input and two outputs. We investigate the rising condition on the input by applying input pattern $<V_1, V_2> = <0,1>$. Levelized circuit netlist, propagated transitions, and the appropriate current source model for each gate are shown in Fig. 12(b). There are four nodes on the power and ground network, respectively, with a total of eight nodes. Equation (11) shows the matrix formulations where G_{8x8}, C_{8x8}, and I_{8x1} are expressed in the Laplace $s-$domain and are known variables. Power and ground node voltages in V_{8x1} are unknown and can be solved accurately using any linear algebra package solvers. Once the node voltages are obtained, they are

$$\tau_{\text{cell}}^A = \beta_A^p V_3^p + \beta_A^g V_3^g + \beta_B^p V_4^p + \beta_B^g V_4^g + \beta_A^w w$$
$$\tau_{\text{cell}}^B = \beta_B^p V_4^p + \beta_B^g V_4^g + \beta_A^p V_3^p + \beta_A^g V_3^g + \beta_C^p V_2^p + \beta_C^g V_2^g$$
$$+ \beta_B^w w$$
$$\tau_{\text{path}}^{AB} = \tau_{\text{cell}}^A + \tau_{\text{cell}}^B. \tag{12}$$

In the next section, we use these mathematical models in our test pattern generation flow in order to accurately determine the impact of the input patterns on the path delay in the presence of power supply noise and ground bounce.

IV. TEST PATTERN GENERATION FLOW CONSIDERING POWER SUPPLY NOISE AND GROUND BOUNCE

To identify path delay faults, a vector pair needs to be applied to the circuit. One solution to finding the maximum
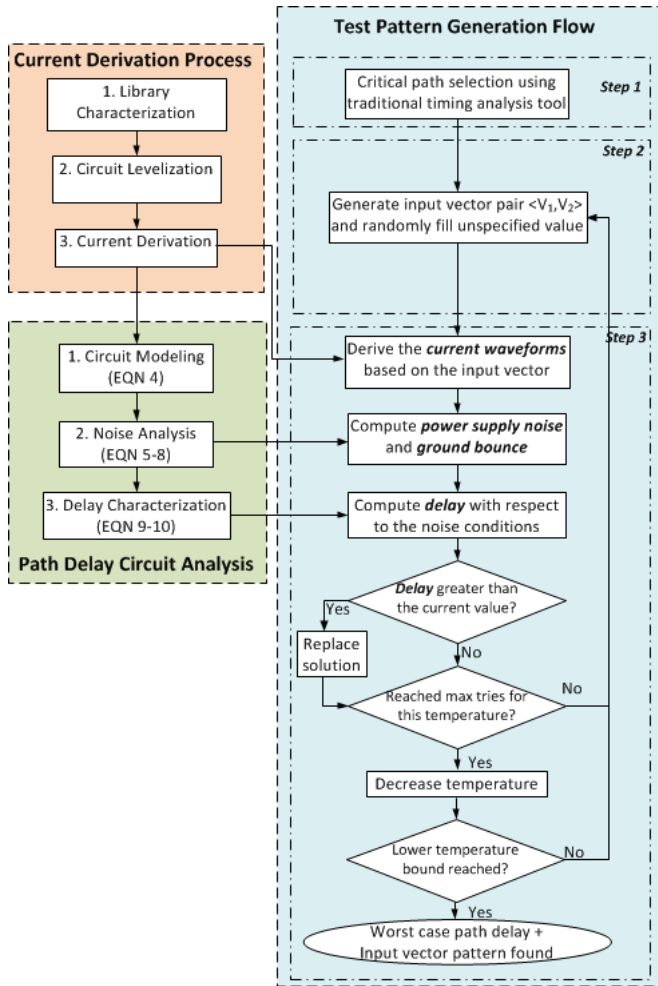
Fig. 13. Test pattern generation flow based on SA iterative process for capturing the worst case path delay in the presence of power supply noise and ground bounce with respect to switching frequency.

TABLE IV

VARIOUS INPUT PATTERNS AND THEIR DELAY AND NOISE MEASUREMENTS FOR THE b01 CIRCUIT

<V1,V2>=(XX011,XX010)

V1=XX011   V2=XX010

Vector Filling <V1,V2>	Delay (s)	Supply Noise (V*s) (SN=PSN+GB)	% Diff wrt min. Delay
(00011,00010)	6.824E-10	2.280E-09	15%
(00011,01010)	6.871E-10	2.877E-09	16%
(01011,00010)	6.708E-10	3.082E-09	13%
(01011,01010)	6.764E-10	2.654E-09	14%
(00011,10010)	6.789E-10	3.081E-09	15%
(00011,11010)	6.895E-10	3.434E-09	16%
(01011,10010)	6.637E-10	2.186E-09	12%
(01011,11010)*	7.040E-10	3.513E-09	19%
(10011,00010)	6.843E-10	3.190E-09	15%
(10011,01010)	6.800E-10	2.329E-09	15%
(11011,00010)	6.659E-10	3.946E-09	12%
(11011,01010)	5.929E-10	3.481E-09	0%
(10011,10010)	6.764E-10	2.655E-09	14%
(10011,11010)	6.889E-10	3.985E-09	16%
(11011,10010)	6.631E-10	3.702E-09	12%
(11011,11010)	6.670E-10	2.955E-09	12%

Selected by our SA-based pattern generation

TABLE V

DELAY VARIATIONS FOR CRITICAL PATHS OF THE b01 CIRCUIT

b01	Delay (s)	PSN (V*s)	GB (V*s)	Supply Noise (PSN+GB)
Path 1 (most critical)	1.98E-10	2.04E-11	2.24E-11	4.28E-11
Path 2	2.12E-10	2.87E-11	4.64E-11	7.51E-11
Path 3	1.87E-10	1.09E-11	1.69E-11	2.78E-11
Path 4 (least critical)	1.76E-10	2.00E-11	3.51E-11	5.51E-11

path delay in the presence of noise is to simulate all possible two-vector patterns for a given circuit. However, this is simply infeasible, as it would require a significantly large number of simulations. We propose a pattern generation flow that makes use of the closed-form equations described in the previous section to estimate delay based on the input patterns in the presence of supply noise.

Our test pattern generation flow for path delay faults considering power supply noise and ground bounce consists of three steps: 1) path selection; 2) vector pair generation; and 3) SA-based pattern generation.

A. Path Selection

We employ the commercial static timing analysis tool Synopsys Primetime [23] to identify the critical paths in the design. Only a small subset of paths is selected by the tool, listing the longest paths based on the timing report. From this small subset, we select only top 10% of critical paths to apply our pattern generation flow. We note that our pattern generation method is independent of the path selection process and it can be applied to any selected path.

B. Vector Pair Generation

Test vectors are generated such that the target path is sensitized under given propagation condition (robust, nonrobust, etc.). As shown in [24], defects on robustly testable paths are guaranteed to be detected regardless of the delays outside the targeted paths, while defects on nonrobustly testable paths can be detected if transitions on certain signals not belonging to the target path are not late.

In this paper, we use the commercial Tetramax ATPG tool [25] to generate partially specified input vector pairs for the selected critical paths. In this step, we attempt to leave as many unspecified (X value) primary input values as possible so that we can apply X filling by considering their impact on path delay in the presence of supply noise.

C. Test Pattern Generation

Different assignments of unspecified primary input values can result in different path delays and supply noise. This is because path delay is dependent on the number of inputs, which are switching and the internal switching activity on the circuit. For the selected critical path, the objective is to generate an *input vector pair* such that the impact of power supply noise and ground bounce on path delay is maximized. We develop a SA-based iterative process in order to evaluate the effect of supply noise on delay for each generated input
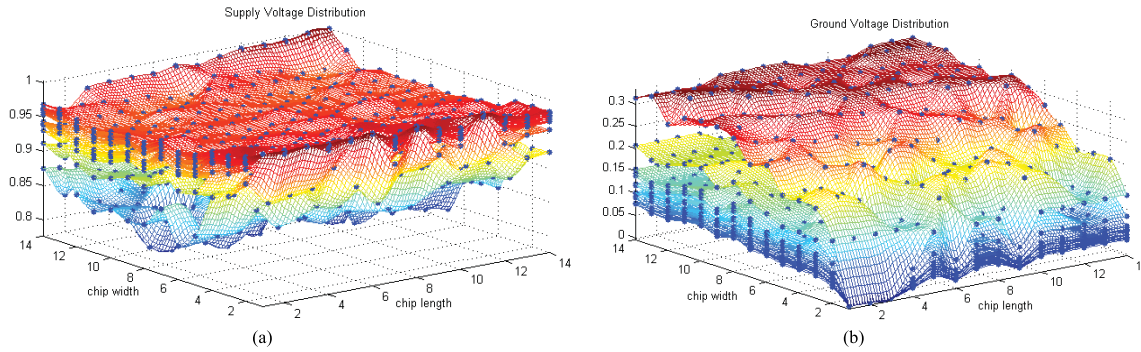
Fig. 14. (a) Voltage distribution on power network for different input patterns for the *b*01 circuit. (b) Voltage distribution on ground network for various input patterns for the *b*01 circuit.
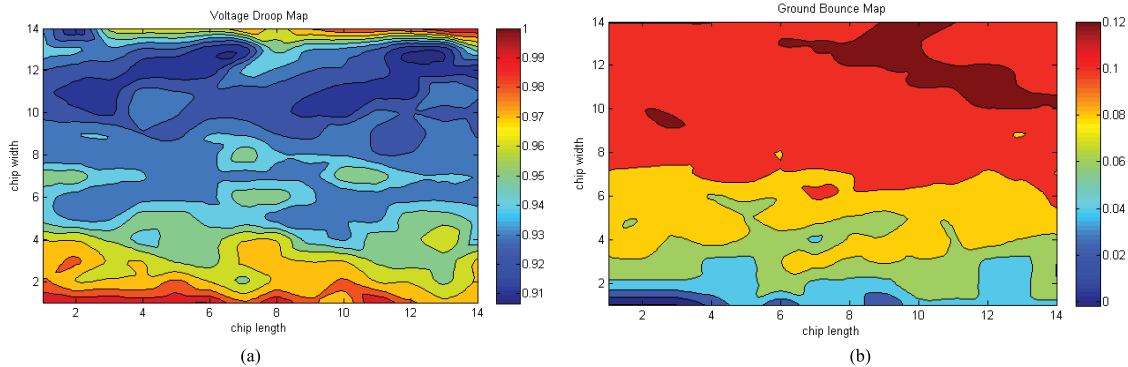

Fig. 15. (a) Voltage drop and (b) ground bounce maps for the *b*01 circuit for the selected input vector from test pattern generation flow.

vector pair. SA is a well-known optimization technique widely used for various applications.

The iterative flow is based on: 1) generating a test vector pattern by filling unspecified primary input values; 2) computing current waveforms by using library characterization data as in Section III-A; 3) computing power supply noise and ground bounce using closed-form equations as in Section III-B; and 4) computing path delay in presence of noise as in Section III-B.

In the first two steps, unspecified input values are randomly filled by either a 0 or 1. Thus, the number of generated patterns is dependent on the number of unspecified input values. In the third and fourth steps, the generated input test pattern is evaluated for supply noise and path delay. Computed path delay serves as the evaluation function for the generated input test pattern. The temperature parameters for SA are set to $T_{i+1} = T_i \cdot CR^{k-1}$, where the cooling rate is $CR = 0.92$ and k is the cooling step in the iteration loop. For each temperature step, equilibrium is reached if there is no more change in path delay for a perturbed input vector configuration. SA iterates among different input patterns in order to identify the pattern that generated the maximum delay in the presence of power supply noise and ground bounce with respect to switching frequency. Fig. 13 illustrates the proposed SA-based approach for pattern generation flow.

V. EXPERIMENTAL RESULTS

Our experiments are conducted on the combinational part of ITC'99 [26] benchmarks which are described in regis-

ter transfer level and synthesized using STMicroelectronics 90-nm cell library with $V_{DD} = 1$ V. The gate level netlists are generated and imported to the SoC Encounter where physical layout information is obtained after power/ground network design, floorplanning, placement, and routing. Timing information and critical path lists obtained from Synopsys PrimeTime along with the circuit netlist are fed to TetraMax to generate input test patterns with unspecified input values (*X* values). In this paper, we use 10% of worst critical path reported from PrimeTime. The extracted netlist with $\{R, L, C\}$ parasitics of the power /ground network, interconnects, and cell placement is then provided to MATLAB[2] where the SA-based test pattern generation is implemented. All the mathematical models and equations described in the previous sections are implemented in MATLAB. The voltage drop constraints were set to 10% of nominal voltage values. The experiments were run on a Linux machine with a speed of 2.5 GHz, memory 4 GB of RAM, and capacity of 250 GB. We studied the effect of power supply noise and ground bounce on path delay and multiple critical path behavior and applied our pattern generation flow on several circuits.

A. Impact of Power Supply Noise and Ground Bounce on Path Delay

We experiment with the *b*01 benchmark of ITC'99 to demonstrate the impact of power supply noise and ground bounce on path delay.

[2]Available online at http://www.mathworks.fr/.

TABLE VI

CIRCUIT DESCRIPTION

circuits	PI	PO	Gates	Critical Paths
b01	5	5	26	5
b02	5	4	14	4
b03	34	30	80	30
b04h	77	67	273	66
b04f	77	67	273	66
b06	6	9	38	9
b07	50	50	205	49
b08	30	22	78	21
b09	29	29	78	28
b10	28	18	96	17
b13	63	54	154	48
b18	3358	3342	57470	100
b19	1024	1605	77734	100
b20	126	75	4724	100
b21	522	512	5595	100
b22	186	110	6993	100

TABLE VII

RESULTS OF SA-BASED TEST PATTERN GENERATION FLOW FOR
SEVERAL ITC'99 CIRCUITS

circuits	SN=PSN+GB (V*s)	Delay (s)	Runtime (s)
b01	4.287E-11	1.984E-10	93
b02	4.902E-11	2.306E-10	137
b03	1.525E-09	8.386E-11	250
b04h	1.328E-09	6.978E-12	270
b04f	7.708E-10	7.786E-12	270
b06	1.069E-11	3.992E-10	262
b07	4.902E-11	2.306E-10	314
b08	4.902E-11	2.148E-10	362
b09	7.956E-10	5.440E-10	289
b10	4.337E-11	4.850E-09	393
b13	9.852E-11	5.540E-09	1048
b18	2.264E-09	7.360E-09	7230
b19	1.186E-09	7.188E-09	5460
b20	2.498E-09	8.126E-09	4258
b21	3.855E-09	8.380E-09	5630
b22	3.995E-09	9.90E-09	2456

TABLE VIII

COMPARISON RESULTS OF SA-BASED TEST PATTERN GENERATION
FLOW WITH 0 FILLING, 1 FILLING, AND RANDOM FILLING
METHODS FOR SEVERAL ITC'99 CIRCUITS

circuits	Measured Delay (s)				% difference with our method		
	F0	F1	FR	Our Method	F0	F1	FR
b01	1.64E-10	1.75E-10	1.74E-10	1.98E-10	17.4%	11.8%	12.4%
b02	1.78E-10	1.74E-10	1.83E-10	2.31E-10	22.8%	24.5%	20.5%
b03	8.26E-11	8.25E-11	8.20E-11	8.39E-11	1.4%	1.6%	2.2%
b04h	6.92E-12	6.90E-12	6.52E-12	6.98E-12	0.8%	1.1%	6.6%
b04f	7.46E-12	7.40E-12	7.26E-12	7.79E-12	4.1%	4.9%	6.7%
b06	3.20E-10	2.82E-10	2.90E-10	3.99E-10	19.7%	29.3%	27.3%
b07	1.90E-10	1.60E-10	1.58E-10	2.31E-10	17.4%	30.5%	31.4%
b08	2.90E-11	3.28E-11	1.11E-11	2.15E-10	86.5%	84.7%	94.8%
b09	2.68E-10	5.43E-10	3.64E-10	5.44E-10	50.8%	0.2%	33.1%
b10	4.82E-09	4.75E-09	4.42E-09	4.85E-09	0.7%	2.1%	8.9%
b13	4.50E-09	4.64E-09	5.00E-09	5.54E-09	18.7%	16.2%	9.7%
b18	6.88E-09	6.72E-09	7.25E-09	7.36E-09	6.5%	8.7%	1.5%
b19	6.58E-09	6.32E-09	7.05E-09	7.18E-09	8.5%	12.1%	1.9%
b20	7.42E-09	7.54E-09	8.10E-09	8.13E-09	8.7%	7.2%	0.3%
b21	7.02E-09	6.54E-09	7.47E-09	8.38E-09	16.2%	22%	10.9%
b22	5.75E-09	5.72E-09	6.70E-09	9.90E-09	41.9%	42.2%	32.3%
avg					20.1%	18.7%	18.8%

The number of primary inputs for the $b01$ benchmark is 5, which allows us to perform a thorough analysis of various input vectors. Input vectors are $<V_1 = XX011, V_2 = XX010>$ and there are 16 possible vectors that can be generated by specifying either a 0 or 1 on X values. To highlight the importance of considering both power supply noise and ground bounce for path delay testing, we evaluate the path delay and supply noise generated from each possible input vector $<V_1, V_2>$. Table IV shows our results. We have highlighted the minimum and maximum path delay and supply noise (power supply noise and ground bounce) for all vectors. There are two main observations from these experiments. First, we observe that the maximum supply noise on the circuit does

not lead to the maximum path delay. This is due to path delay speed-up/slow-down phenomena triggered from noise conditions on the cell and its neighboring cells. Second, there is a maximum up to 19% of the measured path delay difference between the input vector selected from our SA-based approach and the pattern with minimum delay $[< V_1, V_2 >= (11011, 01010)]$. These experimental results clearly indicate the need for a new delay testing technique that takes into account the impact that power supply noise and ground bounce can cause on path delay.

Fig. 14(a) and (b) show the voltage distribution on power and ground networks generated throughout the pattern generation flow. As shown in Fig. 14(a), there are many layers of voltage distribution due to different input patterns applied on the circuit. Our objective in this paper is to not select the pattern with minimum or maximum voltage drop or ground bounce, but rather to select a pattern that causes maximum delay in the presence of supply noise. Similarly, Fig. 14(b) shows the various voltage distributions on the ground network for different input patterns as listed in Table IV. Fig. 15 shows the voltage drop and ground bounce map for the the selected input pattern that causes maximum path delay.

B. Impact of Multiple Critical Paths

Here, we investigate critical paths for the benchmark $b01$ provided from the static timing analysis tool and compute their path delay variations in the presence of power supply noise and ground bounce. The results are listed in Table V. Paths are listed based on their criticality where path1 is the most

critical and path4 is the least critical. From the results shown in Table V, we observe that path delay of path2 is larger than the delay of path1 when both power supply noise and ground bounce are considered.

Such an observation indicates that critical paths selected by the timing analysis tools might not necessarily be the actual critical paths of the circuit, as the impacts of power supply noise, ground bounce, and resonance frequency are ignored. Therefore, for accurate results, the test pattern generation methodology should be combined with the critical path selection technique in order to take into account the impact of power supply noise and ground bounce.

C. Test Pattern Generation Flow

We apply our test pattern generation flow to the combination part of circuits on the ITC'99 benchmark. Table VI shows the list of circuits and their characteristics in terms of the number of inputs, outputs, and critical paths (reported by the static timing analysis tool). We apply our SA-based test pattern flow on the circuits and list their supply noise (power supply noise and ground bounce) and path delay. The results are listed in Table VII.

The number of the generated patterns greatly depends on the number of unspecified input values which also impact the runtime and the quality of the solution obtained by test pattern generation flow. The quality of the solutions depends on the number of X values, as a smaller number of X values on the input pattern imposes less flexibility to our pattern generation flow for finding a pattern that generates maximum path delay. Additionally, the runtime grows proportionally with the number of X values, as it increases the number of patterns and mathematical computations to be evaluated. Furthermore, the choice of the simulator (MATLAB) to perform the analysis of the linear system (power/ground network analysis) can also contribute to the long runtime.

We implement three other methods for comparison. The first method performs 0 filling on the unspecified input values and labeled as $F0$. The second method performs 1 filling on the unspecified input values and is labeled $F1$. The third method performs random filling on the unspecified input values and is labeled FR. Table VIII shows the results. We obtain that 0, 1, and random fillings underestimate the impact of supply noise on path delay. These experiments clearly indicate the need for a power supply noise and ground bounce aware test pattern generation tool. As future work, we aim to integrate signal integrity issues (i.e., crosstalk) and switching activity distribution (i.e., accurate hot spot and voltage droop distribution) and combine them with the path selection step for more accurate path delay computation in the presence of power supply noise and ground bounce.

VI. CONCLUSION

Current path delay testing techniques do not consider the combined impact of power supply noise and ground bounce on path delay. In this paper, we proposed close-form mathematical models for capturing the impact of supply noise on path delay variation for generating suitable input test patterns. We proposed an SA-based pattern generation technique which, for its fitness function, uses the mathematical models for deriving accurately the impact of supply noise on path delay. Experimental results showed considerable differences in path delays when both power supply noise and ground bounce effects were considered.

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