A Study of Tapered 3-D TSVs for Power and Thermal Integrity

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***Abstract*—3-D integration presents a path to higher performance, greater density, increased functionality and heterogeneous technology implementation. However, 3-D integration introduces many challenges for power and thermal integrity due to large switching currents, longer power delivery paths, and increased parasitics compared to 2-D integration. In this work, we provide an in-depth study of power and thermal issues while incorporating the physical design characteristics unique to 3-D integration. We provide a qualitative perspective of the power and thermal dissipation issues in 3-D and study the impact of Through Silicon Vias (TSVs) size for their mitigation. We investigate and discuss the design implications of power and thermal issues in the presence of decoupling capacitors, TSV/on-die/package parasitics, various resonance effects and power gating. Our study is based on a ten-tier system utilizing existing 3-D technology specifications. Based on detailed power distribution and heat dissipation models, we present a comprehensive analysis of TSV tapering for alleviating power and thermal integrity issues in 3-D ICs.**

***Index Terms*—3-D integration, power and thermal analysis, power delivery.**

I. Introduction

THE RECENT advancements in semiconductor processing technologies have enabled three dimensional circuit design and implementation of heterogeneous systems in the same platform, i.e., Flash, DRAM, SRAM placed atop logic devices and microprocessor cores [1]. 3-D vertical integration results in shorter interconnect lengths, greater device density and enhanced performance. However, the densely packed vertical tiers introduce significant power and thermal integrity challenges compared to 2-D integration.

Power delivery in 3-D systems draws much larger current from package and power/ground networks than in conventional 2-D systems due to multiple tiers [2]. The large current demand leads to significant *voltage droop* (accumulated IR drop, $L\ di/dt$ and $RC\ dv/dt$ effects) due to the parasitics of power and ground networks. Furthermore, the surge of current can lead to considerable di/dt effects due to on-chip and package inductances.

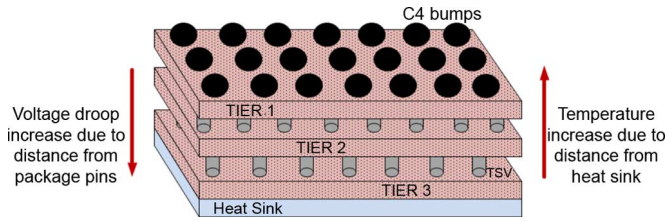

Fig. 1. Illustration of multi-tier system with through silicon vias. Voltage droop and temperature increase in opposite direction.

Due to the increased power density and greater thermal resistance to heat sink, thermal integrity is a crucial challenge for reliable 3-D integration. High temperatures can degrade the reliability and performance of interconnects and devices [3]. Power/ground network resistivity is a function of temperature, thus at nodes with high temperature, voltage droop values become even worse. Furthermore, the large amount of current on power and ground networks flowing for significant amount of time can ultimately elevate the temperature and cause Joule heating and electromigration [4]. Thus, voltage droop and temperature are interdependent and should be considered simultaneously during analysis. Fig. 1 shows an illustration of a 3-D system and depicts the opposing direction of voltage droop and temperature increase. Voltage droop tends to increase for tiers further away from package controlled-collapse chip-connection (C4) bumps and close to heat sink while temperature increases for tiers further away from heat sink and near to package pins.

While 3-D technology is still maturing, the following questions must be addressed for an accurate understanding of the criticality of power and thermal integrity issues in 3-D systems.

- How significant is the voltage droop impact of an actively switching tier on neighboring tiers? Do decoupling capacitors of neighboring tiers provide any mitigation?
- How critical are power supply noise and heat dissipation on a multi-tier system?
- What is the impact of power gating an entire tier?
- What is the impact of resonant frequency of a power delivery network (PDN) in 3-D systems?
- Does TSV sizing play a role?
- Are tapered TSVs more effective in mitigating power and thermal integrity problems, and if so, what are the design implications?

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To answer these questions, it requires accurate modeling and analysis to account for all the physical effects unique to 3-D integration. Our target platform is a ten-tier 3-D system consisting of tiers that dissipate identical power, unless a tier is power gated or subject to dynamic frequency scaling. Further, we assume that the number of power/ground TSVs connecting any two adjacent tiers is the same. TSVs may only vary in their cross-sectional area. We investigate optimal tapering of TSVs under the above constraints. We also assume a 3-D power delivery network, where each tier has its own delivery network connected through power/ground TSVs.

This study presents a comprehensive power and thermal co-analysis for 3-D integrated systems. RLC models are used for TSVs and power/ground networks. Models are flexible to represent TSVs of different dimensions and extracted for high frequencies in order to capture the skin effect and substrate coupling of TSVs as in [5]–[8]. Power and thermal analysis is based on the well-known electrical-thermal duality principle. Tapering of power/ground TSVs is investigated as means to ease power and thermal integrity issues in 3-D integration.

There are a few works in the literature that aim at performing both power and thermal analysis for 3-D systems. An electrical-thermal co-analysis method was proposed in [9], however, important physical level details were not considered, i.e., heat transfer among tiers and TSVs skin effect. In [10] and [11], a via stapling method for 3-D systems was proposed based on power and thermal integrity. In contrast to previous works, we aim to provide a comprehensive power-thermal co-analysis to fully understand the criticality of power and thermal issues in 3-D systems. Furthermore, we investigate the impact of tapered TSVs on power and thermal integrity.

The rest of this paper is organized as follows. Models for TSVs, C4 and power/ground networks are presented in Section II. Our power-thermal co-analysis methodology is presented in Section III. In Section IV, we present several case studies for investigating 3-D power and thermal issues. Section V discusses the impact of tapered TSVs. Section VI presents design implications of using tapered TSVs. We conclude this paper in Section VII.

II. Models

We make use of 3-D technology specifications that are available from open literature to study power and thermal integrity issues. Table I summarizes the technology data that are referenced throughout this section and some are obtained from [12]. This section provides detailed descriptions of the models used in our analysis.

To quantify the impact of TSVs on multi-tier systems, we utilize detailed analytical models including $\{R, L, C\}$ parasitics from the package, on-chip power/ground global distribution networks, TSVs, and underlying switching circuits. Current is delivered from the package pins through C4 arrays, and then distributed over the power network and TSVs through each tier where switching circuits draw the current. Fig. 1 provides an illustration of the multi-tier systems considered in this work. It is important to note that models discussed in this work are not specific to any 3-D prototype.

TABLE I
Technology Specifications

Technology Specifications	
TSV pitch (Cu filled)	1:10
TSV dimensions	1-10μm diameter 10-100μm height
TSV density ("via last")	10^4/mm^2
C4 dimensions	100-200μm
C4 current per bump	200mA
Cell area	300-300μm
Circuit Specifications	
Circuit technology node	90nm
Switching frequency	100MHz-10GHz
Current density	0.025A/μm^2
Thermal Specifications	
Thermal model	1-D Model
Temperature at substrate	27°C

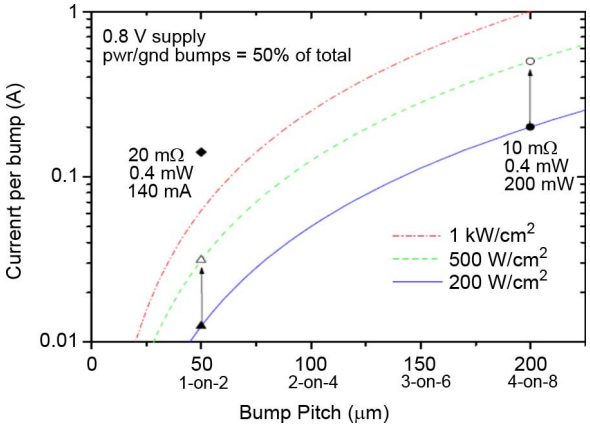

Fig. 2. Current provided by C4 bump with respect to its pitch [14].

A. C4 Model

C4 bumps are a technology standard for allowing high wiring density and high signal bandwidth between the chip and package. Packaging industry is recently moving toward bump arrays for high-density connections with bumps smaller than the standard 100 μm diameter on 200 μm pitch [13]. Compared to wire-bonding, flip-chip packaging with C4 bumps provide a significant improvement in power and ground network distribution.

Detailed characterization of C4 bumps is performed by [14] and Fig. 2 shows a plot of the C4 current with respect to C4 pitch for various power densities. In our analysis, we employ standard size C4 with 100 μm diameter on 200 μm pitch with power density of 200 W/cm2. The current provided from each C4 is 200 mA. The parasitics of C4 bump are 10 mΩ and 60 pH. In this work, we consider an array of C4s bumps and half of them supply power and ground, respectively.

For our analysis, we consider a portion of the power and ground network distribution which includes an array of C4s with several power and ground C4 bumps. Chip footprint can be divided into cells which are identical square regions between pair

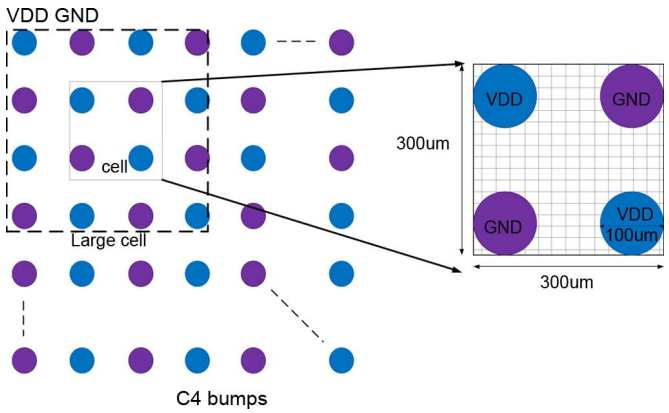

Fig. 3. Illustration of the power network area and 16 C4 power and ground bumps that are considered in this analysis. Cell dimensions are 300 μm by 300 μm. Large cell dimensions are 700 μm by 700 μm.

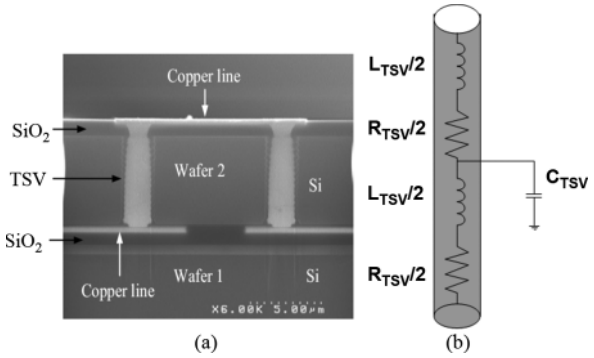

Fig. 4. (a) Photograph of CU TSV [17]. (b) Electrical model of a TSV.

of adjacent power and ground pads as shown in Fig. 3. In literature, a small area of power grid such as the cell shown in Fig. 3 which is among two power and ground C4s is often used for power analysis where due to symmetry it is assumed that no current passes in the normal direction to the cell border[15]. In this work, we utilize a larger power network area 700 μm $\times$ 700 μm and include several power/ground C4s. This allows us to investigate the impact of several power/ground pins for current supply and represent more realistically the boundary conditions between cells.

B. TSV Model

TSVs enable vertical integration and have a significant impact on the power and thermal integrity of the system, as they introduce additional parasitics between each tier. TSVs [16], [18] form a cylindrical metal-oxide-semiconductor (MOS) capacitor with semiconductor substrate acting as the bulk and TSV metal acting as a gate. TSVs allow voltage/signal distribution among the tiers; however, they also behave as a medium for power supply noise propagation from one tier to the next. Similarly, TSVs allow heat dissipation in vertical direction which is highly dependent on the TSV geometry and circuit switching activity on its surrounding. In this work, we consider copper filled TSV as shown in Fig. 4(a).

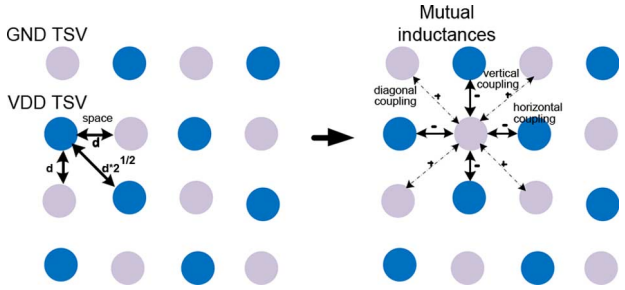

Fig. 5. TSV distribution.

To determine the impact of TSVs on power and thermal integrity for multi-tier systems, we apply analytical models to express the resistance, inductance and capacitance parasitics of the TSV with respect to its physical dimensions. The values of the parasitic $\mathrm{R_{TSV}}$, $\mathrm{L_{TSV}}$, and $\mathrm{C_{TSV}}$ are derived as a function of physical parameters, material characteristics and technology parameters [8]. Fig. 4(b) shows the electrical model of a TSV.

The resistance of the TSV with respect to its radius, r_{TSV} and length l_{TSV} is as

$$R_{\mathrm{TSV}_{DC}} = \frac{\rho l_{\mathrm{TSV}}}{\pi r_{\mathrm{TSV}}^2} \tag{1}$$

where ρ is the resistivity of the conducting material. Authors in [17] performed TSV characterization with varying frequencies from 0 to 20 GHz. TSV resistance increases with frequency from 120 to 270 mΩ due to skin effects [17]. In our analysis, we perform a study with various switching frequencies to account for skin effect and represent various workloads.

TSV inductance is also derived through partial self-inductance and mutual inductance. Partial self-inductance depends on the diameter and length of TSV and is expressed as

$$L_{\mathrm{self}} = \frac{\mu_0 l_{\mathrm{TSV}}}{2\pi} \cdot \left[\ln\left(\frac{2l_{\mathrm{TSV}}}{r_{\mathrm{TSV}}} \right) - \frac{3}{4} \right] \tag{2}$$

where μ_0 is the permeability of free space given by $4\pi \cdot 10^{-7}$ H/m. Additionally, mutual inductance between TSVs has an impact on the overall inductance parasitic of a TSV. Fig. 5 shows the TSV distribution assumed in this work. Depending on the location and spacing between the neighboring TSVs, mutual inductance can have an additive effect when the current flow is in the same direction and a diminutive effect when current flows on opposite direction, i.e., between a power and ground TSV. Mutual inductance between two TSVs can be derived as

$$L_M = \frac{\mu_0 l_{\mathrm{TSV}}}{2\pi} \cdot \left[\begin{array}{c} \ln\left(\frac{l_{\mathrm{TSV}}}{s_{\mathrm{TSV}}} + \sqrt{1 + \left(\frac{l_{\mathrm{TSV}}}{s_{\mathrm{TSV}}} \right)^2} \right) \\ -\sqrt{1 + \left(\frac{s_{\mathrm{TSV}}}{l_{\mathrm{TSV}}} \right)^2} + \frac{s_{\mathrm{TSV}}}{l_{\mathrm{TSV}}} \end{array} \right] \tag{3}$$

where s_{TSV} is the spacing between two TSVs. Spacing between two TSVs varies depending on their location. For example, in our study, mutual coupling between two neighbor TSVs in either vertical or horizontal direction have a space $d = 60$ μm, while

two TSVs mutually coupled in diagonal direction have a space of $d\sqrt{2} \approx 85$ μm as shown in Fig. 5. Thus, the inductance for any TSV is computed taking into account the partial self-inductance and mutual inductances as

$$\begin{aligned} L_i^{\mathrm{VDD}} &= L_{\mathrm{self}_i}^{\mathrm{VDD}} + \sum_{j \in \mathrm{neighbors}} \alpha_j L_{M_j}^{\mathrm{VDD}} \\ &\quad - \sum_{k \in \mathrm{neighbors}} \alpha_k L_{M_k}^{\mathrm{GND}} \\ L_i^{\mathrm{GND}} &= L_{\mathrm{self}_i}^{\mathrm{GND}} + \sum_{j \in \mathrm{neighbors}} \alpha_j L_{M_j}^{\mathrm{GND}} \\ &\quad - \sum_{k \in \mathrm{neighbors}} \alpha_k L_{M_k}^{\mathrm{VDD}} \end{aligned} \tag{4}$$

where L_i^{VDD} is the inductance for a power TSV and L_i^{GND} is the inductance for ground TSV. Coefficient α_i is the ratio of currents flowing through the TSV under investigation and its neighboring TSV as the current flow on each TSV can differ based on the switching activity of the underlying circuits. Furthermore, the number of neighboring TSVs varies based on the location of the TSV under investigation. For example, a TSV located on the boundary of the TSV array has fewer neighboring TSVs than a TSV located in the center of the TSV array; hence their mutual inductance would vary. Additionally, mutual inductance varies with respect to the distance between TSVs, as the space between two TSV increases, their coupling decreases as well. Fig. 5 illustrates TSV array and inductance coupling between neighboring TSVs and their effect (i.e., additive or subtractive) based on the direction of the current flow.

TSV capacitance can be derived by solving Poisson's equations for MOS capacitor structure in cylindrical coordinate system due to TSV shape [18]. It is sufficient to solve 1-D Poisson's equation along radial direction to obtain the capacitance [8]. Equation (5) describes TSV capacitance as a function of oxide and depletion capacitance as

$$\begin{aligned} C_{\mathrm{TSV}} &= \frac{C_{\mathrm{ox}} C_{\mathrm{dep_{min}}}}{c_{\mathrm{ox}} + c_{\mathrm{dep_{min}}}} \text{ where } C_{\mathrm{ox}} = \frac{2\pi\varepsilon_{\mathrm{ox}} l_{\mathrm{TSV}}}{\ln\left(\frac{R_{\mathrm{ox}}}{R_{\mathrm{metal}}}\right)} \\ C_{\mathrm{dep_{min}}} &= \frac{2\pi\varepsilon_{si} l_{\mathrm{TSV}}}{\ln\left(\frac{R_{\mathrm{max}}}{R_{\mathrm{ox}}}\right)} \end{aligned} \tag{5}$$

where $\varepsilon_{\mathrm{ox}}, \varepsilon_{si}$ are permittivity of oxide and silicon, respectively. As shown in (5), C_{TSV} is directly proportional to the length of TSV and inversely proportional to the dielectric thickness of TSV. With increasing frequency up to 20 GHz, for 2 μm diameter TSV, its capacitance drops off from 30 to 5 fF [17]. In this work, we utilize parasitic values obtained up to 10 GHz frequency and their values are listed in Table II for different TSV geometries.

C. Power and Ground Distribution Network

In 2-D high-performance designs, power distribution networks are commonly structured as a multi layered mesh grid [19]. In such a grid, power tracks of each metal layer span the entire die and vias are inserted on intersections between them. Power is distributed over many metal tracks creating local and global power grids. In 3-D multi-tier systems, power and ground networks for each tier can be represented as a 2-D mesh grid. Additionally, in 3-D systems, power distribution networks deliver power and ground voltages from pads to all tiers passing through the TSVs. TSV can be inserted BEOL ("via last") or FEOL ("via first") [20]. In this analysis a "via last" approach is assumed which indicates that a TSV is connected to the global power grid of one tier and to the local power grid of the next tier. Fig. 6 illustrates this concept. The physical and analytical models described in this work can be applied to TSVs of any size and approach, i.e., representing "via first" approach would differ the power network size and granularity (local or global network) that is connected through the TSV from one tier to another. In the following subsections, both electrical and thermal models of power/ground distribution networks are described.

TABLE II
PARASITIC VALUES OF A TSV

TSV Diameter (μm)	TSV Oxide Thickness (nm)	TSV Length (μm)	$R_{\mathrm{TSV\_DC}}$ (mΩ)	L_{TSV} (pH)	C_{TSV} (fF)
2	50	20	118.49	13.827	52.229
2	100	20	132.02	14.039	21.429
5	50	50	44.539	34.262	69.982
5	100	50	46.414	34.521	35.889

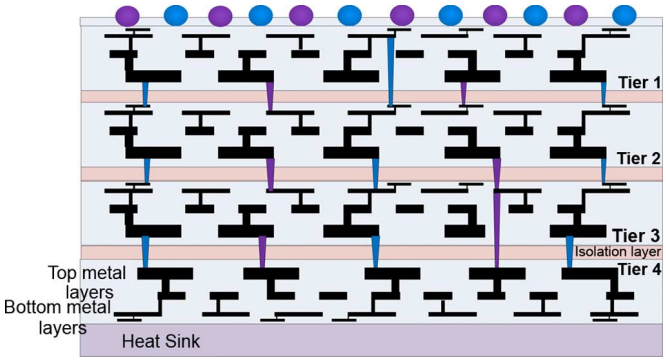

Fig. 6. Four tier 3-D system with TSVs and C4 bumps on top.

D. Electrical Model

Our analysis considers dynamics power analysis by including RLC parasitics of the 3-D multi-tier system. The extracted parasitics represent the package (C4 bumps), power/ground networks, switching circuits, decoupling capacitance (intentionally inserted capacitance and/or equivalent capacitance from non-switching circuits), and TSVs. We assume a uniform distribution of power/ground TSVs among all tiers. Power and ground grids for each tier vary in granularity and track dimensions depending on TSV connection which represent either a local or global grid for the given grid area. Power analysis is applied on the large cell area as described in the previous Section II-A. Package parasitics are modeled by resistance, R_{pkg} and inductance, L_{pkg}. Power and ground networks are modeled by resistance, R_{grid} and capacitance, L_{grid}. Switching circuits on each tier are modeled as time-varying current sources to represent the electrical characteristics of the underlying hardware in terms of: 1) switching frequency; 2) peak current; 3) leakage

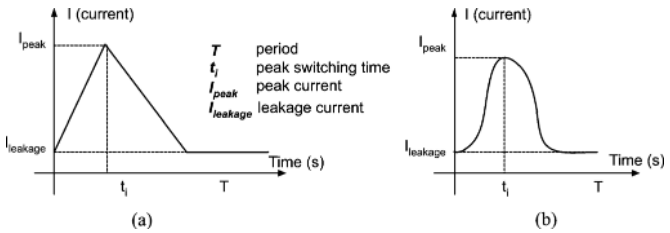

Fig. 7. (a) Triangular and (b) Weibull function-based current model.

current; and 4) rise and fall times. Switching circuits are typically represented by triangular waveforms [21]; as those shown in Fig. 7(a). A triangular or trapezoidal current waveform is used to represent circuit's average current consumption, peak current, cycle time, rise and fall times. For simplicity, we refer to switching circuits using parameters of the triangular waveform, but in our computations, we utilize a continuous Weibull function with a period T, peak switching time tp, peak current Ip, and leakage current, Il in idle mode. Fig. 7(b) illustrates the continuous current waveform model that we use in our analysis. The Weibull current model is continuous which facilitates our mathematical computations, rather than the discrete triangular waveform.

Switching current sources using Weibull function are expressed as

$$I_{\text{load}}(t) = \frac{k}{\lambda}\left(\frac{t}{\lambda}\right) \cdot e^{-(t/\lambda)k} + I_{\text{leakage}} \tag{6}$$

where k is the shape parameter that corresponds to I_{peak}, and λ is the scaling parameter that corresponds to t_i. Furthermore, in our analysis, we convert the time-varying function to frequency domain.

The analysis are performed on a 3-D multi-tier structure using workload characteristics of high performance cores at the 90-nm node with frequencies up to 10 GHz and models are obtained from predictive technology model which provides technology parameter files for transistors and interconnects [22]. The key premise of this analysis is to perform simultaneous power and thermal analysis. To do so, temperature dependent resistivity is used and expressed as

$$\rho = \rho_0 \left[1 + \beta(T_{\text{empature}} - T_0)\right] \tag{7}$$

where ρ_0 is the electrical resistivity at T_0 which is 27 °C and β is the temperature coefficient of electrical resistance [23]. As temperature increases, the electrical resistivity of the conductors goes up and eventually impacts power supply noise. Furthermore, voltage droop due to the flowing currents on the power/ground tracks causes Joule Heating and if these currents flow for a considerable amount of time, they can lead to electromigration (EM) issues by creating voids and/or hillocks [24]. Thus, power and thermal issues are coupled together and we simultaneously investigate the impact of voltage droop on thermal distribution and vice versa.

To accurately solve the 3-D multi-tier system for power analysis, we employ Kirchhoff's law to formulate set of linear equations for describing the current flow at each node on the system. These equations can be devised together in matrix arrangement

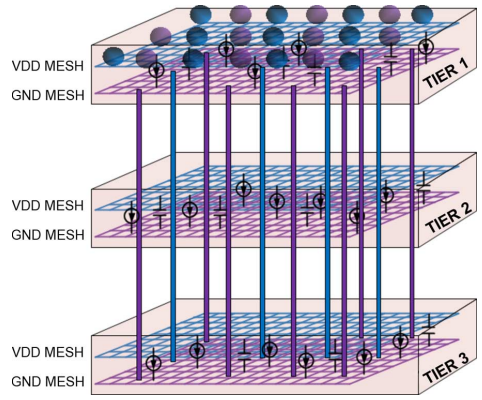

Fig. 8. Four tier 3-D system with TSVs and C4 bumps on top.

and solved accurately using any linear solver package. The matrix formulation of the system is based on modified nodal analysis (MNA) method which is commonly used in literature for power grid analysis [25]. These matrices serve as analytical models to represent the physical design parameters and are expressed as

$$[G + sC]x(s) = I(s) \tag{8}$$

where G is the *m-by-m* conductance matrix, C is the *m-by-m* capacitance and inductance matrix, and I is the *m-by-1* vector of switching current and voltage sources. $x(s)$ is the *m-by-1* vector that represents node voltages and inductive branch currents. To obtain voltage droop and current distributions, we solve the system in (8) and obtain node voltages on the power/ground networks along with the branch currents on the power/ground network and TSVs. Note that matrix computations are performed on the large cell area as referred to Section II-A (several hundred nodes) which facilitate the mathematical computations and derivation of inverse matrix. For large system analysis, there exist mathematical methods to ease matrix computations; however, it is not the aim of this work to elaborate on them.

In Fig. 8, power and ground mesh networks of a four tier 3-D multi-tier structure is illustrated along with switching current sources, decoupling capacitance, and C4 bumps. Such models are utilized on our power analysis.

E. Thermal Model

Our investigations are based on the 1-D treatment of the thermal problem for 3-D integration. Temperature rise due to multiple tiers switching has a significant impact on the heat dissipation and temperature gradient on a tier and among tiers. TSVs behave as a medium for heat transfer from one tier to the next, which can be beneficial for dissipating heat away from a hot tier but can also be detrimental to neighboring switching tiers. In this work, we develop thermal models by exploiting the principle of electrical-thermal duality [25]. The duality states that the heat flow passing through a thermal resistor is equivalent to the current passing through the electrical resistance where temperature difference is equivalent to voltage difference.

Heat is removed through heat sink (bottom surface) while heat is generated from upper tiers and has to be transferred

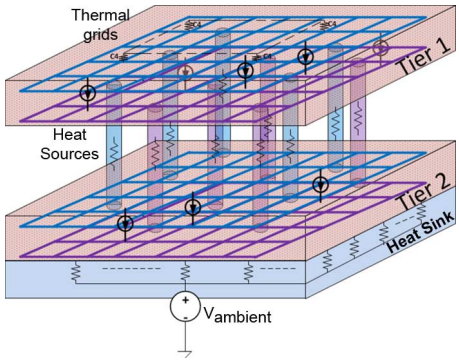

Fig. 9. Thermal modeling of a two tier 3-D system.

through TSVs and several material layers to reach the silicon substrate. SiO_2 and isolation layers between tiers act as thermal barriers since their thermal conductivities are different (a few order of magnitude lower) to that of silicon. Switching circuits contribute to the heat generation and are modeled by current sources. C4s, power/ground networks, TSVs and heat sink are modeled as thermal resistances to indicate the lateral and vertical heat flows through the tiers. Due to dissimilar lateral and vertical thermal resistances heat dissipates at different rates. Lateral resistances are represented as the thermal resistance of the power and ground networks while vertical resistances are based on TSVs thermal resistance. The temperature of heat sink is assumed uniformly distributed with value of 300 K (27 °C) and modeled by constant voltage sources. Fig. 9 provides an illustration of 3-D thermal models for a two tier system.

Similar to electrical analysis, Kirchhoff's law can be applied to present the heat flow as a function of thermal resistance and temperature on 3-D multi-tier system as

$$G_{th}T_{\text{emp}} = Q \tag{9}$$

where G_{th} is the thermal resistivity matrix of size *m-by-m* and m is the number of power/ground nodes on the 3-D system. T_{emp} is the *m-by-1* vector of temperature nodes and Q is the *m-by-1* vector for heat sources.

III. Power and Thermal Analysis

We developed a simultaneous power and thermal analysis flow to account for temperature effects on electrical performance of a 3-D system. The proposed methodology is an iterative process and Fig. 10 shows the proposed power and thermal analysis flow.

Power analysis is based on transient analysis that derives voltage droop distribution for each tier where excessive droop results in elevated temperatures on metal tracks. The increase in temperature is applied to update thermal models for thermal analysis step. Thermal analysis is based on 1-D static analysis and provides temperature distribution for each tier and TSVs, where elevated temperatures alter conductors' resistivity and are included in power analysis step. The changes in resistivity and temperature result in an iterative process, which converges when there are no more changes on voltage droop and temperature distribution. Please note, that the thermal analysis is based on a steady state thermal analysis to capture temperature distribution on each tier for a given power profile. It is limited to capture the dynamic thermal distribution to varying power profiles. However, as we aim to capture fast and accurately the temperature distribution on each tier for a given power profile, 1-D thermal analysis is a viable approach.

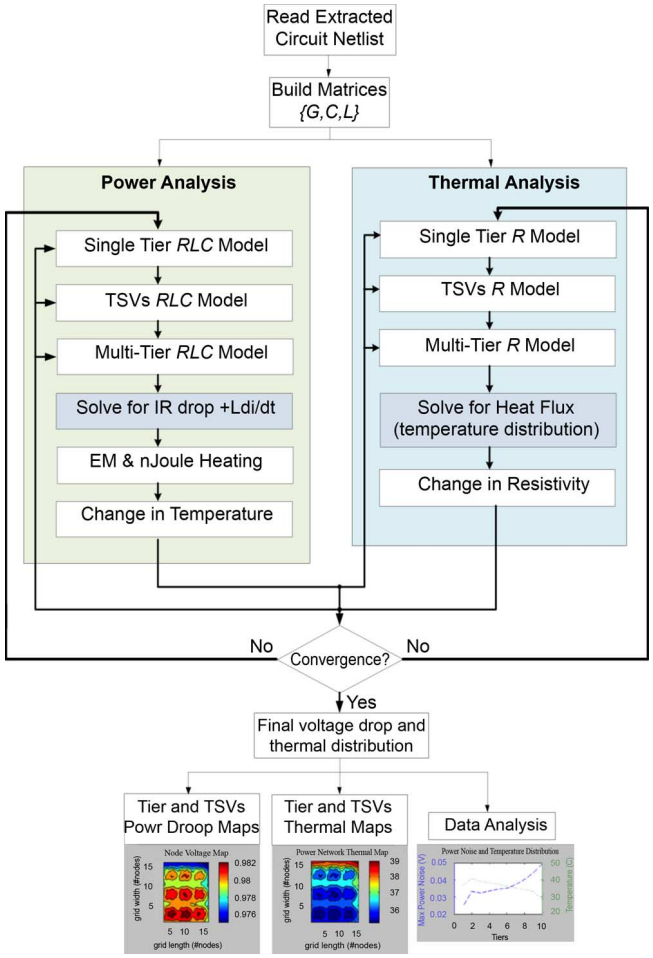

Fig. 10. Proposed methodology for performing simultaneous power and thermal analysis of 3-D integrated systems.

We employ mathematical models as described in the previous section and advanced numerical analysis methods to perform efficient power/ground and thermal networks analysis. Power analysis is performed by utilizing (6)–(8) and thermal analysis is performed by using (9).

IV. Case Studies

In the following subsections, we utilize the proposed analysis flow as shown in Fig. 10 to investigate several physical design issues pertaining to 3-D integration. Our investigations are targeting power and thermal integrity of 3-D systems for various operational scenarios of switching tiers. Tapered TSVs are also studied for their impact on power thermal integrity of 3-D systems.

A. Impact of One Tier Activity

To understand the implications of power and thermal integrity for a 3-D system, we start by investigating a single active tier

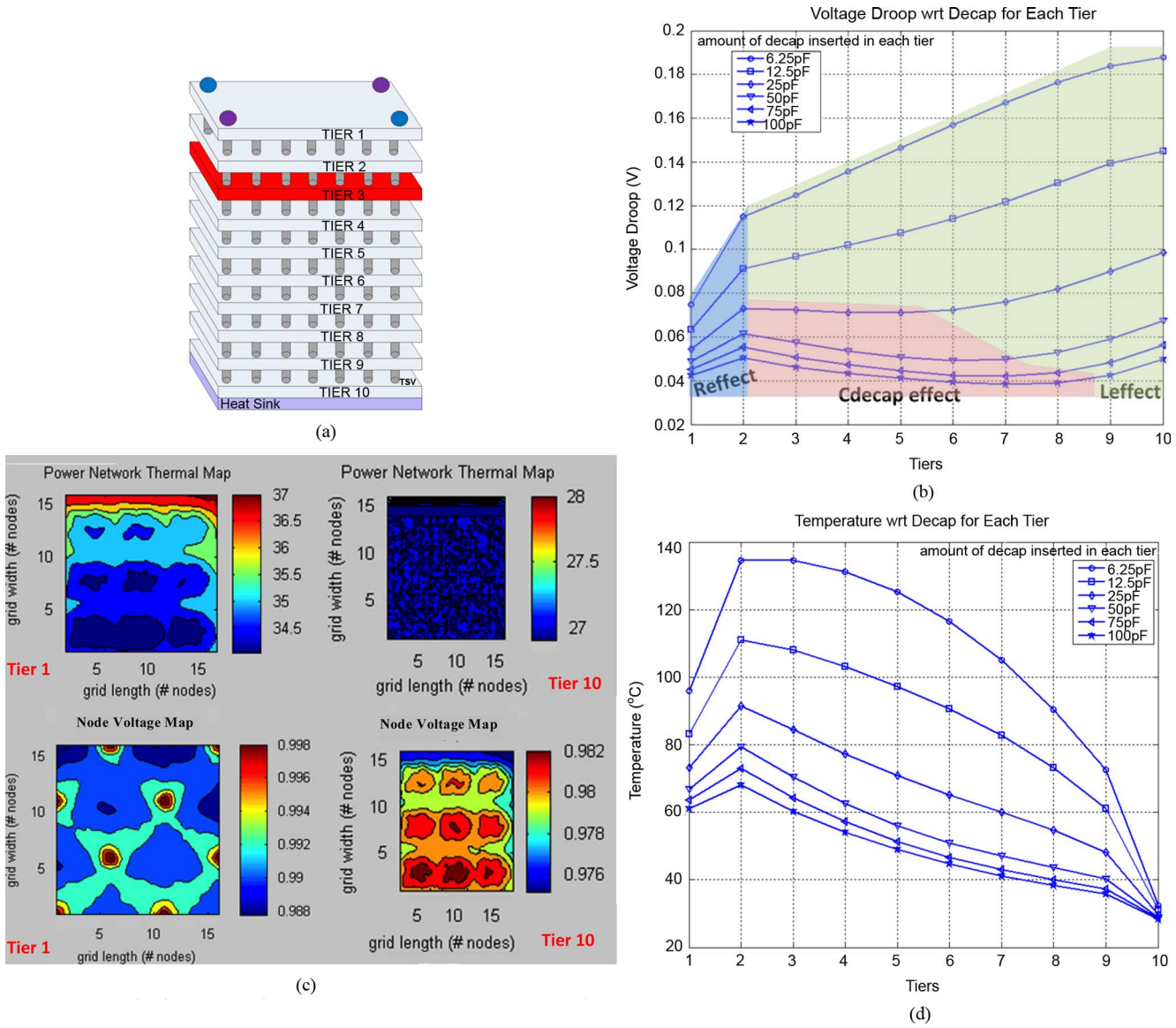

Fig. 11. (a) Case study for one switching tier on ten tiers. (b) Voltage droop. (c) Thermal and node voltage distribution maps for top and bottom tiers (1 and 10). (d) Temperature distribution for each tier.

on a multi-tier system. The number of total tiers is set to ten and connected by TSVs as shown in Fig. 11(a) for a single cell area while analysis is applied on a larger area as described in Section II-A. The workload is applied to a tier, which is varied for each configuration from tier one to ten. For each configuration, we compute voltage droop and thermal distribution on the switching tier as the workload is applied to each tier. For example, in first configuration, the workload is applied at TIER 1, second configuration at TIER 2, and so on, till workload is applied at TIER 10. The package pins are located next to TIER 1 and heat sink is located next to TIER 10. The package, power/ground network, TSVs, switching circuits, and decoupling capacitor models described in the Section III are applied. In this study, frequencies up to 10 GHz range are considered. Additionally, we vary the amount of decoupling capacitance available on each tier. R and L parasitics are not varied as they are represent the parasitics of package, tiers and TSVs while the amount of intentionally inserted decoupling capacitance can be varied to investigate the overall impact of R, L, and C parasitics on the voltage droop and temperature trend. We report total analysis runtime of 359 s with 4 iterative convergence steps between electrical and thermal analysis.

In Fig. 11(b), it is shown the computed voltage droop and temperature of the active tier for all configurations. As the workload is applied to a tier further away from the package pins, there is an increase on voltage droop, i.e., up to 180 mV when active tier is TIER 10. Additionally, we observe that the trend on the increase of voltage droop is not linear but rather three different regions can be identified as color shaded areas in Fig. 11(b). In the first region, we notice a sharp increase in voltage droop as the switching tier is moving from TIER 1 to TIER 2 because of the accumulated resistance parasitics of tier one, two and TSVs. This region is referred to as "*Reffect*" due to the dominant effect observed from the accumulated resistance. Also, note that the non-switching tiers are acting as decoupling capacitors, which provide some mitigation to the switching cir-

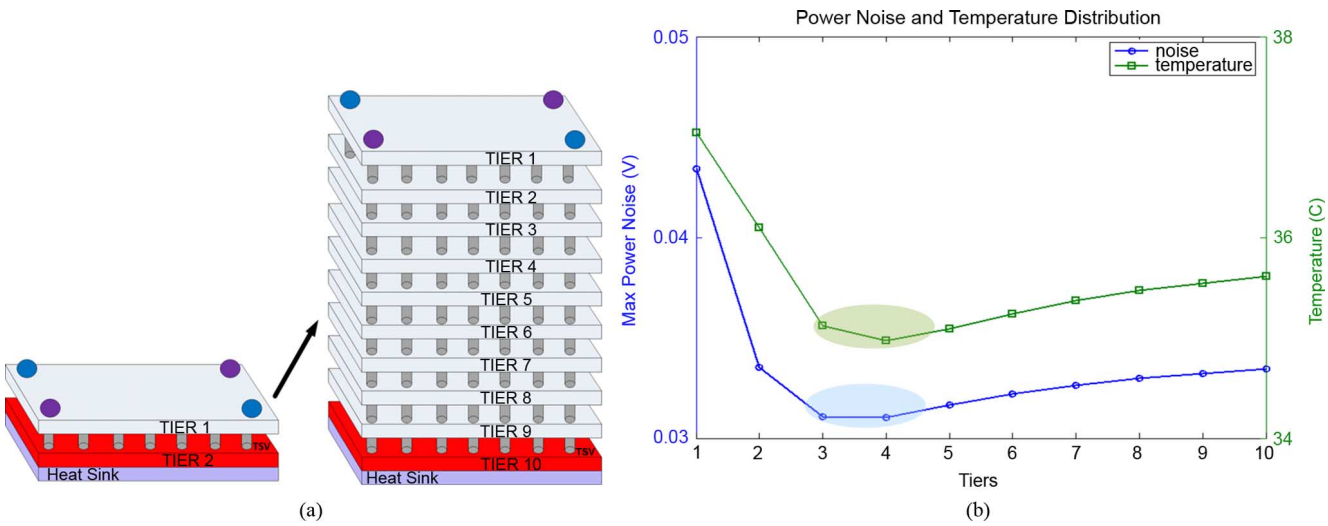

Fig. 12. (a) Case study for one active tier to capture the decoupling capacitor effectiveness and (b) voltage droop and temperature distribution for each tier.

cuits through charge sharing. The amount of available decoupling capacitance depends on neighboring tiers, i.e., TIER 1 has less decoupling capacitance available due to having only one immediate neighbor tier (TIER 2), whereas, TIER 4 has more available decoupling capacitance due to having two neighboring tiers (TIER 3 and 5). Thus, the available amount of decoupling capacitance that each tier experiences will vary based on their tier location.

We also observe that voltage droop is sensitive to the amount of inserted decoupling capacitance as shown in Fig. 11(b). In the second region, we observe an almost a flat curve where the increase in voltage droop remains nearly steady. This region is referred to as "*Ceffect*" due to the dominant impact of decoupling capacitance. We observe an increase in decoupling capacitance for mid range tiers because of the increase in number of neighboring tiers. The amount of decoupling capacitance available increases and mitigates the amount of power supply noise generated. Furthermore, we observe that this region vanishes for some curves with small amount of inserted decoupling capacitance.

In the third region, we observe a sharp increase in voltage droop when the workload is applied on the bottom-most tiers. This region is referred to as "*Leffect*" due the dominant effect observed from the inductance and resistive parasitics. As the workload is applied to a tier located further away from the package pins, power delivery traces experience an increase in the resistive and inductive parasitics accumulated through the many tiers and TSVs. The parasitics resistance and inductance of package, tiers and TSVs contribute to the increase of voltage droop. Furthermore, the amount of voltage droop is proportional to the switching frequency. Inductive effects become more prominent with increasing frequency due to jwL. In the next subsections, we perform frequency dependent analysis.

On the contrary to the voltage droop distribution, we observe that temperature has an inverse distribution among the tiers. The bottom-most tiers are located near to the heat sink and experience lower temperatures. We observe that temperature increases as the workload is applied to a tier located further away from the heat sink. We also notice a temperature drop when the workload is applied to TIER 1 in comparison when it is applied to TIER 2. This is due to the effect of power supply noise. TIER 1 experiences less power supply noise than TIER 2, thus, the heat generated is also less; consequently, there is a decrease in temperature levels.

B. *Decoupling Capacitor Efficiency*

To understand the impact and effectiveness of decoupling capacitance in a multi-tier 3-D system, we perform experiments with a single workload while increasing the total number of tiers. Our aim is to capture the optimal number of tiers required in order to achieve minimum voltage droop and minor temperature increase while benefiting from the increase of decoupling capacitance due to having multiple tiers. Fig. 12(a) shows the setup of this experiment for a single cell area as described in Section II-A. Voltage droop and temperature are monitored on the switching tier (bottom-most tier) as the number of tiers is increasing. We report total analysis runtime of 190 s with 4 iterative convergence steps between electrical and thermal analysis.

Fig. 12(b) shows the curves for the measured voltage droop and temperature. As the workload is applied to a tier located further away from the package pins, we observe an increase on the parasitics resistance due to longer traces from package to switching tier. We notice a decrease in voltage droop when the switching tier is located either in TIER 3 or 4. For these cases, the increase of resistance parasitics (further away from package) is compensated by an increase of available decoupling capacitance from the idle neighboring tiers.

The measured reduction in voltage droop is about 15 mV between TIER 1 and 3. When active tier is TIER 1, voltage droop is roughly 45 mV and reduced to 30 mV when active tier is TIER 3. As the active tier moves down, the available decoupling capacitance is not sufficient to compensate for the long traces with resistive and inductive parasitics. A similar trend is observed for temperature variations. Further, temperature variations are contributed based on the generated supply noise. Even though, the same workload with the same attributes (current drive and switching frequency) is applied for all scenarios, the amount of

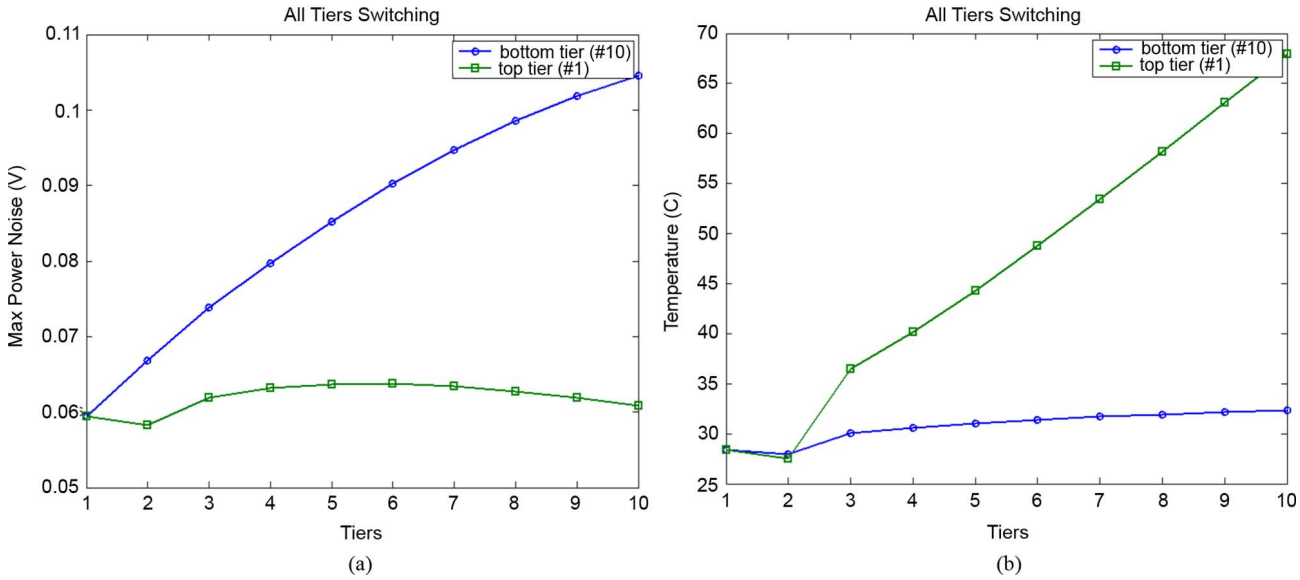

Fig. 13. (a) Voltage droop and (b) temperature distribution on the top and bottom tiers for each configuration (increasing number of total tiers).

supply noise and generated heat varies for each tier due to the effectiveness of decoupling capacitance. TIER 4 experiences the least voltage droop; hence minimal amount of heat is generated in this tier. Temperature difference is around 2 °C between TIER 1 (furthest from heat sink) and TIER 4 (with minimum voltage droop). As the switching tier moves away from package, voltage droop and temperature increase.

C. Impact of Multi-Tier Activity

In this study, we investigate power and thermal integrity of a 3-D system when multiple workloads are applied. The applied total number of workloads varies from one to ten in each configuration. Voltage droop and temperature distribution are measured on the topmost and bottom-most tiers in order to capture their trend as shown in Figs. 13(a) and 13(b). We report total analysis runtime of 352.4 s with 4 iterative convergence steps between electrical and thermal analysis.

We observe an increase in voltage droop and temperature when multiple tiers are active in comparison to a single active tier. In the case when only a single tier is switching, the amount of power supply noise and heat generated is smaller than when several tiers are switching, because the non-switching layers can contribute as decoupling capacitors for noise suppression.

Furthermore, as the number of workloads increases, there is a progressive rise of voltage droop and temperature up to a point that these levels may be intolerable for reliable circuit operation. For the bottom-most tier, voltage droop can reach up to 110 mV while for the topmost tier, temperature can rise up to 70 °C. These trends urge for techniques to suppress noise and manage temperature levels on a 3-D system.

D. Impact of Power Gating at Tier Level

In this experiment, we investigate voltage droop and temperature distribution on each tier with power gating. For this study, power gating is applied at a tier level where a tier can be shut-off by using distributed PMOS sleep transistors between the global and virtual power networks. For simplicity, sleep transistors are modeled by their resistive parasitics. The study is applied on a multi-tier system composed of ten tiers. We apply three different power gating configurations: 1) no power gating is applied and all tiers are switching; 2) power gating is applied to TIER 2, 4, 6, 8 and referred to as power gating *configuration 1*; and 3) power gating is applied to middle tiers, TIER 5, 6, 7 and referred to as power gating *configuration 2*. We report total analysis runtime of 13.6 s with 4 iterative convergence steps between electrical and thermal analysis.

In Fig. 14(a), the comparison of TSV current densities for each power gating configuration are shown. We observe that TSVs on the top tiers (i.e., TIER 1 and 2) experience the highest current density due to the large current that flows through them. Furthermore, some power-gating configurations can induce some TSVs, i.e., TIER 7 and 8, to experience higher current densities than when no power gating is applied. Such increase in current densities that can last for multiple clock cycles can induce atom migration on the TSVs, which ultimately may reduce their reliability.

Fig. 14(b) shows temperature distribution comparisons for different power gating configurations. We observe that TSVs, which are further away from heat sink, experience the highest temperatures. A similar trend is observed when power gating is applied; however, the temperature levels are lower due to overall reduction in supply noise (overall less current is drawn with power gating).

We compute the mean time to failure (MTTF) metric [measurement unit hour (h)] by utilizing TSVs current density and temperature distributions for different power gating configurations. MTTF is described by Black equations [26] as

$$\mathrm{MTTF} = \frac{C}{J^a} e^{E_a/k-T} \tag{10}$$

where C and a are empirical constants, J is the current density, E_a is the activation energy for electromigration mechanism, k is the Boltzmann constant and T is temperature. Comparisons with respect to the MTTF metric are shown in Fig. 14(c). We

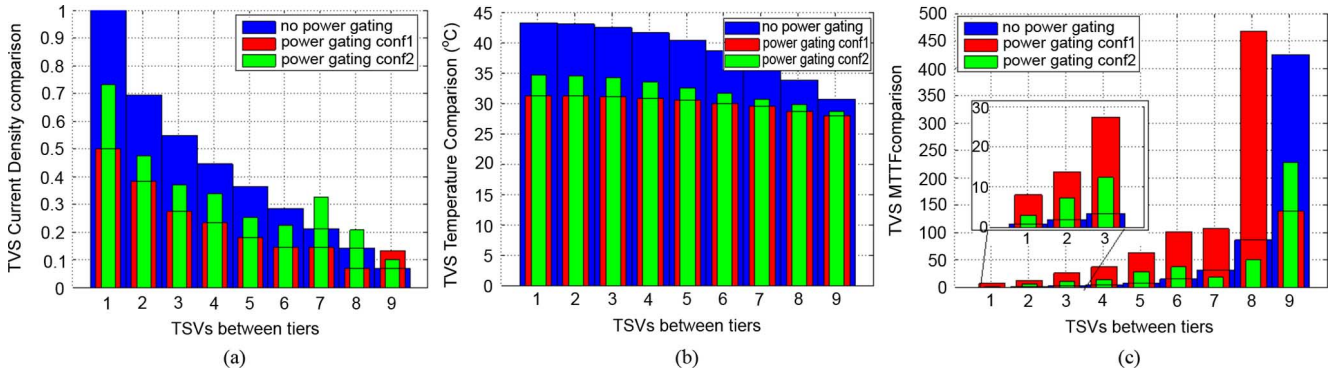

Fig. 14. (a) Current densities comparison with respect to maximum allowed current density for different power gating configurations. (b) Maximum temperature comparison of different power gating configurations. (c) MTTF comparison of different power gating configurations.

observe that TSVs in the top tiers (closest to package pins) experience highest current density and temperature that leads to smallest MTTF metric.

These TSVs are predisposed to potential electromigration and Joule Heating issues than TSVs in the bottom tiers, due to the large amount of currents flowing for long periods of time with elevated temperatures. Such observation further advocates that sizing and distribution of TSVs should be performed by taking into account current demand and temperature distribution along multi-tier systems.

E. Impact of Resonance Frequency

To understand the implications of current transients with different switching frequencies on power and thermal integrity for a multi-tier system, we start by investigating supply noise on the power/ground networks. We consider a wide range of switching frequencies to represents different workloads. We utilize the same multi-tier system composed of ten tiers as in the previous studies. We apply a range of switching frequencies and compute voltage droop and temperature distribution on each tier. We report total analysis runtime of 9 s with 4 iterative convergence steps between electrical and thermal analysis. Fig. 15 shows voltage droop distribution on each tier with respect to switching frequency.

We observe that voltage droop of each tier experiences an increase toward the mid range frequencies with the peak between 100–300 MHz. This is due to the coupling of package inductive parasitics with on-chip decoupling capacitance, which creates an LC tank and introduces excessive harmonics on the power delivery. For high frequencies, these harmonics are localized, sharp and quick transients. At high frequencies suppression of these harmonics is done through local decoupling capacitors, which provide current. However, for low and mid frequencies ranges, excessive switching impact is broader and affect numerous neighboring gates and can last for several clock cycles.

Temperature is also susceptible to resonance frequency. Fig. 16 shows temperature distribution for each tier with respect to varying switching frequency. We notice that for each tier temperature elevates around 100–200 MHz frequency range. The magnitude of temperature increase for each tier differs, i.e., TIER 1 has the largest temperature increase from 27 °C to 39 °C. This behavior is due to the interdependencies between power supply noise and thermal dissipation. As power

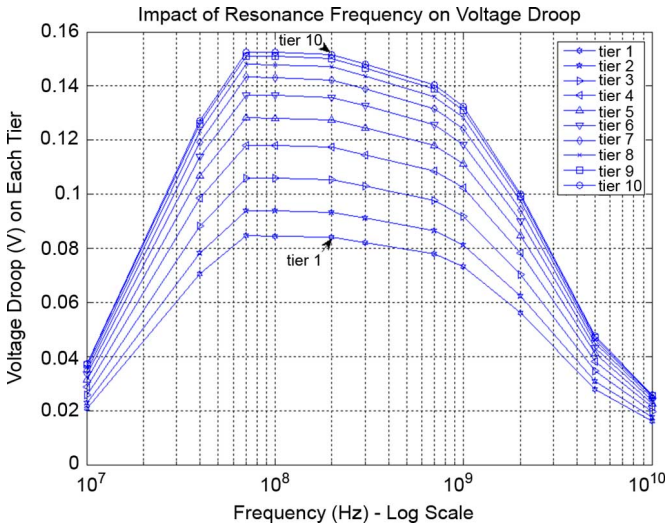

Fig. 15. Voltage droop as function of switching frequency for each tier.

supply noise increases at mid range (resonance) frequencies, temperature rise follows. Also, we observe that temperature remains nearly constant at high frequencies.

For 3-D multi-tier system, impact of resonance frequency is even more crucial than in 2-D systems, due to: 1) a larger amount of parasitics from package to each tier; 2) TSVs propagate supply noise from one tier to another and allow for additional noise resonation between tiers; and 3) increased supply noise lead to elevated temperatures.

V. Impact of Tapered TSVs

Given the conclusions of the previous studies, we determine that power supply noise and thermal dissipation on a 3-D multi-tier are closely coupled and degrade by progressing in opposite directions. Even though the same workload is applied to each tier, power and thermal parameters on each tier can vary considerably.

To counter balance the opposing direction of power and thermal dissipation, we start by investigating the size of TSVs in each tier. We utilize the ten tier multi-tier structure as in previous experiments. We compute the size of TSVs (radius) in three steps: 1) derive the optimal TSV size such that it satisfies voltage droop constraints throughout all tiers; 2) derive the

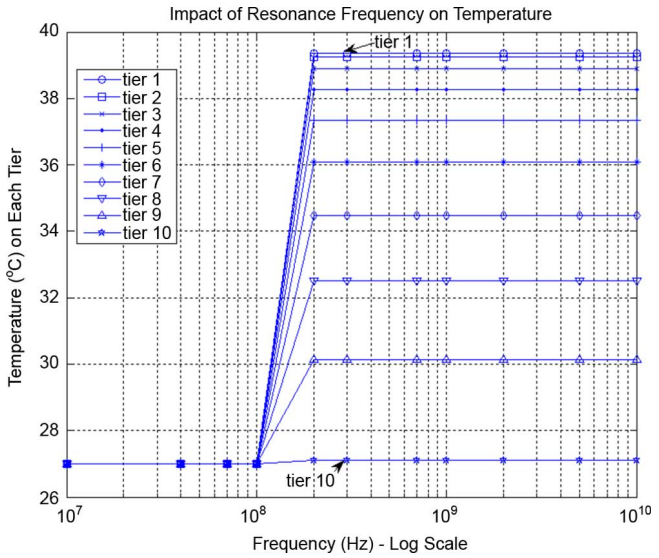

Fig. 16. Temperature as function of switching frequency for each tier.

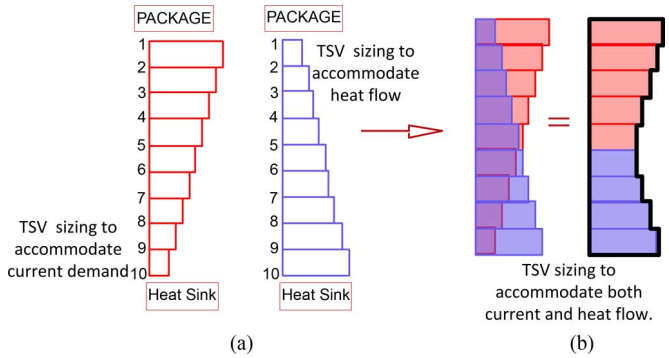

Fig. 17. Illustration of sizing power/ground TSVs (a) to accommodate current and heat flow separately and (b) to accommodate simultaneously current and heat flow considering the opposing direction between voltage droop and thermal dissipation.

optimal TSV size such that it satisfies temperature constraints for all tiers; and 3) combine both solutions from 1) and 2) to derive the optimal TSV size that satisfies both power and thermal constraints. Tapering of TSVs is performed to obtain minimum voltage droop and temperature difference between tiers in order to ascertain similar environmental conditions throughout all the tiers. Thus, even though the TSVs on each tier have different radiuses, they satisfy reliability (EM) and power/thermal integrity constraints. We report runtime of 11 s with 4 convergence steps for performing electrical and thermal analysis.

TSV sizing can be setup as a Thevenin network, where the resistance values and current demand for each tier are known, and TSV resistance values can be derived by satisfying voltage droop constraints. Similarly, TSVs thermal resistances can be obtained by imposing thermal constraints. In this study, we consider only the size of power/ground TSVs and no thermal TSVs are considered. Please note that signal TSVs are also not considered. Tapering of signal TSVs would not be practical from both electrical and thermal perspective. From the electrical perspective, signal TSVs require minimum width to reduce capacitive loading on signals for achieving high performance, thus, tapering would detriment the performance of signal TSVs. From the thermal perspective, signal TSVs are not likely to be uniformly placed and their distribution is highly design specific, which makes tapering unsuitable. Thus, we ignore tapering of signal TSVs.

Fig. 17(a) shows an illustration for sizing power/ground TSVs for current and heat flow separately by considering the opposite direction of voltage droop and temperature increase. In the case of sizing the TSV to satisfy current flow, the top tier (TIER 1) TSVs (closest to the package) is the widest in side in order to allow large current flow at low resistance. The size of TSVs narrows down as it reaches the bottom-most tier (TIER 10) following the decrease in current demand. Hence, TSV sizing is proportional to the current flow through each tier. Similarly, but in the opposite direction, TSV sizing is obtained to sustain temperature levels for each tier. The final TSV size is obtained by combining TSV dimensions for heat and current flow as illustrated in Fig. 17(b).

Please note that a uniform TSV size can also be applied to satisfy both power and thermal constraints. However, the focus of this study is to investigate the impact of nonuniform TSV radius which can be obtained either by designer choice or as a manufacturing result, i.e., overlay defects and/or time-dependent dielectric breakdown (TDDB) effect [27]. Tapered TSVs impose different keep-out zone for circuit implementation. They can provide additional area on some tiers (with narrow TSVs) for circuit and routing. The applied radiuses of tapered TSVs are incremented by 2 μm between tiers as: $\mathrm{R}_{910} = 9\ \mu\mathrm{m}$, $\mathrm{R}_{89} = 7\ \mu\mathrm{m}$, $\mathrm{R}_{78} = 5\ \mu\mathrm{m}$, $\mathrm{R}_{67} = 3\ \mu\mathrm{m}$, $\mathrm{R}_{56} = 1\ \mu\mathrm{m}$, $\mathrm{R}_{45} = 3\ \mu\mathrm{m}$, $\mathrm{R}_{34} = 5\ \mu\mathrm{m}$, $\mathrm{R}_{23} = 7\ \mu\mathrm{m}$, $\mathrm{R}_{12} = 9\ \mu\mathrm{m}$ while uniform TSV radius is $R = 1\ \mu\mathrm{m}$. Additionally, we investigate TSV tapering by four other different coefficients as $0.2\ \mu\mathrm{m}$, $0.5\ \mu\mathrm{m}$, $1\ \mu\mathrm{m}$, and $1.5\ \mu\mathrm{m}$. For example when tapering is applied by incrementing the radiuses by $0.2\ \mu\mathrm{m}$, TSVs between each tier have radiuses as $\mathrm{R}_{910} = 1.8\ \mu\mathrm{m}$, $\mathrm{R}_{89} = 1.6\ \mu\mathrm{m}$, $\mathrm{R}_{78} = 1.4\ \mu\mathrm{m}$, $\mathrm{R}_{67} = 1.2\ \mu\mathrm{m}$, $\mathrm{R}_{56} = 1\ \mu\mathrm{m}$, $\mathrm{R}_{45} = 1.2\ \mu\mathrm{m}$, $\mathrm{R}_{34} = 1.4\ \mu\mathrm{m}$, $\mathrm{R}_{23} = 1.6\ \mu\mathrm{m}$, $\mathrm{R}_{12} = 1.8\ \mu\mathrm{m}$. We applied tapered TSVs on the multi-tier structure and derive voltage droop and temperature distribution for each tier when all tiers are switching simultaneously. We compared these results with uniformly sized TSVs as shown in Fig. 18(a) and (b), respectively.

We observe that TIER 10 experiences 90 mV with uniform TSVs and about 65 mV when TSVs are tapered by 2 μm. Additionally, we notice that voltage droop decreases as the size of tapering is increased from $0.2\ \mu\mathrm{m}$ to $2\ \mu\mathrm{m}$. Furthermore, we notice that tapered TSVs introduce slightly higher voltage droop for TIER 1 and some cases TIER 2 which is due to the resistance parasitic difference among the tiers. For bottom-most tiers (i.e from TIER 3 to 10) tapered TSVs reduce a considerable amount of voltage droop. Similarly, there is a considerable temperature drop off (43 °C to 30 °C for TIER 1) when tapered TSVs are used. Likewise, temperature increase is reduced considerably when the size of tapering is increased from $0.2\ \mu\mathrm{m}$ to $2\ \mu\mathrm{m}$. Such observations clearly highlight the benefits of tapered TSVs to counterbalance the effect of power and thermal distribution.

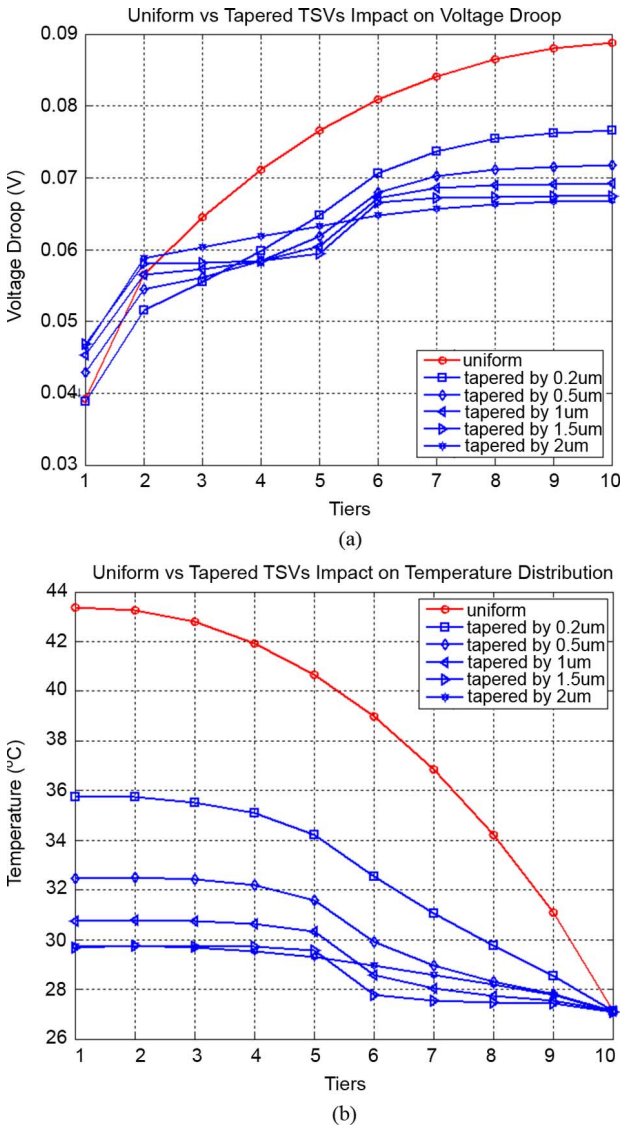

Fig. 18. Comparisons between uniform and tapered size TSVs, (a) voltage droop distribution comparison, and (b) temperature distribution for each tier.

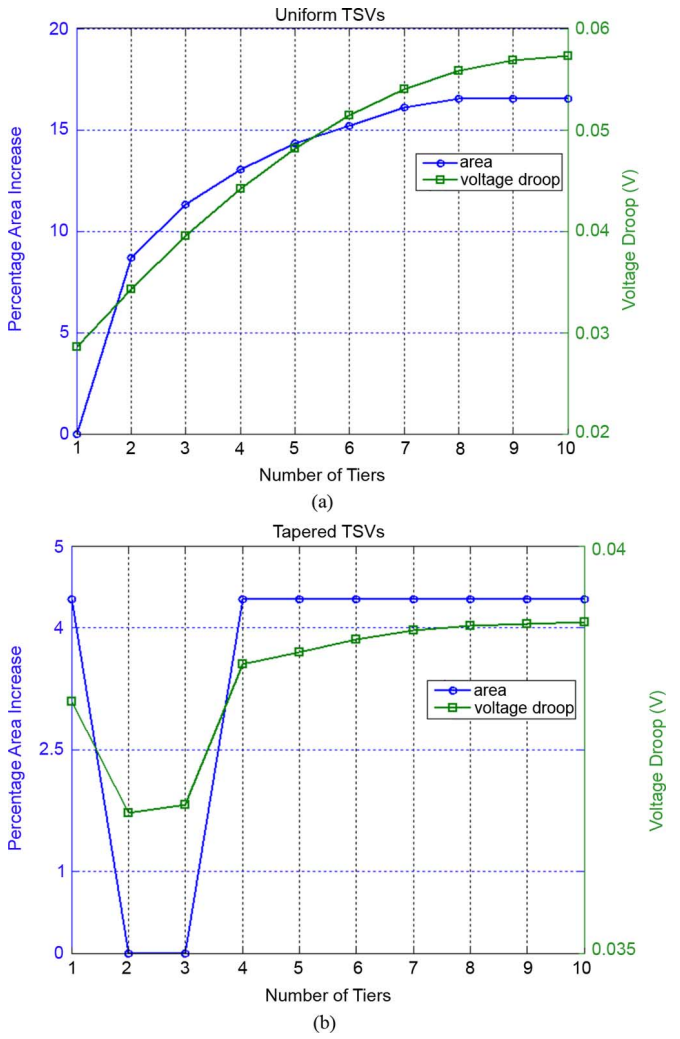

Fig. 19. Voltage droop and circuit area increase required for each tier while obtaining same performance on all tiers for (a) uniform and (b) tapered TSVs.

VI. Design Implications

We implemented the two types of power and ground TSVs (uniform and tapered) on a small design where the same circuit is implemented on each tier. The sample circuit consists of only buffers inserted on the cell area of 300 μm by 300 μm. To capture the impact of power/ground TSVs, there is no data communication between tiers, hence, no signal TSVs are utilized. The sample circuit is floorplanned, placed & routed and timing measurements are performed for determining nominal performance (in the presence of no power supply noise and room temperature conditions). Next, the sample circuit is inserted on each tier where power and ground networks are connected through the power/ground TSVs. The objective of this analysis is to obtain the percentage of circuit area increase for each tier in presence of power supply noise and heat dissipation, given that the nominal performance is required on each tier. Such analysis serves as an indicator to the impact that the size of TSVs have on design rules and methodology that should be considered early on during the design cycle. We report analysis runtime of 31.5 s with 4 convergence steps.

The area of the sample circuit can be varied by changing the sizes of the buffers in order to meet the timing constraints. In the following analyses, we derive the area of the sample circuit when uniform and tapered TSVs are used. Uniform TSV radius is 1 μm while tapered TSVs are as: $R_{910} = 5\ \mu$m, $R_{89} = 4\ \mu$m, $R_{78} = 3\ \mu$m, $R_{67} = 2\ \mu$m, $R_{56} = 1\ \mu$m, $R_{45} = 2\ \mu$m, $R_{34} = 3\ \mu$m, $R_{23} = 4\ \mu$m, $R_{12} = 5\ \mu$m. Circuit area is calculated by considering only the size of the buffer gates. The number of TSVs remains unchanged but their radiuses vary. We note that the keep-out area of the TSVs will vary based on their size, which can limit the available area for circuit implementation.

Fig. 19(a) shows the results of the analysis performed with uniform sized TSVs. The area of the sample circuit is derived for each tier and plotted against the measured voltage droop. We observe that the area of the circuit increases on the tiers that are further away from the power and ground pins i.e., higher-level tiers. Such trend is similar to the increase in voltage droop. Voltage droop levels can reach up to 60 mV for TIER 10 while it requires a 16.5% increase in circuit area in order to satisfy the fixed performance constraints among all the tiers. Fig. 19(b)

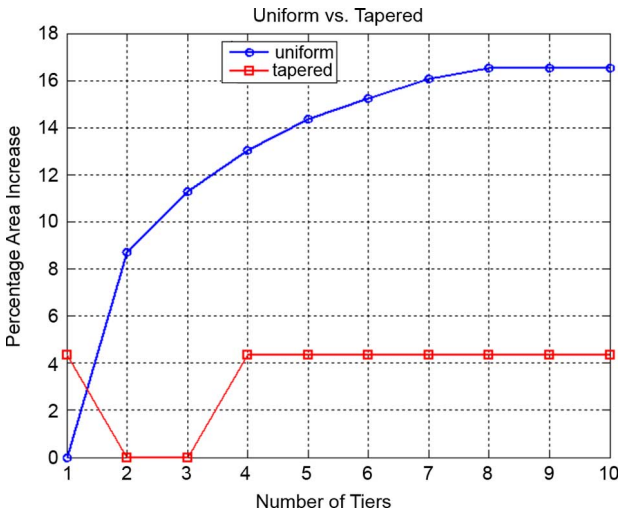

Fig. 20. Circuit area increase for all tiers using uniform and tapered TSVs.

shows the results of the analysis performed with tapered TSVs. We observe that tapered power and ground TSVs provide more flexibility to meet timing constraints without a large increase in circuit area, such as varying from 0 to 4.3% of area increase with a range of 35 to 40 mV of voltage droop on various tiers. We observe that TIER 2 and 3 do not require an area increase to satisfy the performance constraints. Additionally, the behaviors of the rest of the tiers are uniform and require a 4.3% increase in circuit area for obtaining the same performance throughout all the tiers. Thus, tapered TSVs allow alleviating significant voltage droop and heat dissipation issues, which consequently facilitates in meeting timing constraints.

Fig. 20 shows the comparison of percentage area increase required when uniform and tapered TSVs are used. Results show that tapered TSVs provide a considerable reduction in voltage droop and heat dissipation to meet performance constraints with a small increase in circuit area. This is a new, unpublished observation, as yet to be addressed in the design and CAD community.

VII. Conclusion

In this work, analytical physical models and power-thermal analysis techniques are presented and utilized to investigate power and thermal integrity issues in 3-D integration. The physical models consider parasitics effects unique to 3-D integration such as: parasitics of TSVs, distributed decoupling capacitors available from each tier, parasitics of power delivery networks and C4 pads. We provide an extensive study of power and thermal dissipation issues in 3-D integration considering several aspects such as:

- single and multi-tier switching effects on 3-D power and thermal dissipation;
- impact of self and mutual inductance of TSVs on power and thermal integrity;
- switching frequency and occurrence of resonance effects;
- power gating and impact of decoupling capacitors;
- tapered TSVs and their impact on power and thermal integrity and their design implications.

Our study shows that tapered power/ground TSVs can be a potential solution for mitigating power and thermal issues in 3-D integration.

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