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João Azevedo, Arnaud Virazel, Alberto Bosio, Luigi Dilillo, Patrick Girard, et al.. Impact of Resistive-Bridge Defects in TAS-MRAM Architectures. ATS: Asian Test Symposium, Nov 2012, Niigata, Japan. pp.125-130, 10.1109/ATS.2012.37 . lirmm-00806809

HAL Id: lirmm-00806809

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Impact of Resistive-Bridge Defects in TAS-MRAM Architectures*

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Abstract—***Magnetic Random Access Memory (MRAM) is an emerging memory technology. Among existing MRAM technologies, the Thermally Assisted Switching (TAS) MRAM technology offers several advantages such as selectivity, single magnetic field and high integration density. In this paper, we analyze resistive-bridge defects that may affect the TAS-MRAM architecture. Electrical simulations were performed on a hypothetical 16-words TAS-MRAM architecture enabling any sequences of read/write operations. Results show that both read and write operations may be affected by these defects. Especially, we demonstrate that resistive-bridge defects may have a local (single cell) or global (multiple cells) impact on the TAS-MRAM functioning. As these analysis results will be further used to develop effective test algorithms targeting faults related to actual resistive bridge-defects that may affect TAS-MRAM architecture.***

Keywords–non-volatile memories, spintronics, TAS-MRAM, resistive-bridge defects, fault modeling, test.

I. INTRODUCTION

Nowadays, Non-Volatile Memories (NVMs) are more and more integrated in consumer applications. Though widely used, Flash memories still have several drawbacks such as high supply voltage requirement, low speed and susceptibility to reliability issues due to high electric field for programming operations. On the other hand, Magnetic Random Access Memory (MRAM) is an emerging technology with high data processing speed, low power consumption and high integration density compared with Flash memories. Moreover, these memories are non-volatile with fair processing speed and reasonable power consumption when compared to Static RAMs (SRAMs). MRAM probably is the closest to an ideal "universal memory" since it is non-volatile and fast, and can be cycled indefinitely. Thus, MRAM may be used as NVM as well as SRAM and DRAM according to the 2011 International Technology Roadmap for Semiconductors (ITRS) [1].

MRAMs have the potential to mitigate almost all Flash related issues but defects can occur as with any other kind of memory. Only few papers on MRAM testing can be found in the literature, and target exclusively FIMS (Field Induced Magnetic Switching) MRAMs technologies. In [2], authors present the Write Disturbance Fault (WDF) model; a fault that affects data stored in the MRAM cells due to an excessive magnetic field during write operation. In [3], two new fault models were identified and are related to the Magnetic Tunnel Junction (MTJ) behavior.

A thorough investigation and a deep analysis must be done for testing MRAMs. In [4] we have presented the first analysis of resistive-open defects in a TAS-MRAM memory organization. We have defined a hypothetical TAS-MRAM architecture composed of an array of Magnetic Tunnel Junctions (MTJ) and a set of drivers/decoders enabling all sequences of read/write operations. Among the possible resistive-open defects, the ones that have the most significant impact on the heat current of the TAS-MRAM were analyzed in detail. Resulting fault models are TF0 (Transition Fault 1 to 0), TF1 (Transition Fault 0 to 1) and WD1 (Write Destructive Fault 1). In [5] defects in the bit-line and word-line selection were analyzed in details. Resulting fault models include SA0 (Stuck-at 0), SA1 (Stuck-at 1) and all types of SCF (State Coupling Faults).

Resistive bridge faults (RBF) are the major class of defects in deep submicron CMOS fabrication process [6] [7]. In this paper, we present a study on resistive-bridge defects injected in a hypothetical TAS-MRAM architecture. The location of injected defects takes into account adjacent lines of the same metal layer or between metal layers of the layout. First, an overall analysis of CMOS related resistive-bridge defects for the proposed architecture is given. Then, a detailed analysis for an MTJ-specific resistive-bridge defect is also performed. Electrical simulations performed show that read and write operations may be corrupted depending on the defect location and size. In addition, we also show that resistive-bridge defects may have a local (single cell) or global (multiple cells) impact on the TAS-MRAM functioning. Such results will be helpful to define an efficient test algorithm to fully test MRAM structures.

The rest of the paper is organized as follows. Section II provides the fundamentals and background on MRAM technologies. The proposed TAS-MRAM architecture is described in Section III. The resistive-bridge defect analysis is provided in Section IV. Section V concludes the paper.

II. MRAM TECHNOLOGIES

MRAMs are Spintronic devices that store data in Magnetic Tunnel Junctions (MTJs). A basic MTJ device is usually composed of two ferromagnetic (FM) layers separated by an insulating layer, as shown in Figure 1. One of the FM layers is pinned and acts as a reference layer. The other one is free and can be switched between, at least, two stable states. These

* This work has been funded by the French national research agency under the framework of the ANR-10-SEGI-007 EMYR (Enhancement of MRAM memory Yield and Reliability) project.

1081-7735/12 $26.00 © 2012 IEEE
DOI 10.1109/ATS.2012.37

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states are parallel or anti-parallel with respect to the reference layer. When the MTJ is in the parallel state, it offers the minimum resistance (Rmin) while the maximum resistance (Rmax) is obtained when anti-parallel. The difference between Rmin and Rmax, quantified by the Tunnel Magneto Resistance (TMR), is high enough to be sensed during the read operation.

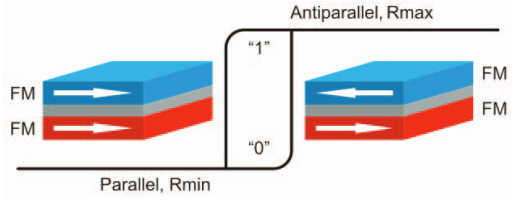

Figure 1. MTJ in parallel and antiparallel states

A read operation consists in determining the MTJ's magnetization state and can be performed by voltage or current sensing across the MTJ stack. A CMOS sense amplifier is used to retrieve the stored bit information. High TMR allows simple and stable sense amplifiers, improving reading accuracy [8].

A write operation can be performed using magnetic fields or spin polarized current and depends on MRAM technologies: **FIMS** (Field Induced Magnetic Switching), **Toggle Switching**, **TAS** (Thermally Assisted Switching) and **CIMS** (Current Induced Magnetic Switching.

The first MRAM generation (**FIMS**) relies on the Stoner-Wohlfarth theory of coherent rotation in single domain particles [9]. In this approach, the energy required to reverse the magnetization is minimized by applying simultaneously two perpendicular magnetic fields. The amounts of magnetic fields necessary to switch the magnetization state are mainly determined by shape anisotropy and edge roughness.

The MTJ is fully selected when two magnetic fields are applied to it. The ability to write a fully-selected MTJ without disturbing half-selected MTJs is called write margin. Finding a set of magnetic fields, which can be used to program all cells, becomes difficult due to the very narrow write margin in this technology [10] as a small deviation of MTJ's characteristics has a huge influence in the switching field distribution in large bit arrays. Another issue is the thermal activation of half-selected MTJs, which increases addressing errors.

A new approach called **Toggle Switching** was proposed by Savtchenko [11] to overcome the selectivity issue of FIMS technology. The FM layers were replaced by synthetic layers and two perpendicular current lines generating magnetic fields are oriented at 45 degrees from the two magnetization stable states. This methodology relies on the unique behavior of the synthetic antiferromagnetic (SAF) free layer.

To toggle the magnetization state, two magnetic pulses are applied in four steps:

1. Switch on bit-line magnetic field.
2. Switch on word-line magnetic field.
3. Switch off bit-line magnetic field.
4. Switch off word-line magnetic field.

When the field is removed the synthetic storage layer will be reversed. A prior read is mandatory as it is only possible to toggle the state. This drawback is compensated by the advantage of using a single current polarity to create the magnetic fields.

Thermally Assisted Switching™ is an alternative switching method for MRAMs. In the scheme proposed by Spintec [12] and industrialized by Crocus Technology, the MTJ is modified by inserting an Anti-FerroMagnetic (AFM) layer that pins the storage layer while below its blocking temperature (T_B).

In AFM materials, the magnetic moments of atoms are aligned in a regular pattern, neighboring spins pointing in opposite directions. This organization vanishes above T_B and the material becomes paramagnetic. When MTJ's temperature rises above T_B, the storage layer is freed and can be reversed under the application of a small magnetic field provided by a single field-line. The magnetic field is maintained beyond the heating voltage pulse to ensure the correct pinning of the storage layer.

TAS approach offers several advantages. The selectivity problem is reduced since only heated MTJs are able to switch and all other MTJs hold their stable state as they remain below their blocking temperature. Although TAS needs an additional heating current, this current is much smaller than the current used to generate the second magnetic field in FIMS-MRAM. The integration density is improved due to thermal stability and the need of only one field-line. Finally, as the free layer can be pinned to any stable state, multi level logic can be achieved [13]. TAS is for the moment the most promising MRAM solution as it mitigates most drawbacks from its predecessors and offers scalability down to the 65nm technology node and below.

Current Induced Magnetic Switching (**CIMS**) is the most recent MRAM technology. The writing is accomplished by injecting a spin-polarized high current density through MTJ without the assistance of any external magnetic field [14]. This approach relies on Spin Transfer Torque (STT) effect. STT phenomenon is the exchange of spin angular momentum between an incoming spin-polarized current and the local magnetization. This effect applied to MRAMs could restore the scalability beyond several Gbit/chip. However, there are some problems to solve in this recent technology. Lowering the write current density while maintaining data stability and improving the read signal are the main concerns of spin induced reversal mechanism. This raises considerable challenges since the MRAM cells must be able to withstand high current densities without exceeding the MTJ's breakdown voltage. Moreover, the transistor's size is related to the writing current, which sets a limit on the memory density.

III. THE TAS-MRAM ARCHITECTURE

Figure 2 shows the TAS-MRAM architecture we have chosen for our study. The organization is done in a square matrix that has 2^{MR} rows and 2^{NC} columns, for a total storage capacity of 2^{MR+NC} bits per page, where MR and NC are the numbers of bits used to specify the row and column address, respectively. In our case study, MR and NC are equal to 2 and the number of pages is 4; hence, the storage capacity is 64 bits (16 words of 4 bits). Each cell in the array is connected to one of the row-lines, called word-lines, and connected to one of the column-lines, called bit-lines. A particular set of MTJs can be

accessed for a read or write operation by selecting its word-line and bit-line.

During a read operation, the read driver applies a small voltage that generates negligible heat to both the selected MTJ and a reference MTJ. The reference MTJ is halfway between the high and low resistance values. The resistance difference is then sensed to determine the stored data in the selected MTJ.

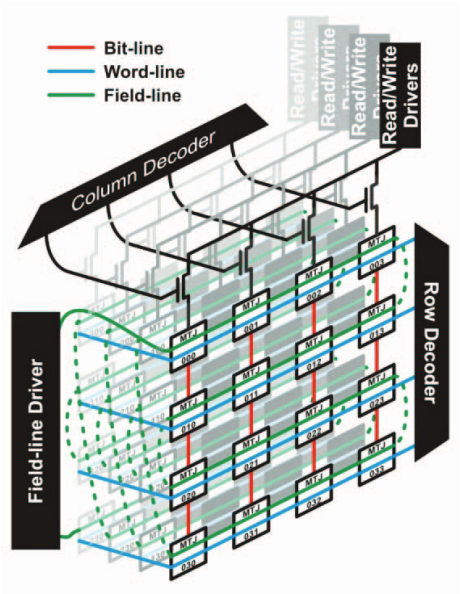

Figure 2. TAS-MRAM architecture

A write operation is performed as follows:

- Initially, the write driver applies a voltage to heat the selected MTJ above its T_B (about 150 °C).
- Next, the field-line driver applies a current to generate the data zero magnetic field. While the MTJ is cooled down below T_B, the magnetic field is maintained.
- Then, the field-line driver inverses the current direction and the MTJ is heated again to perform the write 1 operation, if needed. When the MTJ reaches room temperature, the writing procedure is accomplished.

This approach allows writing logic '0' and logic '1' in one cycle to different MTJs sharing the same field-line. Note that, a write 1 operation (denoted W1) consists of applying first a write 0 and then a write 1 operation. Conversely, a write 0 operation (denoted W0) consists of applying only a write 0 operation. These writing procedures are inspired by the Flash programming procedures in which a write operation (write 1) is always preceded by an erase operation (write 0).

Electrical simulations were performed using the TAS-MTJ model developed by Spintec [12]. This model is based on the physical equations of the MTJ and it is calibrated with respect to the targeted TAS-MRAM technology. Moreover, this model is compiled in C language and is compatible with Spectre [15] simulator of the standard Cadence design suite.

Table I summarizes simulated fault-free characteristics of $MTJ_{1,1,1}$ ($MTJ_{i,j,k}$ with i □ page number, j □ row number and k □ column number) in the second page, second column and second line of the TAS-MRAM architecture shown in Figure 2. The first column in the table gives the four possible operations R0, R1, W0 and W1. The next five columns provide all the MTJ's parameters:

- **V** – Voltage level at the MTJ interface.
- **I** – Current passing through the MTJ during read or write operations.
- **R** – Resistance of the MTJ.
- **T** – Temperature of the MTJ during operations.
- **M** – Magnetization state that is related to the angle between the two ferromagnetic layers. The parallel magnetization state is represented ideally by "1 □ logic 0" and the anti-parallel magnetization state by "-1 □ logic 1". The magnetization state is related to resistivity of the MTJ.

Finally, the last column gives the sensing voltage (S) during read operation only. The two resistive states of the MTJ are 1.48kΩ for Rmin and 2.80kΩ for Rmax when reading. In normal operation the sensing voltage (S) is around 165mV for Rmin and 254mV for Rmax. During write operations, the current that passes through the MTJ is high enough to heat its temperature above the blocking temperature, i.e. 193°C for W0 and 193/183°C for W1. We can see that the MTJ's resistivity is different during reading and writing even if the magnetization state is the same. This is due to the voltage applied to the MTJ as well as its operating temperature.

TABLE I. $MTJ_{1,1,1}$ CHARACTERISTICS UNDER READ/WRITE OPERATIONS

	$MTJ_{1,1,1}$ parameters					
Operation	**V (mV)**	**I (uA)**	**R (kΩ)**	**T (°C)**	**M**	**S (mV)**
R0	111.49	74.89	1.48	31.16	1	165.67
R1	202.35	72.11	2.80	34.26	-1	254.49
W0	745.32	606.59	1.22	193.18	1	n.a.
W1	745.32 863.09	606.59 542.63	1.22 1.59	193.18 183.75	-1	n.a.

In Figure 3 are shown temperature profiles for a W0 operation performed in a 16-bit fault-free TAS-MRAM memory page. The MTJs are written row by row from $MTJ_{x,0,0}$ to $MTJ_{x,3,3}$. We can observe that the temperature rises only once per writing cycle in response to the voltage/current applied to each MTJ. On the other hand, Figure 4 shows the profiles for a W1 operation performed on the same fault-free memory page. In this case, the temperature of each MTJ rises twice per writing cycle in accordance with the writing approach previously described.

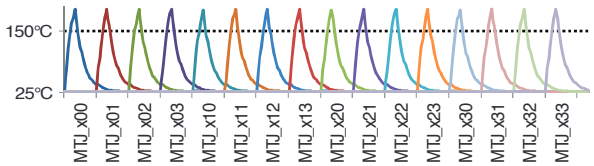

Figure 3. 16-bit W0 fault-free temperature profiles

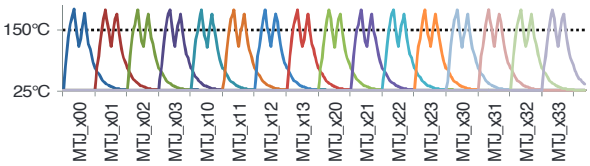

Figure 4. 16 bits W1 fault-free temperature profiles

IV. Resistive-Bridge Defect Analysis

The defect injection in the TAS-MRAM array is depicted in Figure 5. Resistive-bridge defects are placed on adjacent lines of the same metal layer or between metal layers as follows:

Defects related to traditional CMOS fabrication process:

- **Df1**: resistive-bridge defect between drain and gate of bit-line selection transistor.
- **Df2**: resistive-bridge defect between source and gate of bit-line selection transistor.
- **Df3**: resistive-bridge defect between drain and gate of MTJ selection transistor.
- **Df4**: resistive-bridge defect between source and gate of MTJ selection transistor.

Defect related to MTJ fabrication process:

- **Df5**: resistive-bridge defect in parallel with the MTJ.

These five defects may impact the TAS-MRAM behavior in different ways. In the following sub-sections we assume $MTJ_{1,1,1}$ as target cell and we show an overall analysis of how resistive-bridge defects affect the TAS-MRAM behavior.

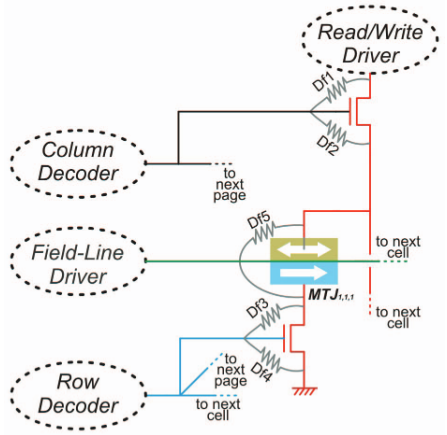

Figure 5. Resistive-bridge defect injection with respect to $MTJ_{1,1,1}$

A. Resistive-bridge related to traditional CMOS fabrication process (Df1, Df2, Df3 and Df4)

We performed W1 operations in the presence of each defect in order to observe how they affect the TAS-MRAM behavior. As we did to obtain the fault-free temperature profiles, the MTJs are written row by row from $MTJ_{x,0,0}$ to $MTJ_{x,3,3}$. In Figure 6 we first observe that Df1 on the bit-line selection transistor where the $MTJ_{1,1,1}$ is connected impacts the page where the defect is located for all write operations and none of them were correctly performed. All MTJs in the same page share the same write driver as shown in Figure 2 and, due to the defect, there will be more than one MTJ selected in the page. We can also observe that, on the remaining pages, only operations performed on the second bit-line were affected. This faulty behavior is due to the fact that the column decoder cannot fully select the bit-line in the presence of the defect.

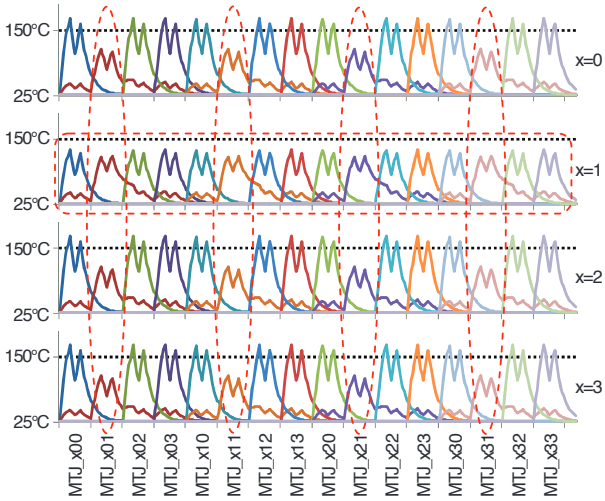

Figure 6. W1 temperature profiles under Df1 (1Ω)

When the writing sequence is applied in presence of Df2 on the bit-line selection transistor which $MTJ_{1,1,1}$ is connected to, only operations performed on the defective bit-line in all pages are affected as shown in Figure 7. In this case, the column decoder cannot fully select the bit-line in the presence of the defect as well.

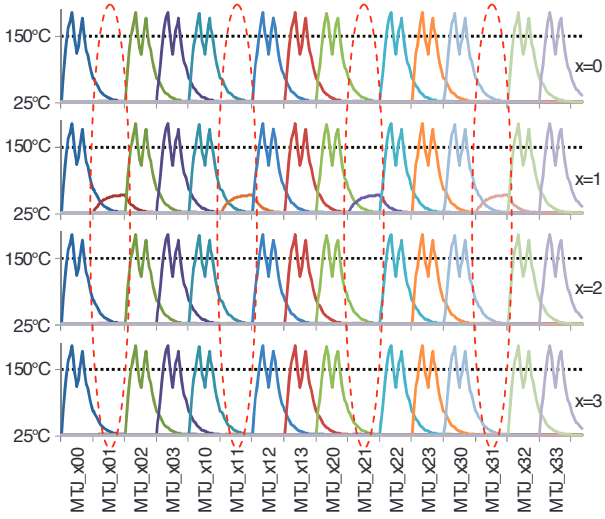

Figure 7. W1 temperature profiles under Df2 (1Ω)

In Figure 8 we first observe that Df3 on the selection transistor of $MTJ_{1,1,1}$ impacts all MTJs that share the same word-line in all pages. As in the previous defect analysis, this behavior is related to the MRAM architecture, i.e. the row decoder is shared by all pages. Moreover, the defect affects also all MTJs in the bit-line where $MTJ_{1,1,1}$ is connected.

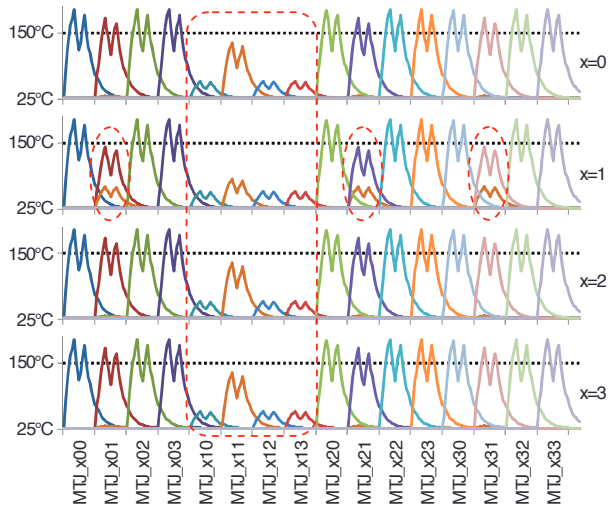

Figure 8. W1 temperature profiles under Df3 (1Ω)

Finally, when the write sequence is applied in the presence of Df4 in the selection transistor of $MTJ_{1,1,1}$, all operations performed in the word-line shared by the MTJ in all pages are affected as we can see in Figure 9. In this case there is no MTJ selection since Df4 act a short between the row decoder and the ground.

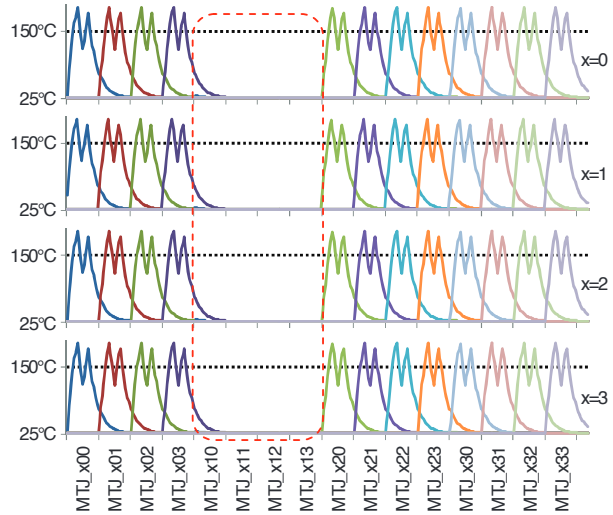

Figure 9. W1 temperature profiles under Df4 (1Ω)

B. Resistive-bridge related to MTJ fabrication process (Df5)

Figure 10 plots the sensing voltage (S) when Df5 is injected for R1 and R0 operations, respectively. Note that the dashed area represents the minimum value of S (Min S) for a proper R1 operation and the maximum value of S (Max S) for R0. We have determined the read voltage threshold in a way to guarantee both logic '0' and logic '1' during read operations. Based on R0 and R1 simulations performed on all MTJs of the TAS-MRAM architecture presented in Figure 2, Min S and Max S values are:

- Min S for a R1 = 230mV represents the upper bound of the dashed area.
- Max S for a R0 = 187mV represents the lower bound of the dashed area.

If the S value is in between the dashed area, the output logic data from the sense amplifier is not reliable.

As shown in Figure 10, R0 operations on $MTJ_{1,1,1}$ are not affected by Df5 as the sensing voltage is always under the dashed area. In this case all read operations return logic '0'. However, R1 operations are not reliable for $5k\Omega < Df5 < 17k\Omega$ as the sensing voltage is in between the required levels. When Df5 lies below $5k\Omega$, the sense amplifier always return logic '0' even if the $MTJ_{1,1,1}$ contains logic '1'. In this case, the current passing through the defect reduces the sensing voltage and makes R1 operations to be faulty.

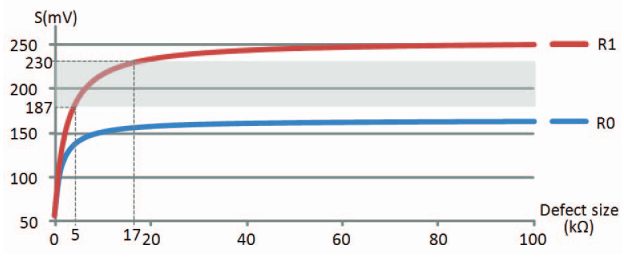

Figure 10. R0 and R1 operations performed on $MTJ_{1,1,1}$ under Df5

Table II summarizes simulated characteristics of write operations performed on $MTJ_{1,1,1}$ in the presence of Df5. The first column gives the operation and the second the simulated defect sizes. The next four columns provide the MTJ's parameters. Transition sequences (1W0 and 0W1) are affected by Df5 smaller than $5.4k\Omega$ and $6.3k\Omega$ defect size, respectively. Also, for Df5 between $5.5k\Omega$ and $6.6k\Omega$, the 1W1 operation is destructive. In this specific range write 1 ceases to work while write 0 works properly. Note that 0W0 is not affected, as there is no transition.

TABLE II. $MTJ_{1,1,1}$ CHARACTERISTICS UNDER DF5 (WRITE OPERATIONS)

Sequence	Defect size (kΩ)	V (mV)	I (uA)	T (°C)	M
1W0	5.4	775.87	446.35	149.93	-1
	5.5	777.30	447.95	150.60	+1
0W1	5.0	670.25 673.32	512.93 510.66	149.80 143.05	+1
	5.1	671.71 674.82	514.49 512.20	**150.46** 143.67	+1
	6.3	685.72 689.23	529.85 527.40	**156.98** 149.80	+1
	6.4	686.66 690.20	530.87 528.44	**157.43** **150.22**	-1
1W1	5.4	775.87 779.05	446.35 444.04	149.93 143.27	-1
	5.5	777.30 780.52	447.95 445.60	**150.60** 143.90	+1
	6.6	790.30 793.90	462.45 459.99	**156.88** 149.89	+1
	6.7	791.30 794.89	463.54 461.09	**157.36** **150.34**	-1

Figure 11 and Figure 12 show how the current provided by the write driver during the write operation is shared between

the MTJ and Df5 (as they are in parallel configuration). As the resistive-bridge defect increases, more current passes through the MTJ that only reaches the blocking temperature when the defect size is near $5.4k\Omega$ for a write 0 operation and $6.6k\Omega$ for a write 1 operation following the writing approach previously described.

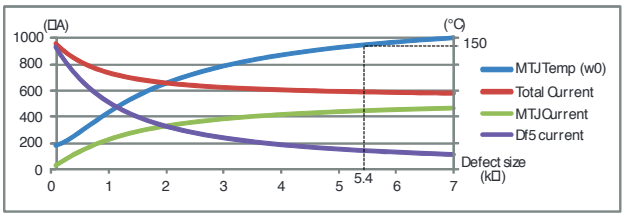

Figure 11. Write 0 operation performed on $MTJ_{1,1,1}$ under Df5

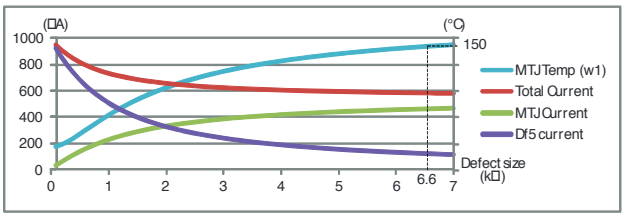

Figure 12. Write 1 operation performed on $MTJ_{1,1,1}$ under Df5

From this set of simulations we conclude that:

- R0 and 0W0 operations are not affected by Df5.
- R1 operation is affected by Df5 below $17k\Omega$
- 1W0 operation is affected by Df5 below $5.4k\Omega$
- 0W1 operation is affected by Df5 below $6.4k\Omega$
- 1W1 operation is affected by Df5 for a specific range $5.5k\Omega < Df1 < 6.6k\Omega$.

V. CONCLUSION

In this paper, we have analyzed resistive-bridge defects in a proposed TAS-MRAM architecture. Electrical simulations performed in the presence of these defects show that both read and write operations may be affected. Resistive-bridge defects may have a local (single MTJ) or global (multiple MTJs) impact depending on where they are located. This study provides insights into the various types of MRAM defects and their behavior. As future work, we plan to use these analyses results to guide the test phase by providing effective test algorithms targeting fault related to actual defects that may affect TAS-MRAM architectures.

REFERENCES

[1] Semiconductor Industry Association, "International technology roadmap for semiconductors (ITRS)", 2011.

[2] C.L. Su, C.W. Tsai, C.W. Wu, C.C. Hung, Y.S. Chen, M.J. Kao, "Testing MRAM for Write Disturbance Fault", IEEE International Test Conference, pp. 277-288, 2006.

[3] C.L. Su, R.F. Huang, C.W. Wu, "MRAM Defect Analysis and Fault Modeling", IEEE International Test Conf., pp. 124-133, 2004.

[4] J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, G. Prenat, J. Alvarez-Herault and K. Mackay, "Impact of Resistive-Open Defects on the Heat Current of TAS-MRAM Architectures", in Proc. of Design Automation and Test in Europe, pp.532-537, 2012.

[5] J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, G. Prenat, J. Alvarez-Herault and K. Mackay, "Coupling-Based Resistive-Open Defects in TAS-MRAM Architectures", to appear in Proc. of IEEE European Test Symp. one-page poster, 2012.

[6] P. Engelke, I. Polian, M. Renovell, and B. Becker, "Simulating resistive bridging and stuck-at faults", IEEE Transactions on Computer-Aided Design, vol. 25, pp. 2181–2192, Oct. 2006.

[7] S. Khursheed, U. Ingelsson, P. Rosinger, B. M. Al-Hashimi, and P. Harrod, "Bridging fault test method with adaptive power management awareness", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 6, Jun. 2008, pp. 1117–1127.

[8] D.D. Tang, Y.J. Lee, "Magnetic Memory – Fundamentals and Technology", Cambridge University Press, UK, 2010.

[9] C. Tannous, J. Gieraltowski, "The Stoner–Wohlfarth model of ferromagnetism", Eur. J. Phys., 29, 475, 2008.

[10] T.M. Maffitt et al., "Design Considerations for MRAM", IBM J. Res. Dev., 50(1):25–39, 2006, ISSN 0018-8646.

[11] L. Savchenko, B. N. Engel, N. D. Rizzo, M. F. D. Herrera, J. A. Janesky, U.S. Patent No. 6,545,906 (Apr. 2003).

[12] M. El Baraji et al., "Dynamic Compact Model of Thermally Assisted Switching Magnetic Tunnel Junctions", Journal of Applied Physics, Vol. 106, N° 12, 2009.

[13] W. Guo, "Compact Modeling of Magnetic Tunnel Junctions and Design of Hybrid CMOS/Magnetic Integrated Circuits", Ph.D. Thesis at Institut Polytechnique de Grenoble, 2010.

[14] J. Slonczewski, "Current-driven excitation of magnetic multilayers", Journal of Magnetism and Magnetic Materials, 159:L1–L7, 1996.

[15] Cadence Inc., Spectre, User Guide 2008.

[16] A. J. van de Goor and Z. Al-Ars, "Functional Memory Faults: A Formal Notation and a Taxonomy", IEEE VLSI Test Symposium, pp. 281-286, 2000.