Tutoriel intitulé "Power-Aware Testing and Test Strategies for Low Power Devices"

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G1

POWER-AWARE TESTING AND TEST STRATEGIES FOR LOW POWER DEVICES

DATE 08 TUTORIAL NOTES

Half-day tutorial on

Power-Aware Testing and Test Strategies for Low Power Devices

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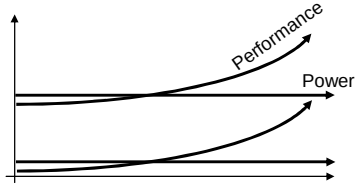
Motivation and Objectives

Power Consumption Trends

- The new power-performance paradigm:



- By-product of power consumption trends:
  - Low (fixed) power budget to limit power density
  - But ever increasing integration and performance …
  - Adoption of low-power design and power management techniques

Motivation and Objectives

Power Impact on Test

- Power constraints have severe impact on test
- Implications to test and DfT engineers / test tool developers :
  - Reduce power consumption also in test mode
  - Test strategies for power management structures
- Objectives of this tutorial:
  - Learning more about the impact of power during test
  - How to alleviate test power issues
  - How low power devices can be tested safely

Outline

1. Introduction
2. Test Power Metrics
3. Test Power Issues
4. Test Application Environments

Part 1

5. Low Power Test Pattern Based Approaches
6. Low Power Design-for-Test
7. Low Power Test Data Compression
8. System-Level Low Power Testing

Part 2

9. Overview of Low Power Design Techniques
10. Test Strategies for Low Power Devices
11. EDA Tools for Power-Aware Design-for-Test
12. Summary and Conclusions

Part 3

1. Introduction

Part 1

Chapter 1

Introduction

1. Introduction

Power dissipation in the test mode is much higher than during functional operations

[ITC 2003] : Texas Inst. & Siemens AG
ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM

Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%

[EEDesign 2004] : Synopsys Inc.
Power under test mode 2-3X more than during functional mode

And many other reported industrial experiences …

1. Introduction

Power dissipation in the test mode is much higher than during functional operations

- High switching activity of test operations (e.g. scan)
- No correlation between consecutive test vectors
- Test vectors ignoring functional constraints
- DFT circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction
- Low power functional features (e.g. clock gating) often disabled during test application

1. Introduction

Industry generally resorts to ad-hoc solutions for reducing test power

- Over sizing power rails
- Over sizing packages and use of cooling systems
- Test with reduced operation frequency
- Partitioning and appropriate test planning

Costly or longer test time

1. Introduction

~ Test in the Past ~

High Fault Coverage
Short Test Time
Small Test Data Volume
Low Test Development Efforts
Low Area Overhead

~ Test from Now ~

•
•
•
+

Low Test Power
(low average and peak power)

Make test power dissipation comparable to functional power

2. Test Power Metrics

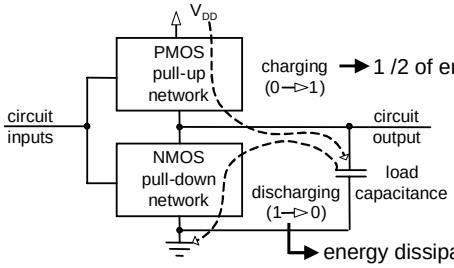
Chapter 2

Test Power Metrics

2. Test Power Metrics

2.1 Power Dissipation in CMOS ICs

- Dynamic Short-Circuit Power
  - Due to direct current path from V_{DD} to Gnd during output switching
  - $P_{SC} = V_{DD}. I_{SC}$ with $I_{SC} \propto$ input_slew / C_{load}
- Dynamic Switching Power
  - Due to charge/discharge of load capacitance during switching



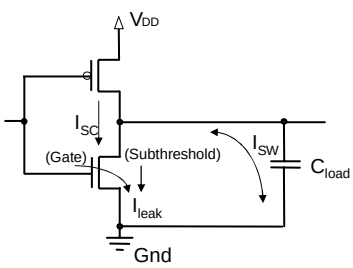
$P_{sw} = C_L.V_{dd}^2.N_{0\to1}.1/T$

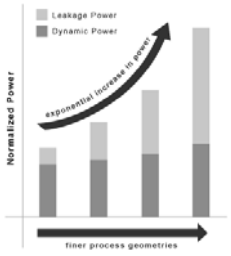
$P_{sw} = ½.C_L.V_{dd}^2.N.1/T$

2. Test Power Metrics

2.1 Power Dissipation in CMOS ICs

- Static Leakage Power
  - Power consumed when the circuit is idle
  - Due to four components of leakage current
  - Mainly due to subthreshold leakage from V_{DD} to Gnd
  - $P_{leak} = V_{DD}. I_{leak}$ and $I_{SUB} \propto V_{DD}$ / Vth

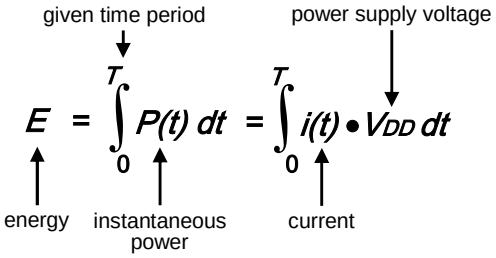




2. Test Power Metrics

2.1 Power Dissipation in CMOS ICs

- Energy:



- Average Power: $\frac{E}{T} = \frac{V_{DD}}{T}\int_0^T i(t)\,dt$
- Peak Power: Maximum instantaneous power in any given clock cycle

2. Test Power Metrics

2.2 Test Power Metrics

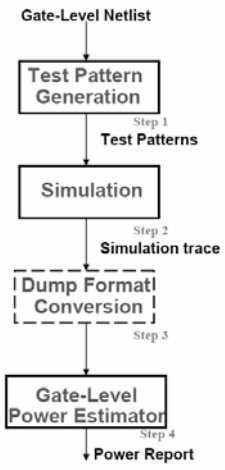
- Energy:
  - Total switching activity generated during test application
  - $E_{Total} = ½ \,.\, c_0.V^2_{DD} \,.\, \sum_k \sum_i s_i(k) \,.\, F_i$
  - $s_i(k)$ is the number of transitions provoked by V_k at node i
  - Impact the battery lifetime during power up or periodic self-test of battery operated devices
- Average Power:
  - Ratio between energy dissipated during test and test time
  - $P_{Average} = E_{Total} / (Length_{Test} \,.\, T)$
  - Impact the thermal load of the device

2.2 Test Power Metrics

- Instantaneous Power:
  - Power consumed at any given instant during test
- Peak Power:
  - Highest value of instantaneous power measured during test
  - $P_{Peak} = max_k\ P_{inst}(V_k) = max_k\ (E_{Vk} / t_{small})$
  - Determines the thermal and electrical limits of components and the system packaging requirements
- Weighted Switching Activity (WSA):
  - $WSA_i = F_i \cdot S_i$ where F_i is the fanout at node i and S_i is the switching activity factor (ave. # of transitions during a time interval)
  - Often used as a metric for test power evaluation

2.3 Test Power Estimation Flow

- Conventional flow adopted to perform test power estimation is simulation-based
  - Performed at gate level
- For average test power consumption, shift power due to a scanout operation is calculated
  - The time interval of interest can be specified as an input in Steps 1/2/3
- Estimation is performed at various PVT corners
- Challenges for multi-million gate SoCs
  - Time-consuming (5.5 hours)
  - Dump sizes can be very large (15GB for ~150 cycle scanout operation)
- Vectorless gate-level test power estimation
  - Significant speedup for a full-chip SoC (10X)



(source: S. Ravi, TI, ITC07)

Chapter 3

Test Power Issues

3.1 Overview of Thermal and Noise Effects

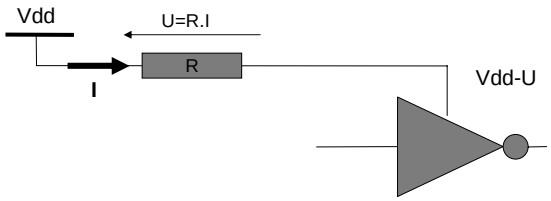
- Heat produced during the operation of a circuit is proportional to the dissipated power (Joule effect) and is responsible for die temperature increase
  - $T_{die} = T_{air} + \theta \times P_{Average}$ where θ is the package thermal impedance

- Too high temperature may lead to reliability issue and test throughput problem.

3. Test Power Issues

3.1 Overview of Thermal and Noise Effects

- IR Drop refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a non negligible resistance between the rail and each node in the circuit under test

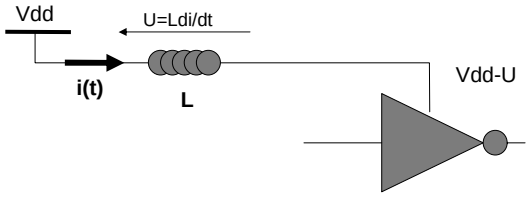


- With high peak current demands, gate voltages are reduced and gate delays increase.
- IR Drop may lead to manufacturing yield loss.

3. Test Power Issues

3.1 Overview of Thermal and Noise Effects

- Power supply noise L(di/dt) due to current variations (during switching) through inductive connections (probes for wafer testing, pins for packaged circuits)

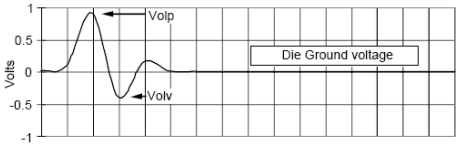


- The level and change rate of current are the two main sources of power supply noise.
- May lead to manufacturing yield loss (like IR drop).

3. Test Power Issues

3.1 Overview of Thermal and Noise Effects

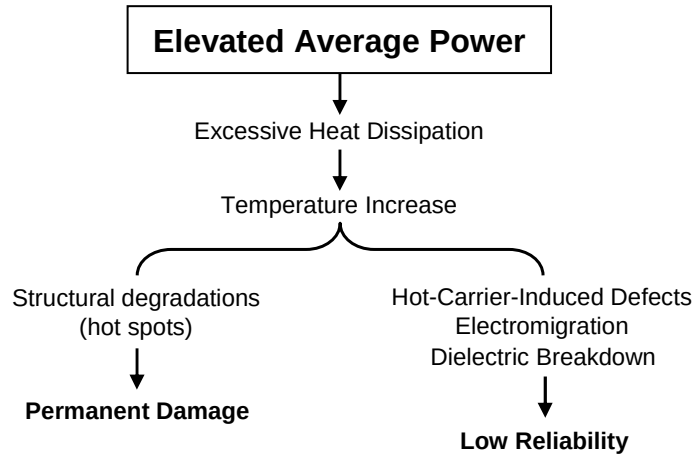
- Ground Bounce is a comparable inductive phenomena (although less significant compared to IR drop and Ldi/dt)
- Wire/substrate inductances or package lead inductances are associated with power or ground rails in DSM circuits
- With high switching currents occurring in the circuit, voltage glitches can be observed at the nodes of these inductances.



- They may change the rise/fall times of some signals in the circuit.
- They can also erroneously change the logic state of some circuit nodes or flip-flops, and cause test fail, thus leading to yield loss.

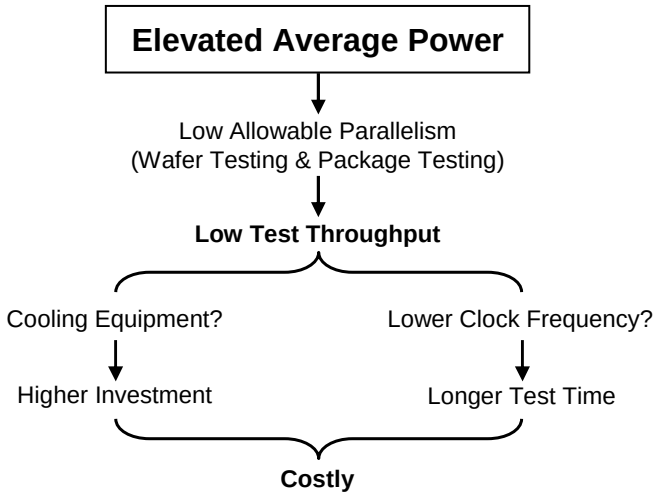
3. Test Power Issues

3.2 Reliability Issue



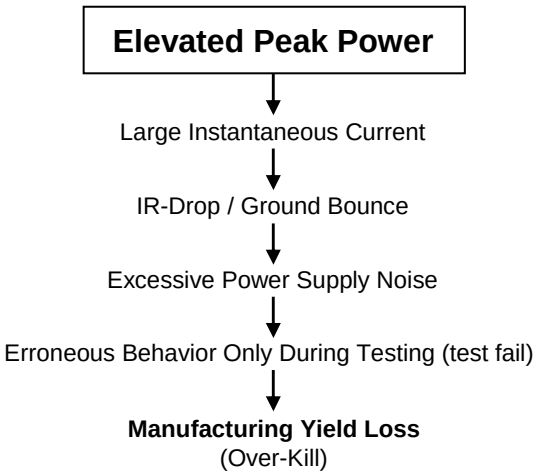
3. Test Power Issues

3.3 Test Throughput Problem



3. Test Power Issues

3.4 Manufacturing Yield Loss



Chapter 4

Test Application Environments

Overview

~ From Where ~

External or Stored Pattern Test
(Applied from ATE which stores the test patterns generated by ATPG)

Built-In Self-Test (BIST)
(Applied from on-chip circuitry that generates test patterns on-the-fly)

~ How Frequently ~

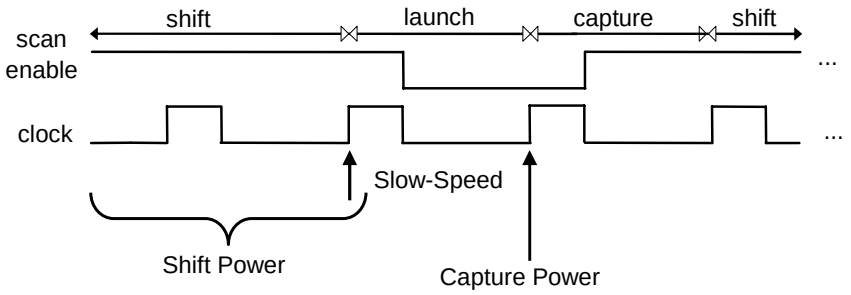
Test-Per-Clock
(Test patterns are applied consecutively in every clock cycle)

Test-Per-Scan
(Test Patterns are applied consecutively in every scan cycle)

w.r.t. a series of clock cycles

4. Test Application Environments

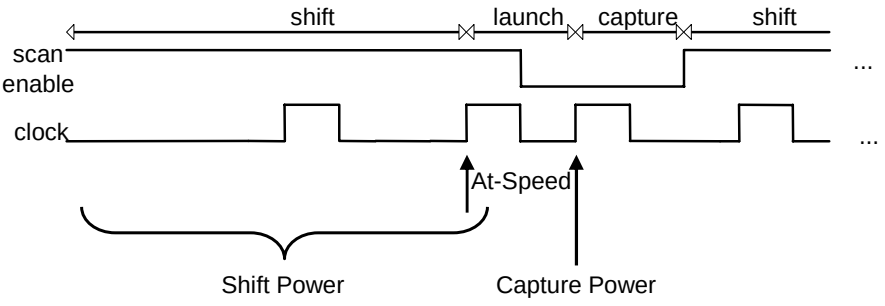
4.1 Conventional Scan Testing



- Conventional scan testing was performed at slow speed
- Low coverage of timing defects

4. Test Application Environments

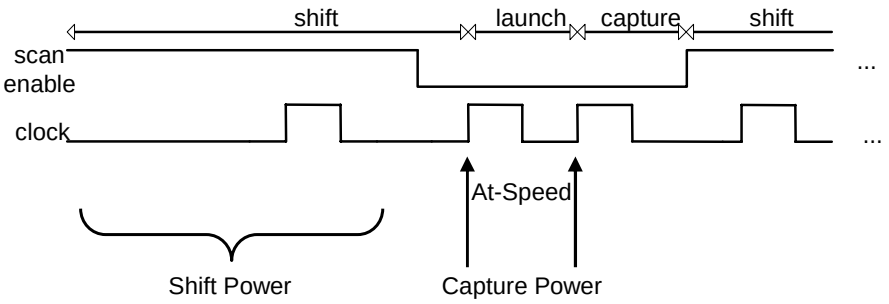
4.2 At-Speed Scan Testing
~ Launch-Off-Shift (LOS) ~



- Launch is caused by the difference between the values loaded by the next-to-last and the last shift pulses.
- High fault coverage can be achieved with a smaller ATPG model.

4. Test Application Environments

4.2 At-Speed Scan Testing
~ Launch-Off-Capture (LOC) ~



- Launch is caused by the difference between the values loaded by the last shift pulse and the first capture pulse.
- Easy to implement the scan enable signal.

4. Test Application Environments

4.2 At-Speed Scan Testing

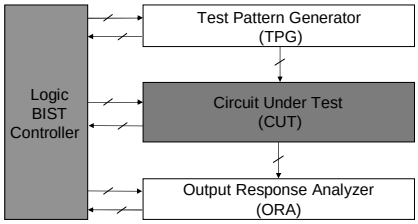
- The problem of excessive power during scan testing can be split into two sub-problems: excessive power during the shift operation (called shift power) and excessive power during the capture operation (called capture power)
- At-speed scan testing especially vulnerable to excessive IR drop and L(di/dt) noise caused by the high switching activity generated in the CUT between launch and capture → yield loss *

* (see T.M. Mak, Intel, IEEE Design & Test of Computers, Vol. 24, No. 3, p. 296, May-June 2007)

4. Test Application Environments

4.3 Logic BIST

~ Test-per-Clock ~

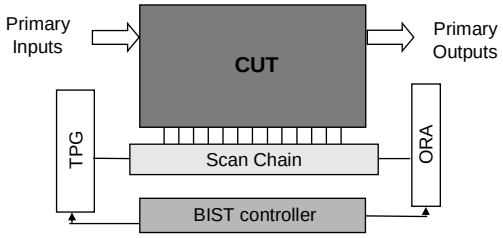


- A test pattern generator (TPG) automatically generates test patterns for application to the inputs of the circuit under test (CUT).
- In-circuit TPG and output response analyzer (ORA) are generally constructed from LFSRs.
- Test patterns are applied every clock cycle from the TPG.

4. Test Application Environments

4.3 Logic BIST

~ Test-per-Scan ~



- Pseudo-random patterns are first shifted into the scan chain (s).
- Capture test responses are shifted out to the ORA.
- Even if slower, test-per-scan is the industry preferred solution today.

Part 2

Chapter 5

Low Power Test Pattern Based Approaches

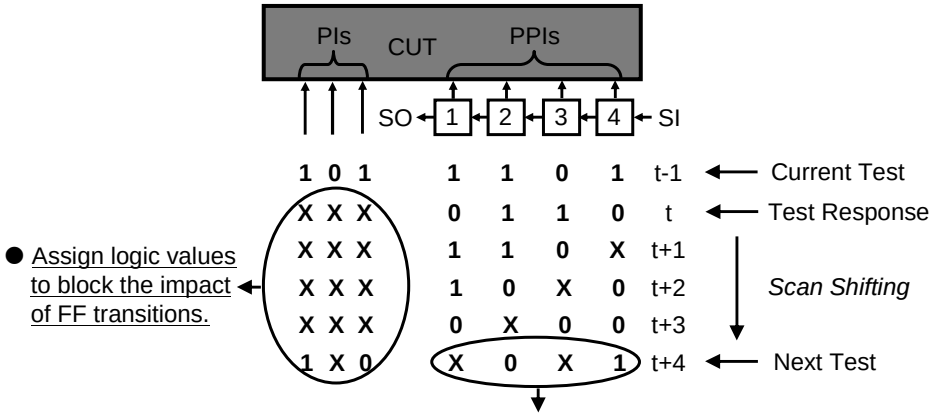
Overview

Scan Testing	Shift Power Reduction	Capture Power Reduction
ATPG	• **Blocking Test Generation** • **Low Power Compaction**	• **Test Generation** *- power constraint checking* *- target fault restriction*
X-Filling	• **X-Filling** *- 0-fill* *- 1-fill* *- adjacent-fill*	• **FF-Oriented X-Filling** *- justification-based* *- probability-based* *- hybrid* • **Node-Oriented X-Filling** *- internal-switching-activity-aware* *- critical-path-aware*
LFSR-Based Low Power Test Generation		
Low Power Memory Test Generation		

5. Low Power Test Pattern Based Approaches

5.1 Low Power ATPG Algorithms

~ Shift Power Reduction ~



- Use modified PODEM to maximize the # of Xs.
- Assign logic values to minimize FF transitions.

(based on S. Wang et. al., Proc. DAC, pp. 614-619, 1997)

5. Low Power Test Pattern Based Approaches

5.1 Low Power ATPG Algorithms

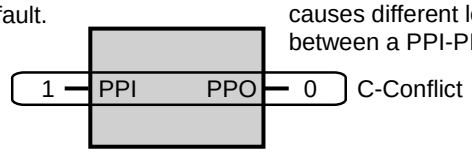
~ Capture Power Reduction ~

D-Conflict

The current input assignment cannot detect the target fault.

C-Conflict

The current input assignment causes different logic values between a PPI-PPO pair.



D-Conflict → Normal Backtrack
C-Conflict → Reversible Backtrack
(Backtrack decision is reversed if it makes a fault undetected.)

- Advantages: High reduction effect due to full search space exploration. (10% higher than reduction by X-filling for ISCAS'89 circuits)
- Disadvantages: Longer CPU time and larger test vector count.

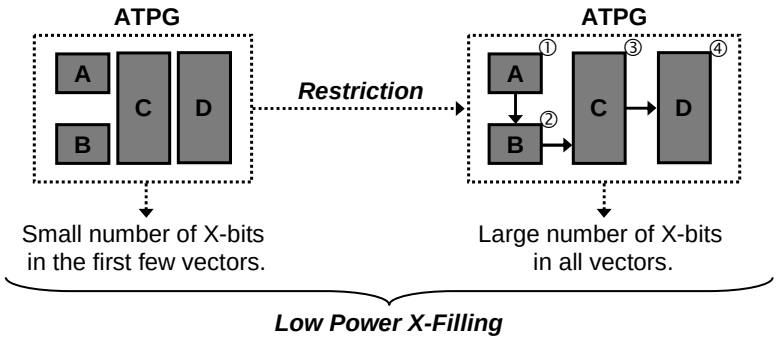
(based on X. Wen et. al., Proc. VTS, pp. 251-258, 2006)

5. Low Power Test Pattern Based Approaches

5.1 Low Power ATPG Algorithms

~ Capture Power Reduction ~

(Target Fault Restriction)



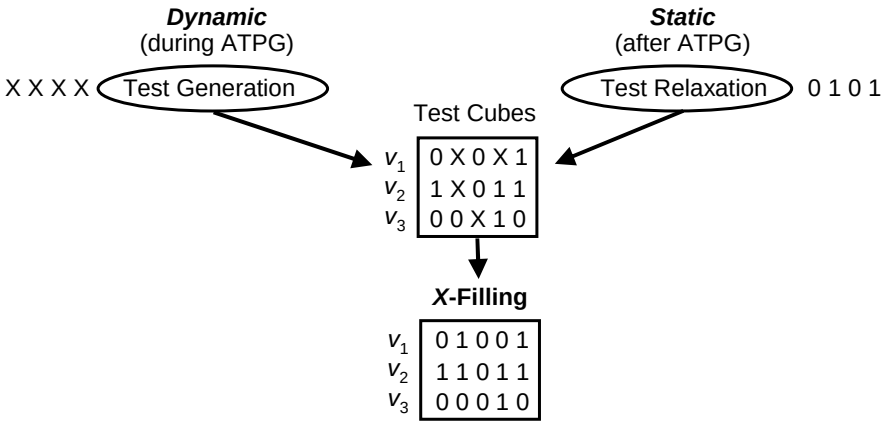
- Advantage: Immediately doable with any existing ATPG tool.
- Disadvantage: larger test vector count.

(based on N. Ahmed et. al., Proc. DAC, pp. 533-538, 2007)

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling

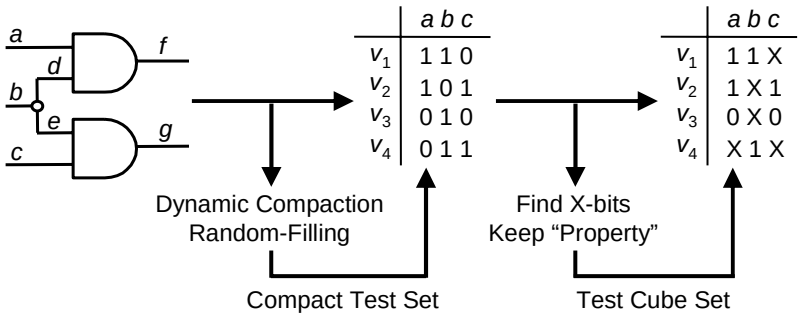
~ Basic Approaches ~



- X-bits are filled to reduce switching activity in capture mode.
- "Static" leads to a smaller test size since it allows full dynamic compaction.

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling
~ Test Relaxation ~

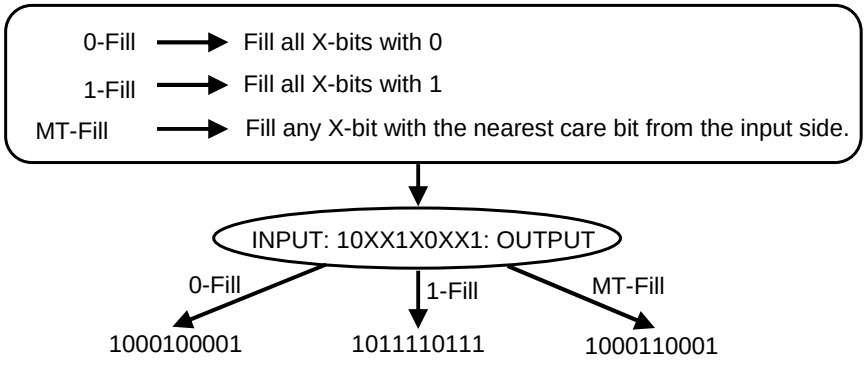


- "Property" is usually the fault coverage for various fault models.
- Fault simulation, justification, and implication are used to find X-bits.
- 60%-80% of bits in a test set are usually identified as X-bits.

(based on K. Miyase et. al., IEEE Trans. On CAD, Vol. 23, No. 2, pp. 321-326, 2004)

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling
~ Shift Power Reduction ~



- All can only reduce (vector) shift-in power but not (response) shift-out power.
- 0-fill can also reduce capture power for AND/NAND-dominant circuits.

(based on K. M. Butler et. al., Proc. ITC, pp. 355-364, 2004)

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling

~ Impact of Shift Power Reduction Techniques on Capture Power ~

Circuit	Test Vec. #	Fault Cov. (%)	Initial Max. WCT	*X* (%)	Max. WCT Reduction Ratio (%)					
					Ran.	*0-Fill*	*1-Fill*	*MT*	*Jus.*	*Est.*
s13207	236	98.5	5238	91.4	10.2	19.8	0.4	12.4	21.7	33.7
s15850	94	96.7	4438	77.3	1.6	20.6	-15.4	4.8	20.7	36.3
s35932	13	89.8	17804	41.2	8.1	9.2	-0.8	-0.8	9.2	12.2
s38417	87	99.5	14183	76.8	2.8	12.4	4.4	12.9	15.7	24.7
s38584	118	95.9	14324	82.0	3.9	25.8	21.9	3.2	35.0	34.1
Ave.				73.7	5.3	17.6	2.1	6.5	20.1	**28.2**

Shift Power Reduction ***Capture Power Reduction***

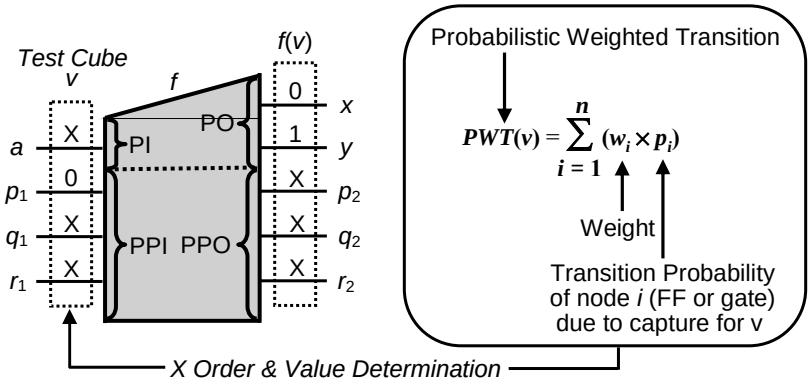
- The 0-fill technique can also reduce capture power to some extent.
- Capture power reduction techniques need to be used for better effects.

(based on X. Wen et. al., Proc. ICCD, pp. 251-258, 2006)

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling

~ Estimation-Based X-Filling for Capture Power Reduction ~



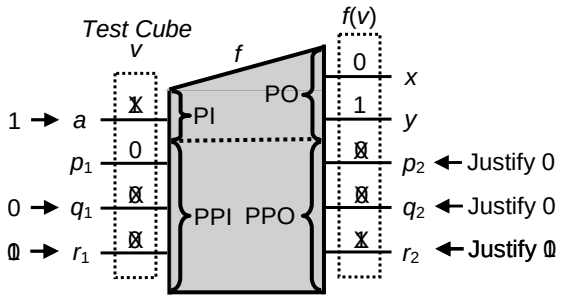
- Various switching activity metrics can be used as guidance, so that the whole circuit or some critical areas can be targeted.
- X-bits are filled to reduce switching activity in capture mode.

(based on X. Wen et. al., Proc. ICCD, pp. 251-258, 2006)

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling

~ Justification-Based X-Filling for Capture Power Reduction ~



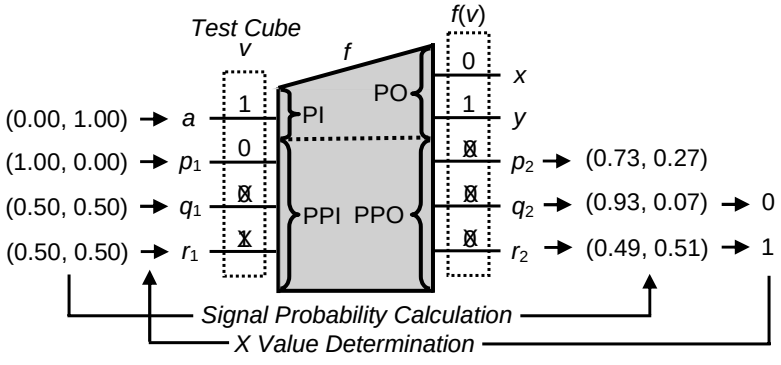
- Highly effective due to the use of deterministic ATPG techniques.
- Relatively long CPU time due to multi-pass processing.

(based on X. Wen et. al., Proc. VTS, pp. 265-270, 2005)

5. Low Power Test Pattern Based Approaches

5.2 Power-Aware X-Filling

~ Probability-Based X-Filling for Capture Power Reduction ~



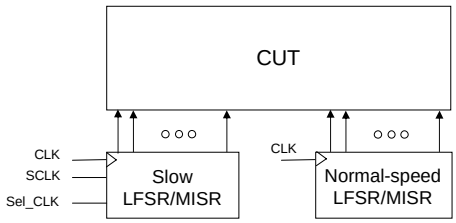
- Relatively short CPU time due to single-pass processing.
- Effectiveness depends on the accuracy of probability calculation.

(based on S. Remersaro et. al., Proc. ITC, Paper. 32-2, 2006)

5. Low Power Test Pattern Based Approaches

5.3 Low Power LFSR-Based Generation

~ Dual-Speed LFSR ~



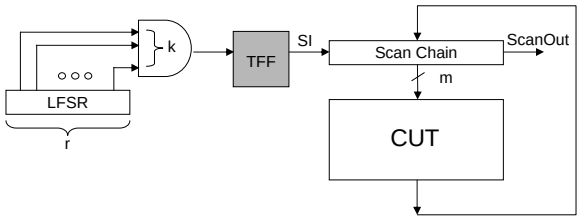
- Based on two LFSRs running at different frequencies.
- Average power during test is reduced by connecting the CUT inputs with the highest transition densities to the low speed LFSR while CUT inputs with the lowest activity are connected to the normal speed LFSR.

(based on S. Wang et. al., Proc. ITC, pp. 848-857, 1997)

5. Low Power Test Pattern Based Approaches

5.3 Low Power LFSR-Based Generation

~ Low Transition Random TPG ~



- Low transition random test pattern generator involves inserting an AND gate and a toggle flip-flop (TFF) between the LFSR and the input of the scan chain to increase the correlation of neighboring bits in scan vectors
- TFF holds its previous values until it receives a 1 on its input. The same value (0 or 1) is repeatedly scanned into the scan chain until the value at the output of the AND gate becomes 1

(based on S. Wang et. al., Proc. ITC, pp. 85-94, 1999)

5. Low Power Test Pattern Based Approaches

5.4 Low Power Test Vector Compaction

- Static compaction minimizes the number of test cubes generated by an ATPG tool by merging test cubes that are compatible in all bit positions

  Example 1: 11XX0 and 1X0X0 are compatible (→ 110X0)
  Example 2: 11XX0 and 011X1 are not compatible

- Conventional approaches target the minimum number of final test cubes
- A solution is to use a greedy heuristic for merging test cubes in a way that minimizes the number of transitions (use of weighted transition metric)

● Significant reductions in average and peak power consumption.

(based on R. Sankaralingam et. al., Proc. VTS, pp. 35-42, 2000)

5. Low Power Test Pattern Based Approaches

5.4 Low Power Memory Test Algorithms

- Motivated by the need to concurrently test several banks of memories in a system to reduce test time
- Reorder memory tests to reduce the switching activity on each address line while retaining the fault coverage and the test time

	Original Test	**Low-power Test**
Zero-One	↕ (W0); ↕ (R0); ↕ (W1); ↕ (R1);	$\updownarrow_s$ (W0, R0, W1, R1);
Checker Board	↕ ($W(1_{odd}/0_{even})$); ↕($R(1_{odd}/0_{even})$); ↕($W(0_{odd}/1_{even})$); ↕($R(0_{odd}/1_{even})$);	$\updownarrow_s$ ($W(1_{odd}/0_{even})$, $R(1_{odd}/0_{even})$, $W(0_{odd}/1_{even})$, $R(0_{odd}/1_{even})$);

Single bit change (SBC) counting

● Power dissipation reduced by a factor of two to sixteen.
● Special design of the BIST circuitry is needed.

(based on H. Cheung et. al., Proc. ITC, pp. 22-32, 1996)

Chapter 6

Low Power Design-for-Test

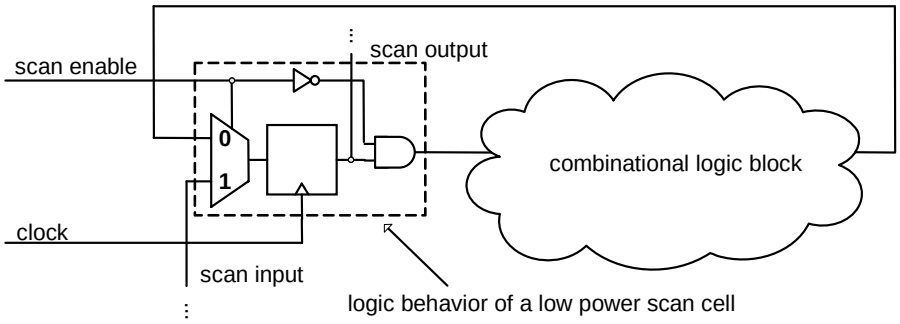
Overview

- Active research area for more than one decade
  - Scan cell modifications
  - Scan chain reordering
  - Scan chain modification
  - Scan chain segmentation
  - Staggered clocking
  - Masking logic insertion
  - Circuit partitioning
  - Low power DFT memories

6. Low Power Design-for-Test

6.1 Gated Scan Cells

~ Suppress Combinational Logic Activity During Shift ~

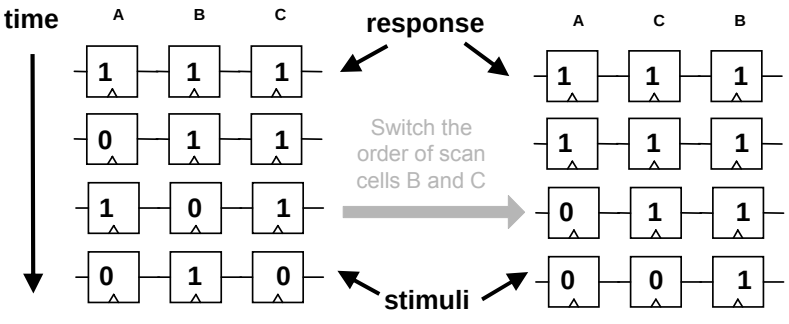


- Various ways of implementing the blocking logic (muxes, transmission gates, …).
- May affect circuit performance in the native mode.
- Addresses only shift power in the combinational logic block.

(based on S. Gerstendorfer et. al., Proc. ITC, Paper. pp. 77-84, 1999)

6. Low Power Design-for-Test

6.2 Scan Cell Reordering

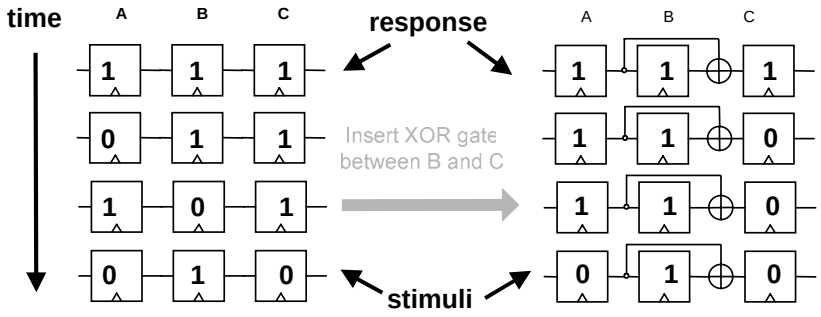


- Scan cell reordering can be combined with vector reordering.
- NP-complete – concerns with scaling.
- Physical design constraints can be included in the reordering algorithm.

(based on S. Dabholkar et. al., IEEE Trans. On CAD, Vol. 17, No. 2, pp. 1325-1333, 1998)

6. Low Power Design-for-Test

6.3 Logic Insertion in Scan Chain



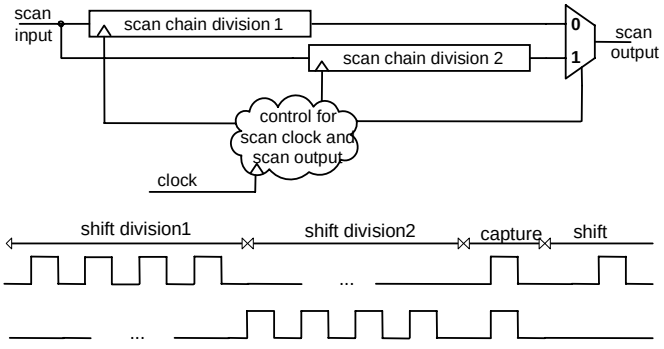
- Addresses only shift power (in both combinational logic and scan path).
- Scan path built based on the test set at hand (problems with top-off patterns).
- Computational demand increases with number of scan cells and pattern count.

(based on S. Sinanoglu et. al., IEEE Trans. On Reliability, Vol. 54, No. 2, pp. 215-223, 2005)

6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

~ Pattern Independent ~



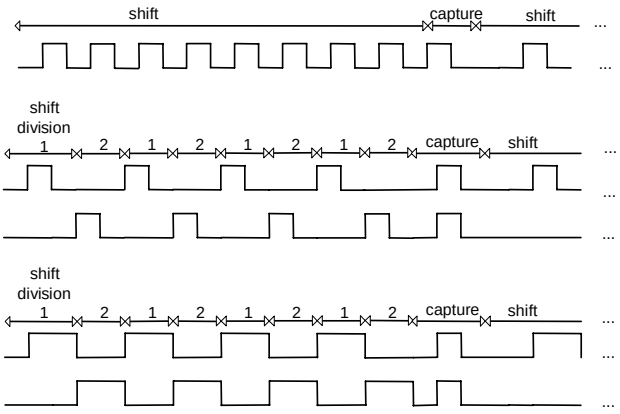
- Not all the scan cells receive the test clock edge at the same time.
- Reducing shift power in scan path, combinational logic and test clock tree.

(based on L. Whetsel Proc. ITC, pp. 863-872, 2000)

6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

~ Variations in Clocking ~

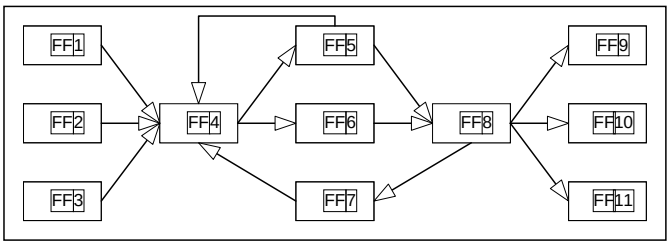


- Capture power remains a concern that needs to be addressed.

6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

~ Addressing Capture Power ~



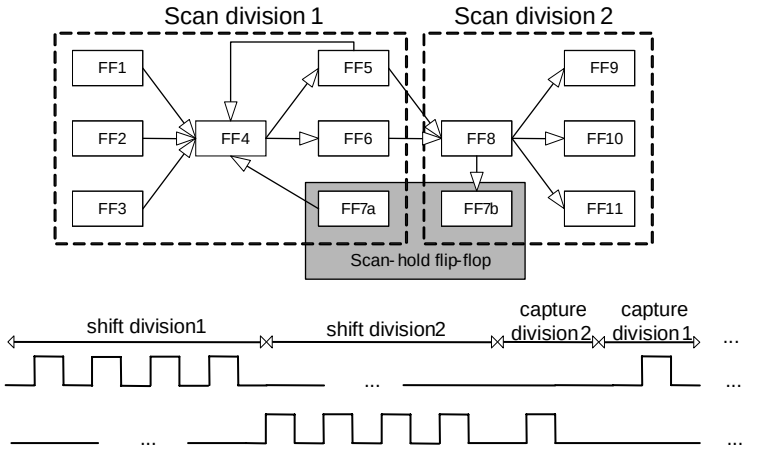
- Create a data dependency graph based on circuit structure.
- Identify the strongly connected components (SCC).
- FFs in an SCC must load responses at the same time to avoid capture violations.

(based on P. Rosinger et. al, IEEE Trans on CAD, Vol. 23, No. 7, pp. 1142-1153 , 2004)

6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

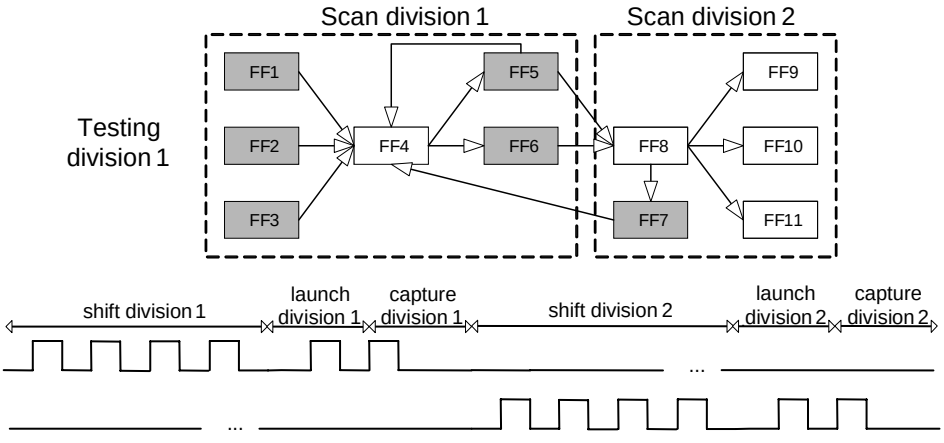
~ Balancing Partitions ~



6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

~ Launch-Off-Shift ~

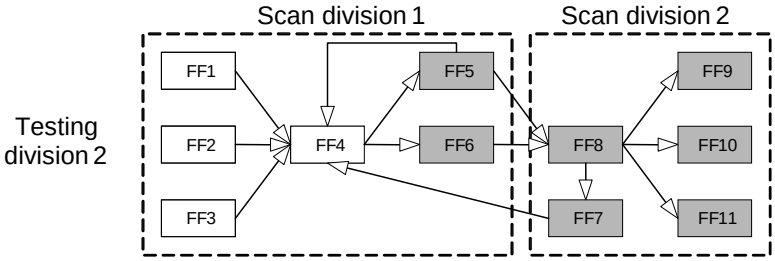


(based on H. Ko et. al., Proc. ICCD, paper 5.3.2, 2006)

6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

~ Launch-Off-Shift ~

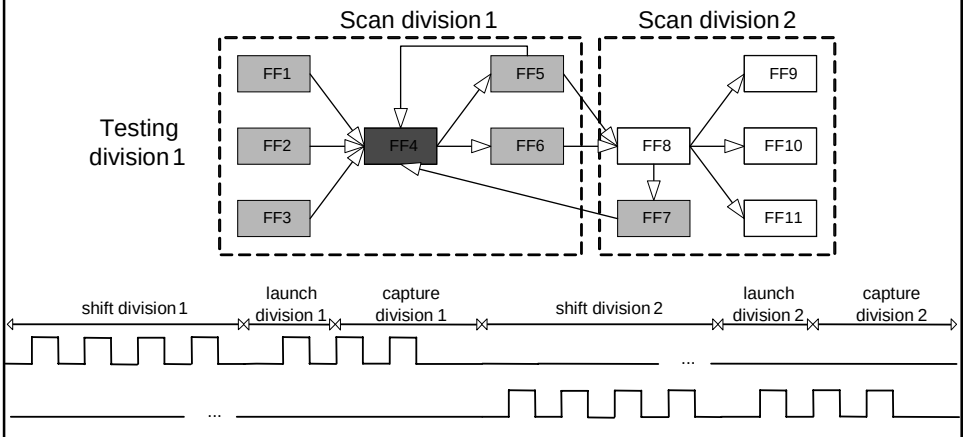


- All the scan cells that drive the FFs in one division are controlled during shift.
- The partitioning objective is to reduce the number of FFs active for multiple divisions.
- Problem is intractable in the general case, yet solvable for few partitions.

6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

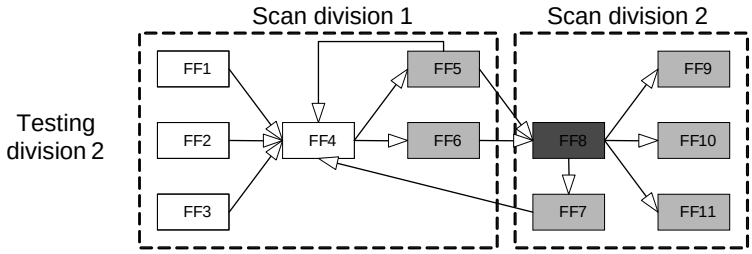
~ Launch-Off-Capture ~



6. Low Power Design-for-Test

6.4 Scan Chain Segmentation

~ Launch-Off-Capture ~

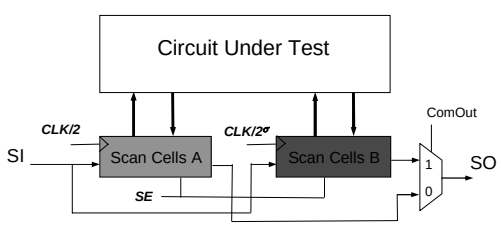


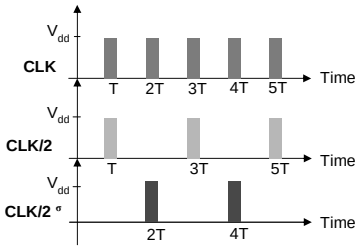
- Fault coverage for transition delay faults can be improved.
- Some FFs can be identified as non-scan .
- Pattern count increases / scan time can be reduced due to shorter scan cycles.

6. Low Power Design-for-Test

6.5 Staggered Clocking

~ Scan Clock Splitting ~





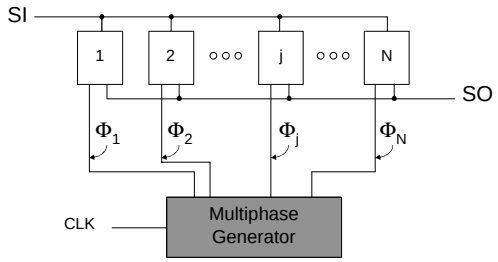
- The two clocks are synchronous with the system clock and have the same period during shift operation except that they are shifted in time.
- During capture operation, the two clocks operate as the system clock.
- Lowers the transition density in the CUT, the scan chains and the clock tree.

(based on Y. Bonhomme et. al., Proc. ATS, pp. 253-258, 2001)

6. Low Power Design-for-Test

6.5 Staggered Clocking

~ Token Scan Architecture ~



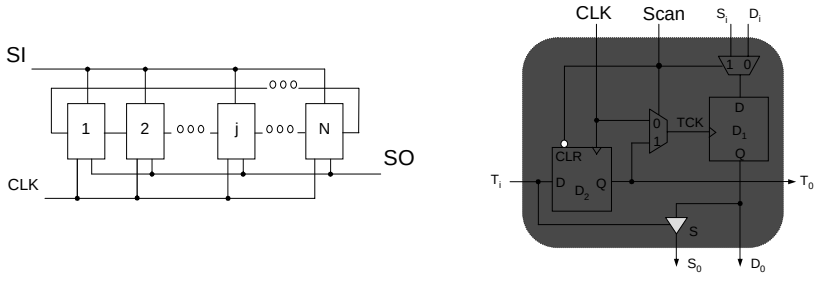
Scan architecture that uses the concept of a “token ring” to reduce shift power.
SI is broadcasted to all scan cells but only one scan cell is activated at a time.
An N-phase non-overlapping clocking scheme is applied with one clock for each scan cell.

(based on T.-C. Huang et. al., Proc. ITC, pp. 660-669, 2001)

6. Low Power Design-for-Test

6.5 Staggered Clocking

~ Token Scan Architecture ~



Alternative solution to avoid large area overhead of the N multiphase clock routes and inter-phase skews due to the different lengths of the N clock routes.
It embeds the multiphase clock generator into each scan cell.
Require the use of a new type of scan cells, called token scan cells.

6. Low Power Design-for-Test

6.6 Masking Logic Insertion

~ Parallel BIST ~

Prevent application of non-detecting (but consuming) vectors to the CUT. A decoder is used to store the first and last vectors of each sub-sequence of consecutive non-detecting vectors to be filtered.

● Minimizes average power without reducing fault coverage.

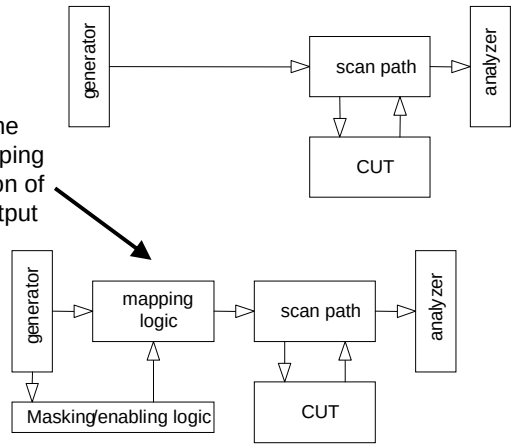
(based on P. Girard et. al., Proc. VTS, pp. 407-412, 1999)

6. Low Power Design-for-Test

6.6 Masking Logic Insertion

~ Scan-Based BIST ~

Masking/enabling logic filters the non-essential vectors and mapping logic can improve the correlation of the values on the generator output

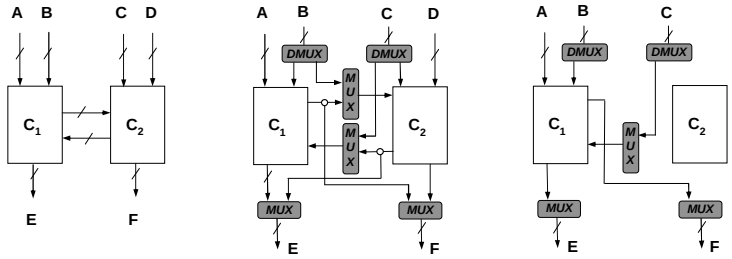


(based on F. Corno et. al., Proc. DFT, pp. 219-226, 1999)

6. Low Power Design-for-Test

6.7 Circuit Partitioning

~ Scan-Based or Parallel BIST ~



Partition the original circuit (using a graph partitioning algorithm that minimizes the cut size) into structural sub-circuits so each sub-circuit can be successively tested through different BIST sessions

- FC and test time are unchanged and area overhead is quite low.
- Drawbacks are a slight penalty on performance and an impact on routing.

(based on P. Girard et. al., Proc. ITC, pp. 652-661, 2000)

6. Low Power Design-for-Test

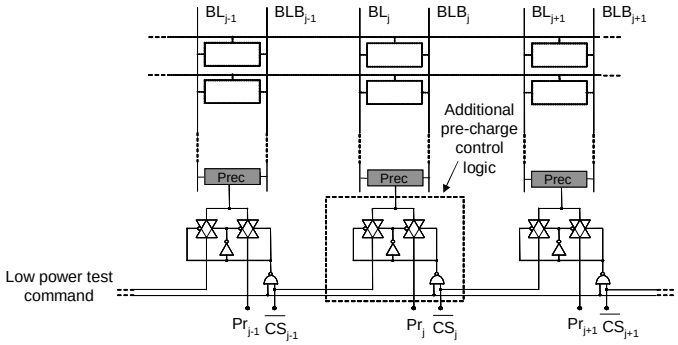
6.8 Low Power DfT for Memories

- Exploit the predictability of the addressing sequence to reduce the pre-charge activity during test
- Pre-charge circuits contribute to up to 70% to power dissipation
- In functional mode, the cells are selected in random sequence, and all pre-charge circuits need to be always active, while during the test mode the access sequence is known, and hence only the columns that are to be selected need to be pre-charged
- This low-power test mode can be implemented by using a modified pre-charge control circuitry, and by exploiting the first degree of freedom of March tests, which allows choosing a specific addressing sequence

(based on L. Dilillo et. al., Proc. DATE, pp. 1159-1165, 2006)

6. Low Power Design-for-Test

6.8 Low Power DfT for Memories



Addressing sequence is fixed to “word line after word line” and the pre-charge activity is restricted to only two columns for each clock cycle: the selected column and the following one

- 50% power savings with negligible impact on area overhead and memory performance

7. Low Power Test Data Compression

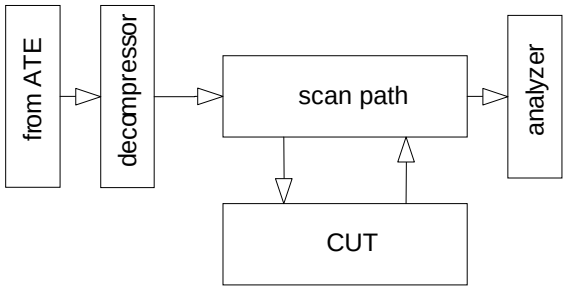
Chapter 7

Low Power Test Data Compression

7. Low Power Test Data Compression

Overview

~ Motivation ~



- Large volume of test data raise the cost of ATEs (memory/bandwidth)
- On-chip decompressor used to inflate test data received from ATE
- Low power test data compression – can reduce memory/scan time

7. Low Power Test Data Compression

7.1 Coding-Based Schemes

~ Golomb Coding ~

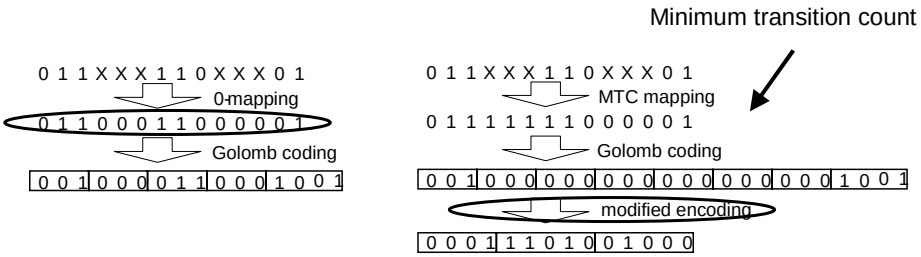
- Use of 0-filling on ATPG test cubes and then encode runs of 0's with Golomb codes (run-length codes) for reducing the number of transitions (75%)
- Golomb coding is very inefficient for runs of 1's
- A synchronization signal between the ATE and the CUT is required as the size of the compressed data (codeword) is of variable length
- Alternating run-length coding improves the encoding efficiency of Golomb coding (can encode both runs of 0's and runs of 1's)
- Other coding schemes have been investigated, such as Huffman

(based on A. Chandra et. al., Proc. DAC, pp. 166-169, 2001 and pp. 673-678, 2002)

7. Low Power Test Data Compression

7.1 Coding-Based Schemes

~ Golomb Coding ~



● Addresses only the scan-in component of shift power.

(based on P. Rosinger et. al, IEE Electronic Letters, Vol. 37, No. 24, pp. 1434-1436 , 2001)

7. Low Power Test Data Compression

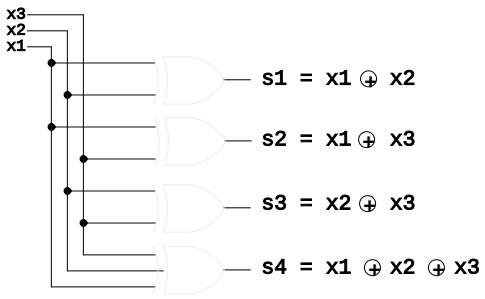
7.2 Linear-Decompression-Based Schemes

~ Basic Principles of Linear Decompression~

- Linear Decompressors (LD) consist of XORs and flip-flops
- In LFSR reseeding
  - Deterministic test cubes generated by expanding seeds
  - Typically 1-5% of bits in test vector specified
  - Most bits need not be considered when seed computed
  - Size of seed much smaller than size of vector
  - Significantly reduces test data volume and bandwidth
- Problem: X's in test cubes filled randomly
  - Results in excessive switching during scan shifting

7.2 Linear-Decompression-Based Schemes

~ Encoding Example Using GF(2) Arithmetic ~



$$\begin{pmatrix} s1 \\ s2 \\ s3 \\ s4 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} x1 \\ x2 \\ x3 \end{pmatrix}$$

$$\Downarrow$$

$$\begin{pmatrix} 1 \\ x \\ x \\ 0 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} x1 \\ x2 \\ x3 \end{pmatrix}$$

$$\Downarrow$$

$$\begin{pmatrix} x1 \\ x2 \\ x3 \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 1 \end{pmatrix} \text{ or } \begin{pmatrix} 0 \\ 1 \\ 1 \end{pmatrix}$$

7. Low Power Test Data Compression

7.2 Linear-Decompression-Based Schemes

~ Combining LFSR Encoding and Repeat/0/1 Fill ~

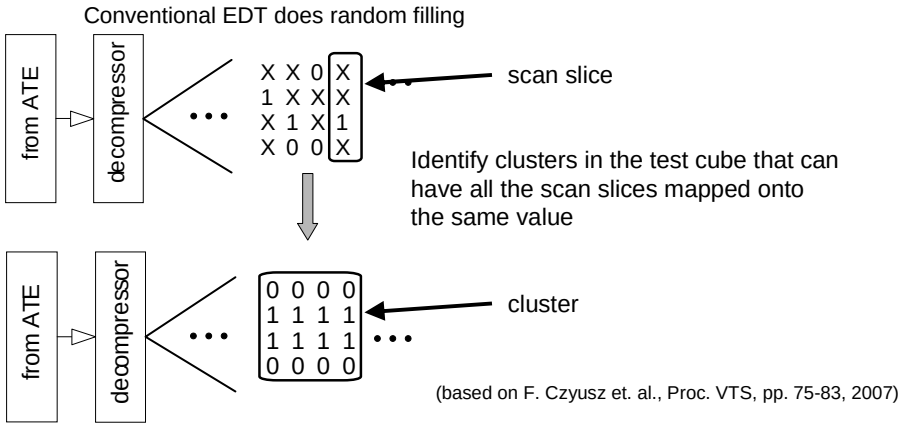
- Low power linear decompression using LFSR reseeding can be used
- LFSR reseeding not used to directly encode specified bits
  - Each test cube divided into blocks
  - LFSR reseeding used only to produce blocks containing transitions
  - For blocks not containing transitions
    - ➢ Logic value fed into scan chain simply held constant
- Reduces number of transitions in scan chain
- Efficient trade-off between test data compression and power reduction

(based on J. Lee et. al., Proc. ICCD, pp. 180-185, 2004)

7. Low Power Test Data Compression

7.2 Linear-Decompression-Based Schemes

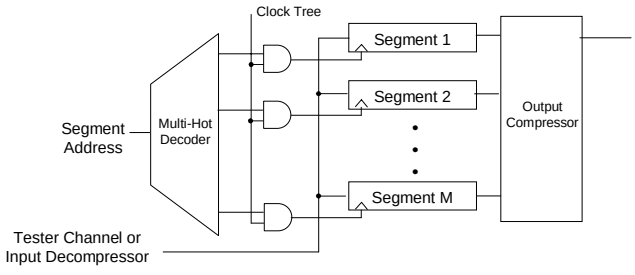
~ Self-Loop States in Ring Generators ~



7. Low Power Test Data Compression

7.3 Broadcast-Scan-Based Schemes

~ Segment Addressable Scan ~



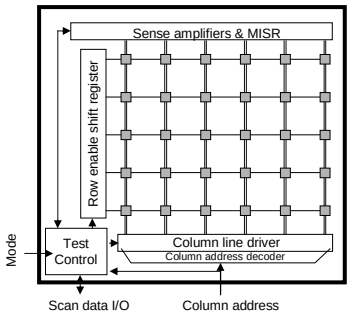
- Based on broadcasting the same value to multiple scan segments
- Test power is reduced as segments which are incompatible during the time needed to upload a given test pattern are not clocked

(based on A. Al-Yamani et. al., Proc. VTS, pp. 405-411, 2005)

7. Low Power Test Data Compression

7.3 Broadcast-Scan-Based Schemes

~ Progressive Random Access Scan ~



- Scan cells are configured as an SRAM-like structure using PRAS scan cells
- PRAS allows individual accessibility to each scan cell, thus eliminating unnecessary switching activity during scan, while reducing the test application time and test data volume by updating only a small fraction of scan-cells

(based on D.H. Baik et. al., Proc. ITC, paper 15.2, 2005)

Chapter 8

System-Level Low Power Testing

Overview

~ Motivation for System Level Solutions ~

- ATPG/DFT/compression test approaches to low power can be combined with system-level solutions to improve test concurrency under power constraints.

- System-level solutions create a test infrastructure and a test plan that schedules tests for different blocks at mutually exclusive times to avoid excessive power.

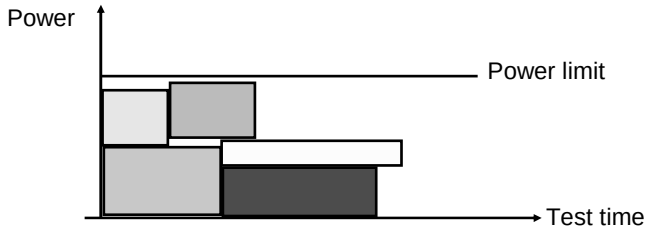
- Main additional advantages of system-level solutions:
  - Improve test throughput and power delivery during wafer probing.
  - Simplify the design of power/ground distribution networks.

- System-level solutions exploit modularity and design hierarchy.

8. System-Level Low Power Testing

8.1 Power-Constrained Test Scheduling

~ Sequence Tests to Meet Power Limits ~



● The goal is to determine the blocks (memory, logic, analog, etc.) of an SOC to be tested in parallel at each stage of the BIST session in order to keep power dissipation under a specified limit while optimizing test time
● Some of the test resources (pattern generators and response analyzers) must be shared among the various blocks

(based on Y. Zorian, Proc. VTS pp. 4-9, 1993)

8. System-Level Low Power Testing

8.1 Power-Constrained Test Scheduling

~ Problem Definition and Computational Complexity ~

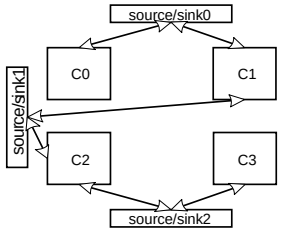
● For given power constraints and parameters related to the test organization (fixed, variable, or undefined test sessions with or without precedence constraints) or to the test structure (test bus width, test resources sharing), these solutions allow to optimize overall SOC test time

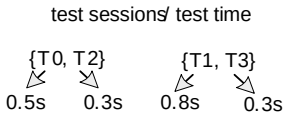
● The NP-complete test scheduling problem may be addressed by using a compatibility graph and heuristic-driven algorithms

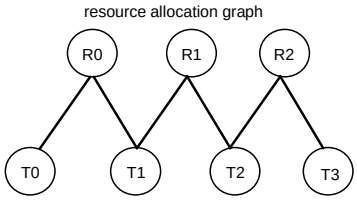
8. System-Level Low Power Testing

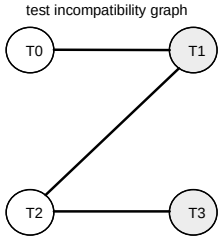
8.1 Power-Constrained Test Scheduling

~ Resource Allocation/Test Incompatibility Graphs ~







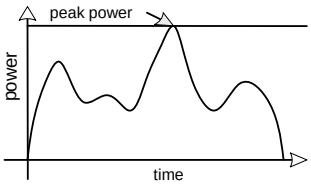


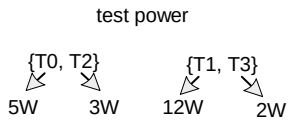
(based on R. Chou et. al, IEEE Trans on VLSI, Vol. 5, No. 2, pp. 175-185 , 1997)

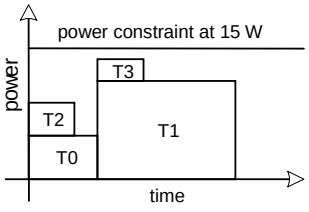
8. System-Level Low Power Testing

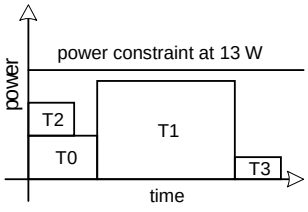
8.1 Power-Constrained Test Scheduling

~ Using Peak Power as Power Constraint ~





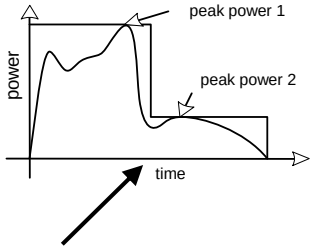




8. System-Level Low Power Testing

8.2 Power Profile Modification

~ Using Two Peaks as Power Model ~

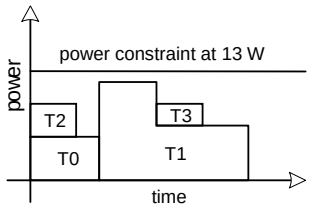


test power

T1 — 12W for 0.3s

6W for 0.5s

Power profile can be modified by pattern modification and/or test set reordering

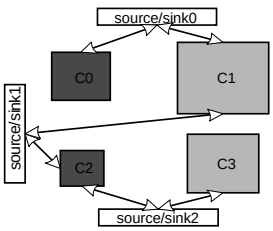


(based on P. Rosinger et. al, IEEE Trans on CAD, Vol. 21, No. 10, pp. 1217-1225 , 2002)

8. System-Level Low Power Testing

8.3 Thermal-Aware Test Scheduling

~ Accounting for On-Chip Temperature Gradients ~



temperature dependent test

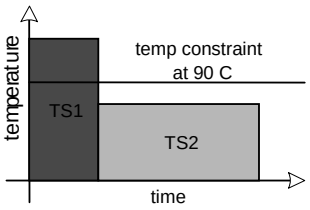
TS1 = {T0, T2} → 130 C

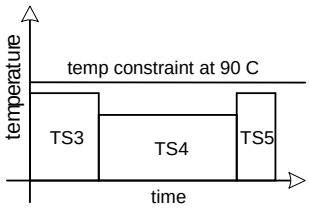
TS2 = {T1, T3} → 70 C

TS3 = {T0, T3} → 80 C

TS4 = {T1} → 60 C

TS5 = {T2} → 80 C





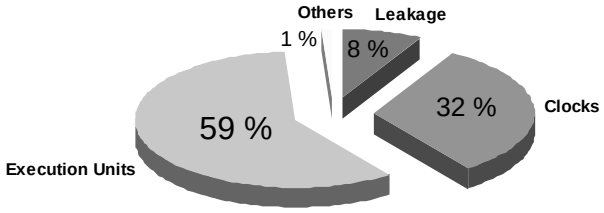
(based on P. Rosinger et. al, IEEE Trans on CAD, Vol. 25, No. 11, pp. 2502-2512 , 2006)

Part 3

Chapter 9

Overview of Low Power Design Techniques

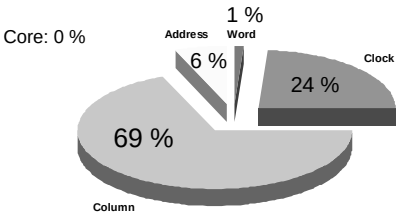
Typical SoC Power Distribution (90nm) *



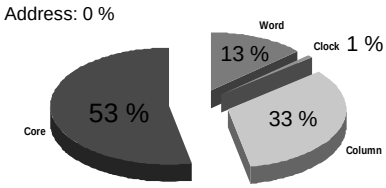
(based on G. Nacer, Sandbridge Technologies, SDC panel, 2005)

9. Overview of Low Power Design Techniques

Typical SRAM Power Distribution *



Dynamic Power



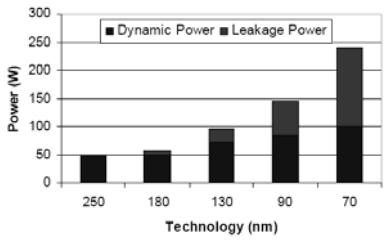
Leakage Power

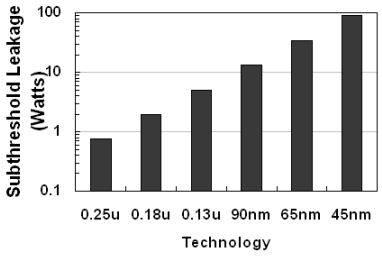
(based on R. Aitken, ARM, SDC panel, 2005)

9. Overview of Low Power Design Techniques

Leakage dominates Power equation beyond 70nm

* Today, leakage power amounts to almost 40% of the total power of a microprocessor





(source: INTEL)

9. Overview of Low Power Design Techniques

Low Power Design Techniques

System & Architecture	▪ Voltage / Frequency Scaling ▪ Architecture (multithreaded design, well managed pipeline, etc.) ▪ Others (H/S partitioning, instruction set, algorithms, etc.)
IC Design & Implementation	▪ Clock Gating ▪ Multiple Supply Voltage ▪ Multiple Threshold Voltage ▪ Substrate-Bias ▪ Power Gating ▪ Others

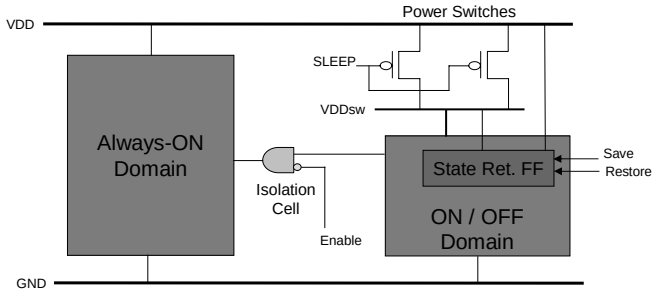
9. Overview of Low Power Design Techniques

Low Power Design Techniques

Circuit (Logic) Design	▪ Low Power Cell Library ▪ Gate sizing (to equalize paths) ▪ Buffer insertion to reduce slew ▪ Logic restructuring to avoid hazards ▪ Memory Bit Cell and Compiler ▪ Others
Process Technology	▪ Reduce Vdd ▪ Threshold Voltage Option ▪ Low Capacitance Dielectric ▪ New Gate Oxide Material ▪ Transistor Sizing ▪ Others

9. Overview of Low Power Design Techniques

Main Power Management Circuitry



PM Structure	Usage
Gated Clocks	Gates clock going to a sequential block
Power Switches	(SLEEP=1) cuts off VDD from going to core
Isolation Cells	(Enable=1) sets output of domain to 0 when power is shut down
State Retention FF	(Save=1) ensures that data is saved when power domain is OFF. (Restore=1) Restores the saved data when power domain wakes up

(courtesy: Srivaths Ravi, TI)

9. Overview of Low Power Design Techniques

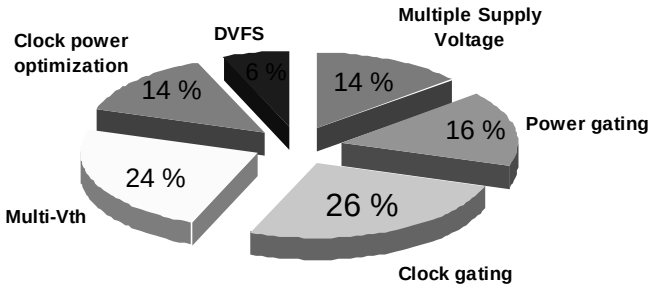
Efficiency of LPD Techniques *

▪ Micro architecture (pipelining, parallelism)	50%
▪ Clock gating and power gating	40%
▪ Logic design	20%
▪ Technology mapping	30%
▪ Cell sizing and wire sizing	30%
▪ Voltage scaling, multi-Vth, multi-Vdd	75%
▪ Floor planning and placement	25%
▪ …	

(based on K. Keutzer, UC Berkeley, SDC panel, 2005)

9. Overview of Low Power Design Techniques

Preferred Techniques to Reduce Power *

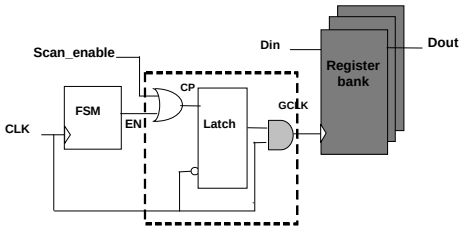


(based on R. Goering, EETimes, 5 July 2007)

9. Overview of Low Power Design Techniques

9.1 Clock Gating

- Reduces dynamic power by restricting clock distribution
- Low overhead technique
- Widely adopted



9. Overview of Low Power Design Techniques

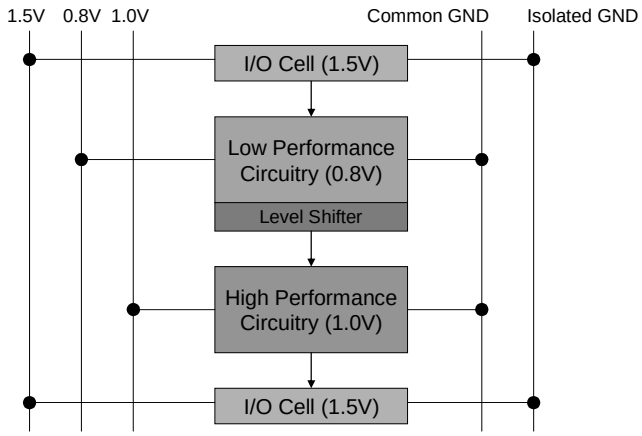
9.2 Multiple Supply Voltage

- Vdd scaling results in quadratic power reduction ($P=kCV^2f$)
- Adopted techniques are:
  - Static voltage scaling
  - Dynamic voltage scaling (change Vdd level during operation)
  - Dynamic voltage and frequency scaling
- Creation of “power islands”
- Reduces dynamic power dissipation
- Requirement / implications:
  - Level shifters to let signals cross power domain boundaries
  - Lower margin for IR drops / increased noise susceptibility

9. Overview of Low Power Design Techniques

9.2 Multiple Supply Voltage

- Static voltage scaling



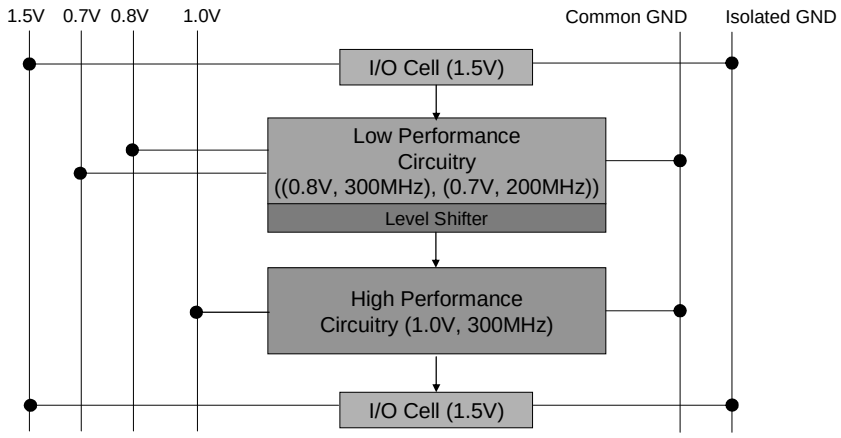
9.2 Multiple Supply Voltage

- When high performance is not required, voltage and frequency can be scaled down
  - Dynamic voltage and frequency scaling
- Design flow is similar to MSV flow
- Implications:
  - Complex control mechanism
  - Complicated timing analysis

9. Overview of Low Power Design Techniques

9.2 Multiple Supply Voltage

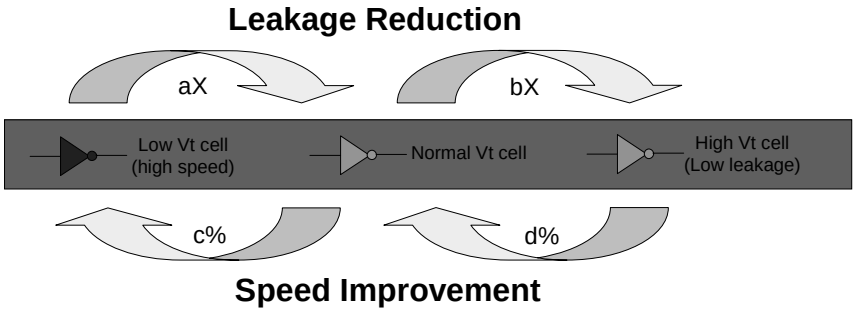
- Dynamic voltage (frequency) scaling



9. Overview of Low Power Design Techniques

9.3 Multiple Threshold Voltage

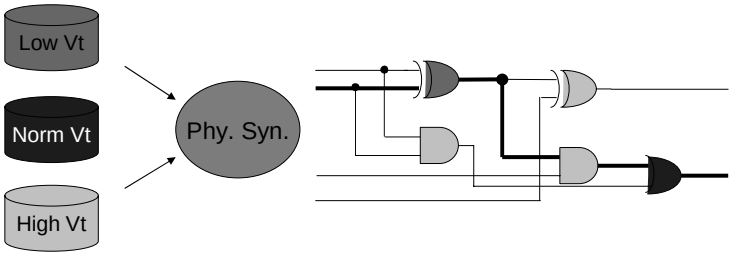
- Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction
- Speed cost to decrease leakage !!



9. Overview of Low Power Design Techniques

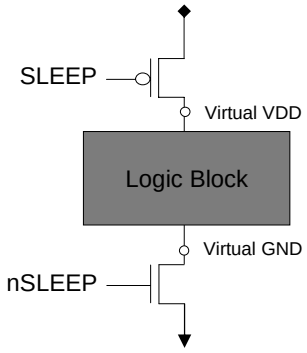
9.3 Multiple Threshold Voltage

- MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)
- Leakage power reduction while meeting timing and no area overhead
- Well established and supported by existing EDA tools



9.4 Power Gating / Power Down

- Used to shut down blocks (power domains) that are not in used (idle mode) hence reducing leakage power
- Done by using Multiple-Threshold CMOS (MTCMOS) switches



9. Overview of Low Power Design Techniques

9.4 Power Gating / Power Down

- Adopted in regular structures (data paths) where the gating transistor can be easily shared
- Power gating cells usually cost 10% area overhead and about 2% performance degradation
- Power-on and power-down sequences can be extremely complex to design and verify
- Careful sizing of gating transistors (wide enough to sustain worst-case switching condition)
- Impact the design flow may be high

9.5 Test Implications of Low Power Design

- Dynamic power and thermal management techniques are attractive since they can achieve maximum performance under a power-temperature envelope
- **But they can have undesirable consequences on Test !!!**

9. Overview of Low Power Design Techniques

9.5 Test Implications of Low Power Design

- **DfT and ATPG tools need to understand the power related constraints and the power management structures**
  - Each step in the DfT insertion has to be made low-power aware
    - Example: scan insertion has to take into account the various power domains so that when a domain is powered down, the scan chains can bypass this domain
  - The ATPG tool has to be guided by a power budget (# toggles)
    - Example: techniques described in Chapter 5

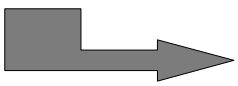
9.5 Test Implications of Low Power Design

- Low power systems generally have several functional modes during which a subset of the system components are active
- But conventional “ad-hoc” approach to testing chips incorporating power management features is to completely power up the chip during test and use a conventional scan approach
  - Excessive (peak) power induced during scan testing needs to be reduced by using multiple test modes – chip test modes have to map low power functional modes

9. Overview of Low Power Design Techniques

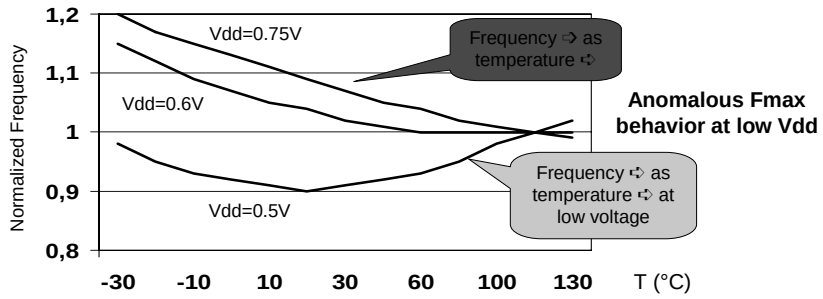
9.5 Test Implications of Low Power Design

- Different activity levels in different parts of a die causes T° variations. Circuit delay change non-linearly with voltage and temperature.
  - Defining the worst-case timing conditions during test will be even more a challenge !!
  - Example:



9. Overview of Low Power Design Techniques

9.5 Test Implications of Low Power Design



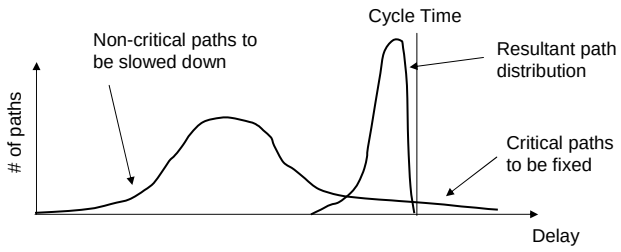
- Traditional Methods of testing at only high temperature for Fmax will be insufficient for low power devices
  - ➢ Testing at additional temperatures increases test time

(based on G. Singer (Intel), Keynote Address, ITC, 2007)

9. Overview of Low Power Design Techniques

9.5 Test Implications of Low Power Design

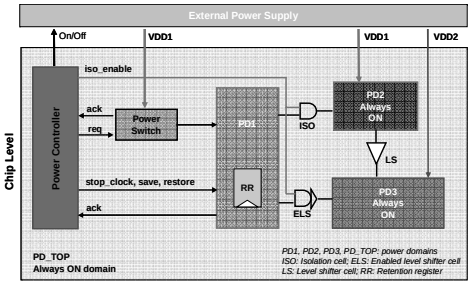
- By using power optimization techniques (gate downsizing, multi-Vth, etc.), more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations
  - ➢ High quality at-speed fault coverage is necessary



9. Overview of Low Power Design Techniques

9.5 Test Implications of Low Power Design

- **Additional work has to be done to test the power management structures themselves. Need of specific test / DfT methods for:**
  - Level shifters
  - Isolation cells
  - State retention registers
  - Power controller
  - Power switches (by far the most challenging task !!)



(courtesy: M. Hirech, Synopsys)

10. Test Strategies for Low Power Devices

Chapter 10

Test Strategies for Low Power Devices

Overview

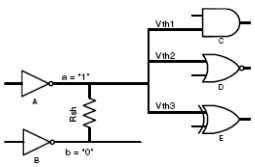
- This chapter is about testing designs that incorporate power management circuitry
- Very few solutions proposed so far (a prospective topic !!)
  - Test generation for multi-voltage designs
  - Test architecture (scan) for multi-voltage designs
  - Test of power management structures (isolation cells, state retention registers, power switches)
- Once again, the goal is:

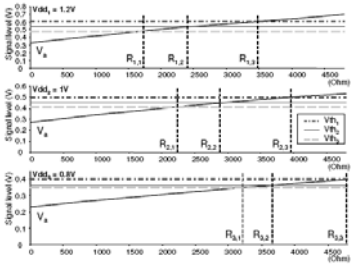
Make test power dissipation comparable to functional power

10.1 Test Generation for Multi-Voltage Designs *

Generate test patterns for multiple supply voltage settings to maximize coverage of Resistive Bridging Faults (RBF) while minimizing test sequence length

Bridging fault example





SPICE simulation for three Vdd settings

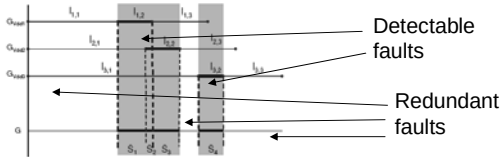
● A given RBF may or may not affect the correct operation of a design depending on the operating Vdd setting → Testing at various Vdd settings is required!!

(based on U. Ingelson et. al., Proc. ATS, 2007)

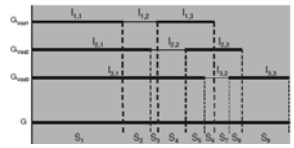
10.1 Test Generation for Multi-Voltage Designs

Identification of Vdd specific test patterns for a given fault f

For full coverage of f, the test pattern should be applied at all three Vdd settings (no full overlap between resistance intervals)



For full coverage of f, the test pattern should be applied at only two Vdd settings: Vdd2 and Vdd3 (full overlap between resistance intervals)



● For a given circuit, 621 test patterns are needed at the three Vdd settings with a commercial tool (207 at each Vdd), while only 391 test patterns applied at 0.8V and 1.2V are needed with the proposed technique (to achieve 100% fault coverage)

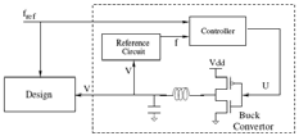
10.2 Power-Managed Scan Using AVS *

- Adaptive Supply Voltage (AVS) Scaling infrastructure for DVS is widely used in modern SoCs to reduce dynamic and leakage power
- Re-use of this infrastructure in the test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
- At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
  - Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan flop (V_t) = 0.35 V, shift Frequency (F_{shift}) = 125 MHz → V_{shift} = 0.635 V

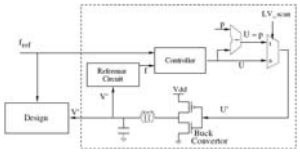
(based on V.R. Devanathan et. al., Proc. ITC, paper 13.3, 2007)

10. Test Strategies for Low Power Devices

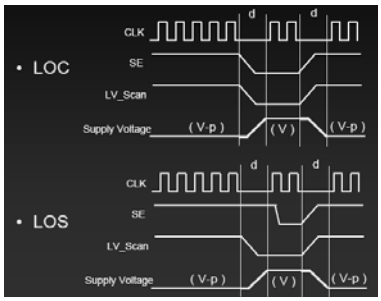
10.2 Power-Managed Scan Using AVS



Conventional Voltage Scaling Apparatus



PMScan: Shift Voltage Scaling Apparatus



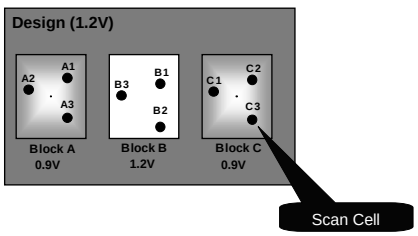
LV_scan: Control signal from tester for low-voltage scan

- Around 45% reduction of dynamic (average and peak) power.
- Around 90% reduction of leakage power.
- PMScan has negligible physical design impact and minimum area overhead.
- Possible tradeoff between test application time and test power !!

10. Test Strategies for Low Power Devices

10.3 Multi-Voltage Aware Scan Cell Ordering *

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93% !!!)



Scan chain assembly

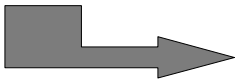
Ordering / Position	Logical	Physical	Multi-Voltage
1	A1	A2	A2
2	A2	A1	A1
3	A3	A3	A3
4	B1	B3	C1
5	B2	B1	C2
6	B3	B2	C3
7	C1	C1	B2
8	C2	C2	B3
9	C3	C3	B1

Level shifter

(based on A. De Colle et. al., Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, pp. 73-84, April 2005)

10.4 Low Power Data Retention Scan Cell *

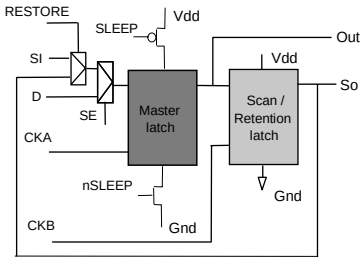
- Low power scan flip-flops can use sleep (power-down) states to reduce leakage power during inactive periods
- Additional latch is needed to store and restore the state of the design after returning from sleep mode
- A low power data retention mechanism needs to be integrated into a conventional scan flip-flop design



(based on V. Zyuban et. al., Proc. ISLPED, pp. 98-102, 2002)

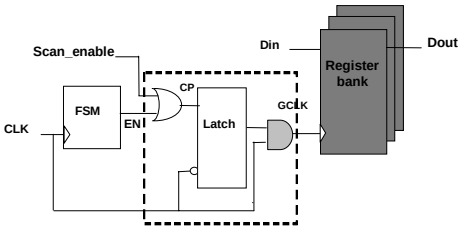
10.4 Low Power Data Retention Scan Cell

- Three modes of operation: functional, scan, low power scan
  - Functional mode: the cell operates as a conventional latch
  - Scan mode (Restore=0): cell operates as a master-slave latch
  - While entering the sleep mode (SLEEP=1), CKB saves data
  - On returning from sleep mode (SLEEP=0, Restore=1), CKA restores data from the retention latch to the main FF



10.5 Testable Clock Gating Logic *

- The clock gating logic may prevent the registers from being fully controllable for the purpose of shifting test data through them
- The proposed logic overrides the clock control signal (EN) and allow for normal operation of the scan chains when shifting test data



- But test power needs to map functional power !!!

(based on A. De Colle et. al., Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, pp. 73-84, April 2005)

10.6 Test of Power Management Structures *

- Test of level shifters
  - A level shifter is a simple buffer
  - No specific test required
- Test of isolation cells
  - Easily testable by adding DfT logic that provides access to the isolation cell control

(based on C.P. Ravikumar et al., Proc. DATE, Hot Topic Session, 2008)

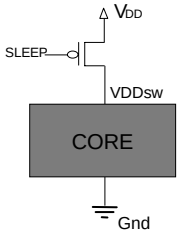
10.6 Test of Power Management Structures *

- Test of state retention registers
  - Similar to memory test
  - Requires both ‘0’ and ‘1’ to be saved and then restored
- Test of power controller
  - Needs test point insertion for providing observability to output pins

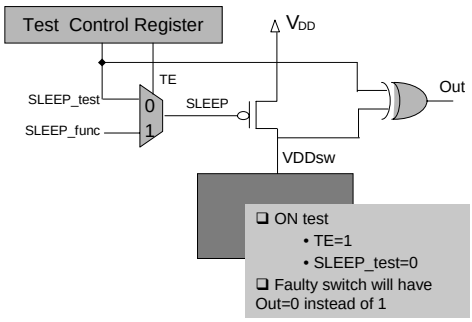
(based on C.P. Ravikumar et al., Proc. DATE, Hot Topic Session, 2008)

10.6 Test of Power Management Structures *

~ Test / Diagnosis of Power Switches ~

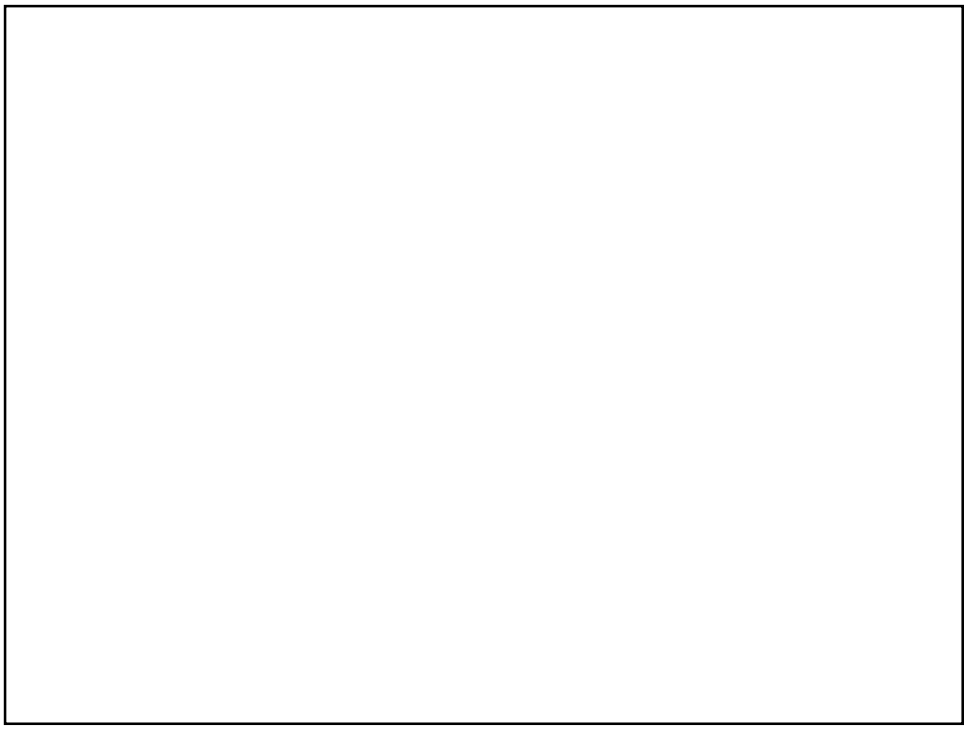


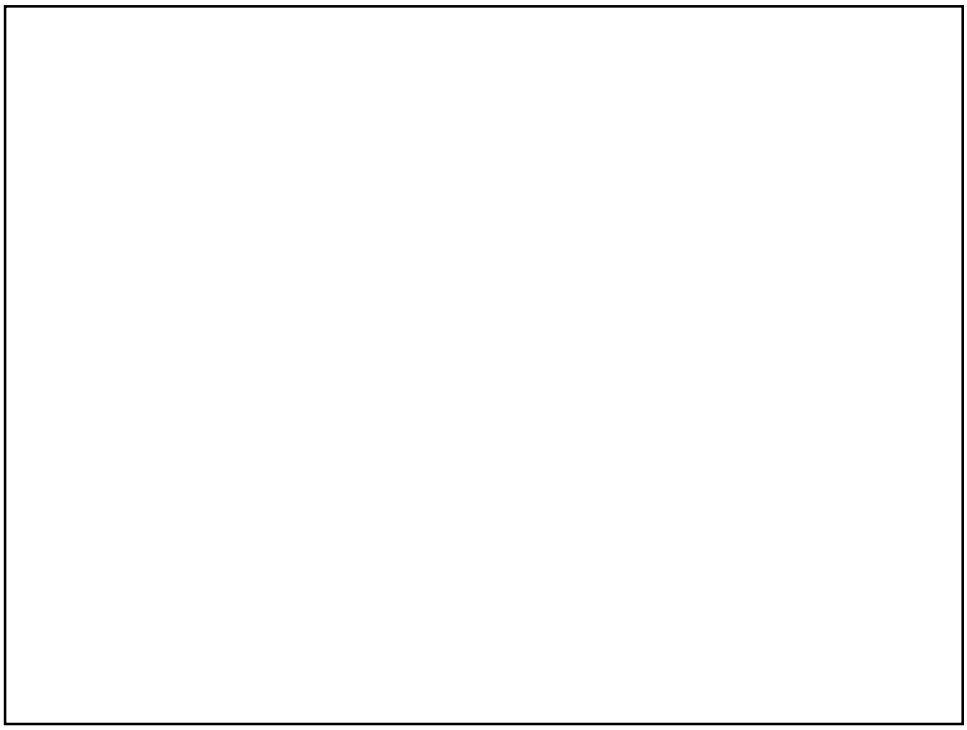
- Conventional power switch test: ON/OFF test for a power domain (iddq current measurements)
- Problem: multiple power switches for a power domain, need to find out which is faulty



- Compare VDDsw with golden value after power ON/OFF
- Test structures:
  - XOR based comparator
  - Control over SLEEP signal in the test mode
  - Test control register bits to supply golden value and mux control

(based on S.K. Goel et. al., IET Computers & Digital Techniques, Vol. 1, pp. 230-236, May 2007)





Chapter 11

EDA Tools for Power-Aware Design-for-Test

Providers of Power-Aware DFT Tools (1/2)

- Synopsys:
  - Galaxy™ Test is a comprehensive test automation solution
  - DFT Compiler and its low power features (for more details on this tools, see “Power and Design for Test: A Design Automation Perspective”, A. De Colle et al, Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, April 2005)
  - DFT MAX and its low power features (for more details on this tools, see “DFT MAX and Power”, R. Kapur et al, Journal of Low Power Electronics (JOLPE), Vol. 3, N° 2, August 2007)
  - TetraMAX® and its low-power management capabilities
  - Details at http://www.synopsys.com/products/solutions/galaxy/test/

Providers of Power-Aware DFT Tools (2/2)

- Cadence:
  - Encounter® Test, a key technology in the Cadence® Encounter digital IC design platform
  - To support manufacturing test of low-power devices, Encounter Test uses power intent information to create distinct test modes automatically for power domains and shut-off requirements. It also inserts design-for-test (DFT) structures to enable control of power shut-off during test. The power-aware ATPG engine targets low-power structures, such as level shifters and isolation cells, and generates low-power scan vectors that significantly reduce power consumption during test. Cumulatively, these capabilities minimize power consumption during test while still delivering the highest quality of test for low-power devices
  - Details at http://www.cadence.com/products/digital_ic/encountertest/

12. Summary and Conclusions

Chapter 12

Summary and Conclusions

12. Summary and Conclusions

- Reliability, test throughput and manufacturing yield may be affected by excessive test power
- Therefore, lowering test power has been and is still a focus of intense research and development
- Following points have been surveyed:
  - Test power parameters and contributors
  - Problems induced by an increased test power
  - Structural and algorithmic solutions for low power test along with their impacts on parameters such as fault coverage, test time, area overhead, circuit performance penalty, and design flow modification
  - Test implications of low power design and emerging test strategies for low-power devices

12. Summary and Conclusions

- Past work explored primarily four directions:
  - ATPG-based low power test approaches are not intrusive; they are pattern dependent and may incur additional computational cost in the design flow.
  - DFT-based low power test approaches change the scan infrastructure; can be pattern independent and hence can guarantee power reduction in a certain range.
  - Low power test data compression techniques combines reduction of test data volume and test application time with power consumption during test
  - System-level low power test considerations can be combined with any of the above and improve test concurrency.
- Future work will be mainly on:
  - Test strategies for low power designs

THANK YOU!

And let us make testing "*cool*".