Keynote intitulé "Power : The New Dimension of Test"

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Power: The New Dimension of Test

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Outline

1. Relevance of power during test
2. Main test power issues
3. Reducing test power by dedicated techniques
4. Low Power Design and its implications on test
5. One step to the future

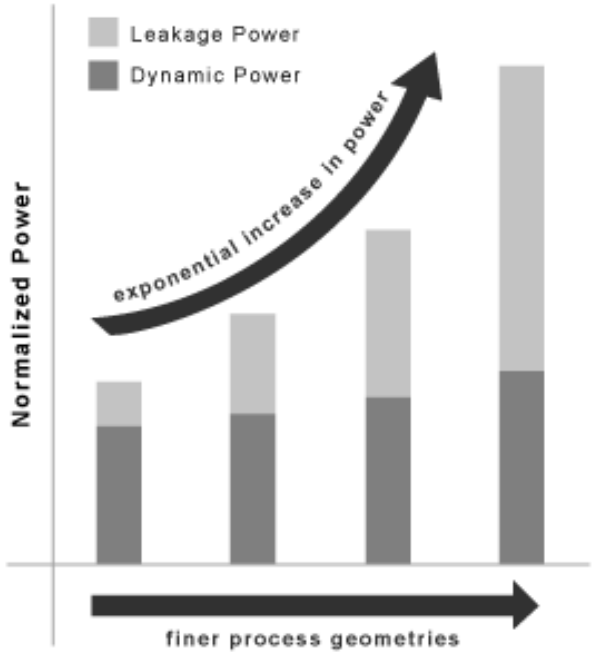
Power Consumption in CMOS

Switching (dynamic) Power

- Due to charge/discharge of load capacitance during switching
- $P_{DYN} \propto V_{DD}^2 . F_{CLK}$

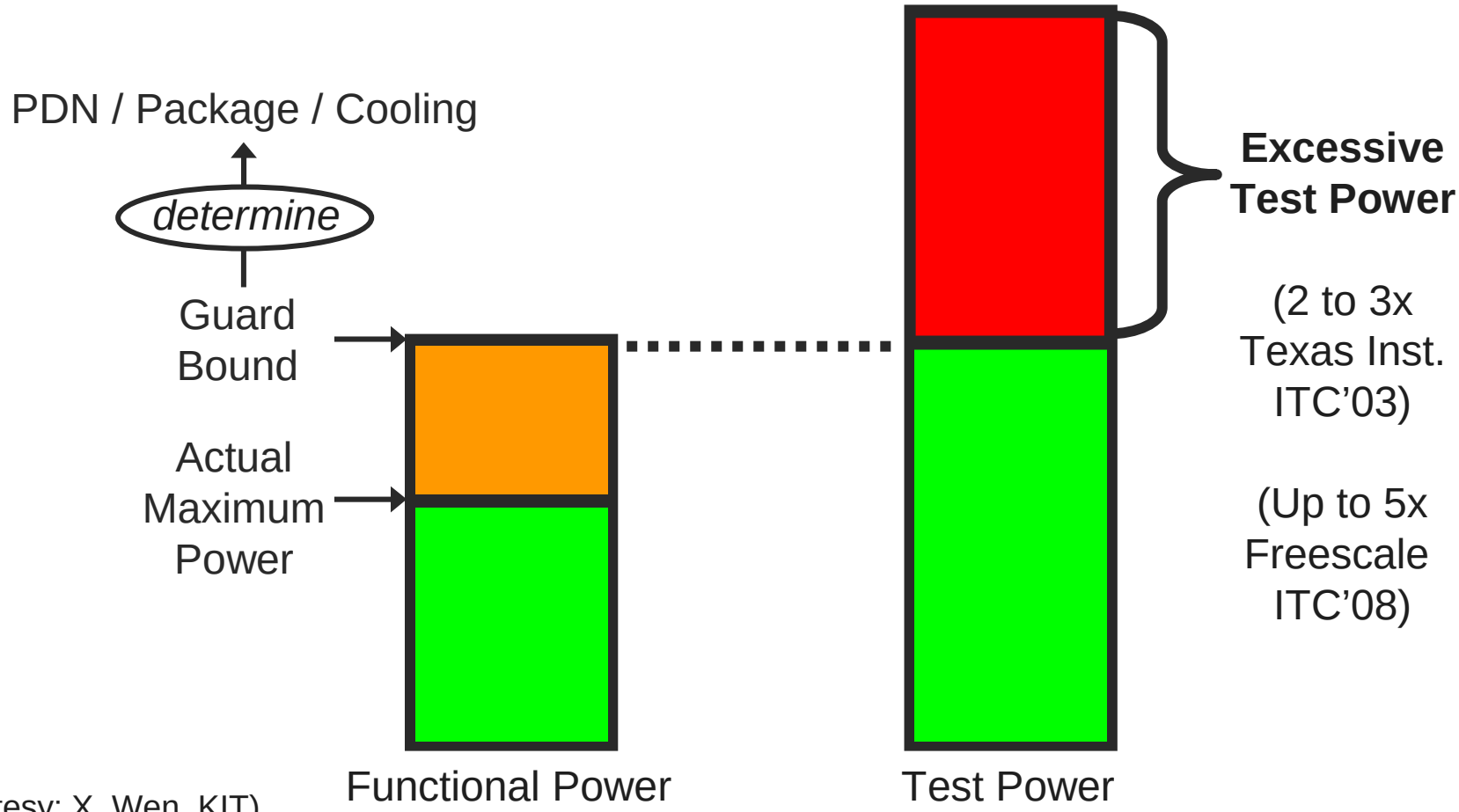
Leakage (static) Power

- Power consumed when the circuit is idle
- Mainly due to sub-threshold leakage
- $I_{SUB} \propto V_{DD} / V_{TH}$



Power During Test …

Much higher than during functional operations



(courtesy: X. Wen, KIT)

Power During Test …

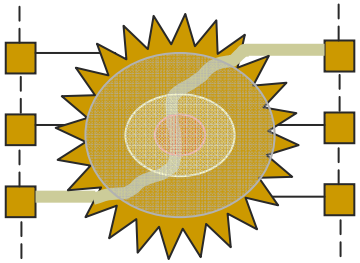
Main reasons for excessive test power

- No correlation between consecutive test vectors
- Test vectors may ignore functional (especially power) constraints
- Non-functional clocking during test
- DFT (e.g. scan) circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction

For conventional (non low-power) designs, dynamic power is the main responsible for excessive test power !!

Leakage power is a real issue during IDDQ test (reduced sensitivity) and during burn-in test (can result in thermal runaway condition and yield loss)

Main Test Power Issues



Elevated Average Power

↓

Temperature Increase

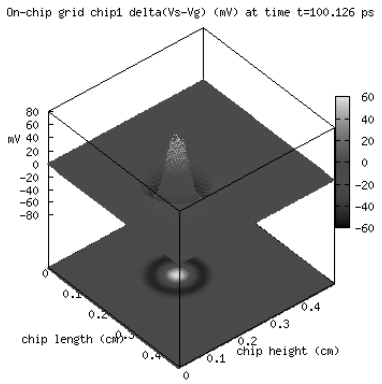
↓

$T_{die} = T_{air} + \theta \times P_{Average}$

Excessive Heat Dissipation

Structural degradations (hot spots)	Hot-Carrier-Induced Defects Electro-migration Dielectric Breakdown	Low Allowable Parallelism (Wafer Testing & Package Testing)
↓	↓	↓
Chip Damage	**Reduced Reliability**	**Low Test Throughput**

Main Test Power Issues



High Instantaneous Current

↓

Elevated Peak Power

↓

Power Supply Noise (IR-Drop, Ldi/dt)

↓

Significant Delay Increase due to Excessive PSN

↓

Erroneous Behavior Only During Testing (test fail)

↓

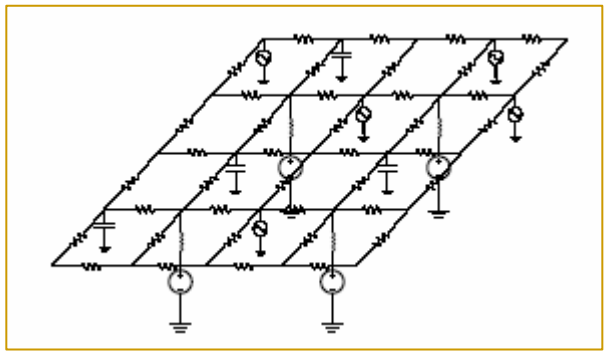
Manufacturing Yield Loss
(Over-Kill)

As huge designs can be manufactured today, most power-related test issues (during scan) are due to excessive peak power

Reducing Test Power

Straightforward Solutions

- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing packages and use of cooling equipments
- Over sizing power distribution network (PDN)
  - Grid Sizing based on functional power requirements
    - all parts not active at a time
  - Grid Sizing for test purpose too expensive !!



Costly or longer test time

Reducing Test Power

Main classes of dedicated solutions

- Design for Test Power Reduction
- Test Data Manipulation for Power Reduction
- Power-Aware Test Data Compression *
- System-Level Power-Aware Test Scheduling *

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

* See: P. Girard, X. Wen and N. Touba, chapter “Low Power Testing” of book “System-on-Chip Test Architectures: Nanometer Design for Testability”, Morgan Kaufmann, 2007.

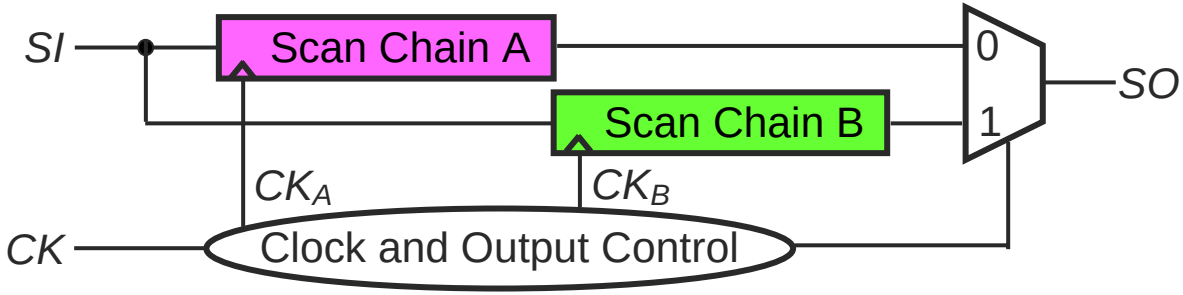
Design for Test Power Reduction

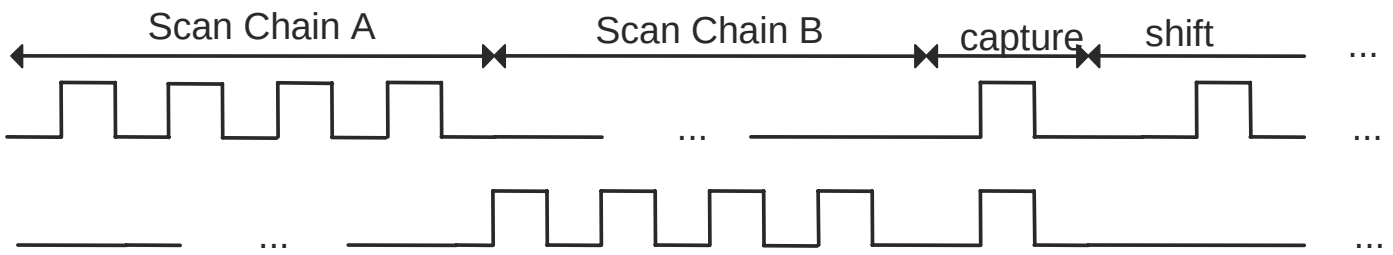
During scan testing (standard or LOC-based at-speed):

Shift Power Reduction	Capture Power Reduction
• **Shift Impact Blocking** - *blocking gate*, *special scan cell* - *first-level power supply gating* • **Scan Chain Modification** - *scan cell reordering* - *scan chain segmentation* - *scan chain disable* • **Scan Clock Manipulation** - *splitting*, *staggering* - *multi-duty clocking*	• **Partial Capture** - *circuit modification* - *scan chain disable* - *one-hot clocking* - *capture-clock staggering*

Design for Test Power Reduction

Example : Scan chain segmentation





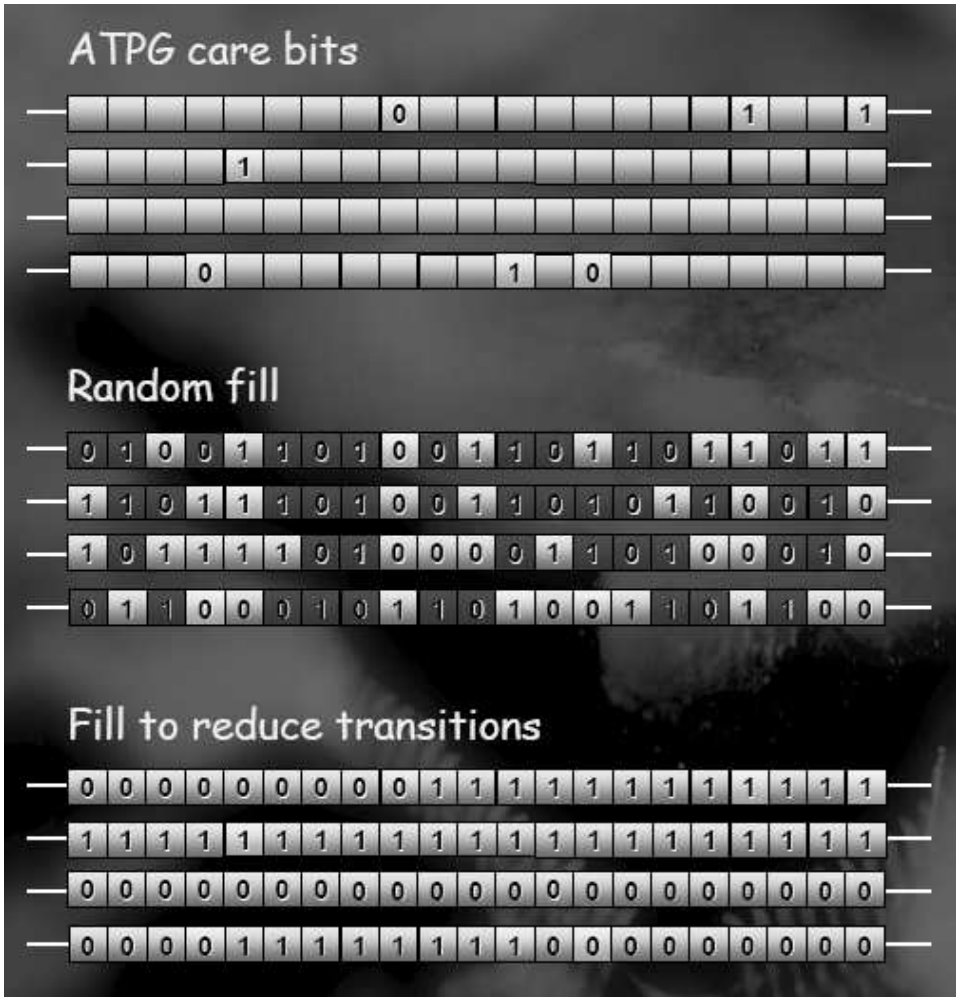
- Controllable and data-independent effect of shift power reduction.
- No change to ATPG and no increase in test application time.

Test Data Manipulation

	Shift Power Reduction	Capture Power Reduction
Low-Power ATPG	• **Blocking Test Generation** • **Low Power Compaction**	• **Test Generation** *- power constraint checking* *- target fault restriction*
Low-Power X-Filling	• **X-Filling** *- 0-fill* *- 1-fill* *- adjacent-fill*	• **FF-Oriented X-Filling** *- justification-based* *- probability-based* *- hybrid* • **Node-Oriented X-Filling** *- internal-switching-activity-aware* *- critical-path-aware*

Test Data Manipulation

Example: Low-Power X-filling



- Fill to reduce power in scan cells and combinational logic
- X-filling can be used to reduce shift-in (not shift-out) power or capture power
- Can be extended to support test compression
- Very efficient !

Evaluating …

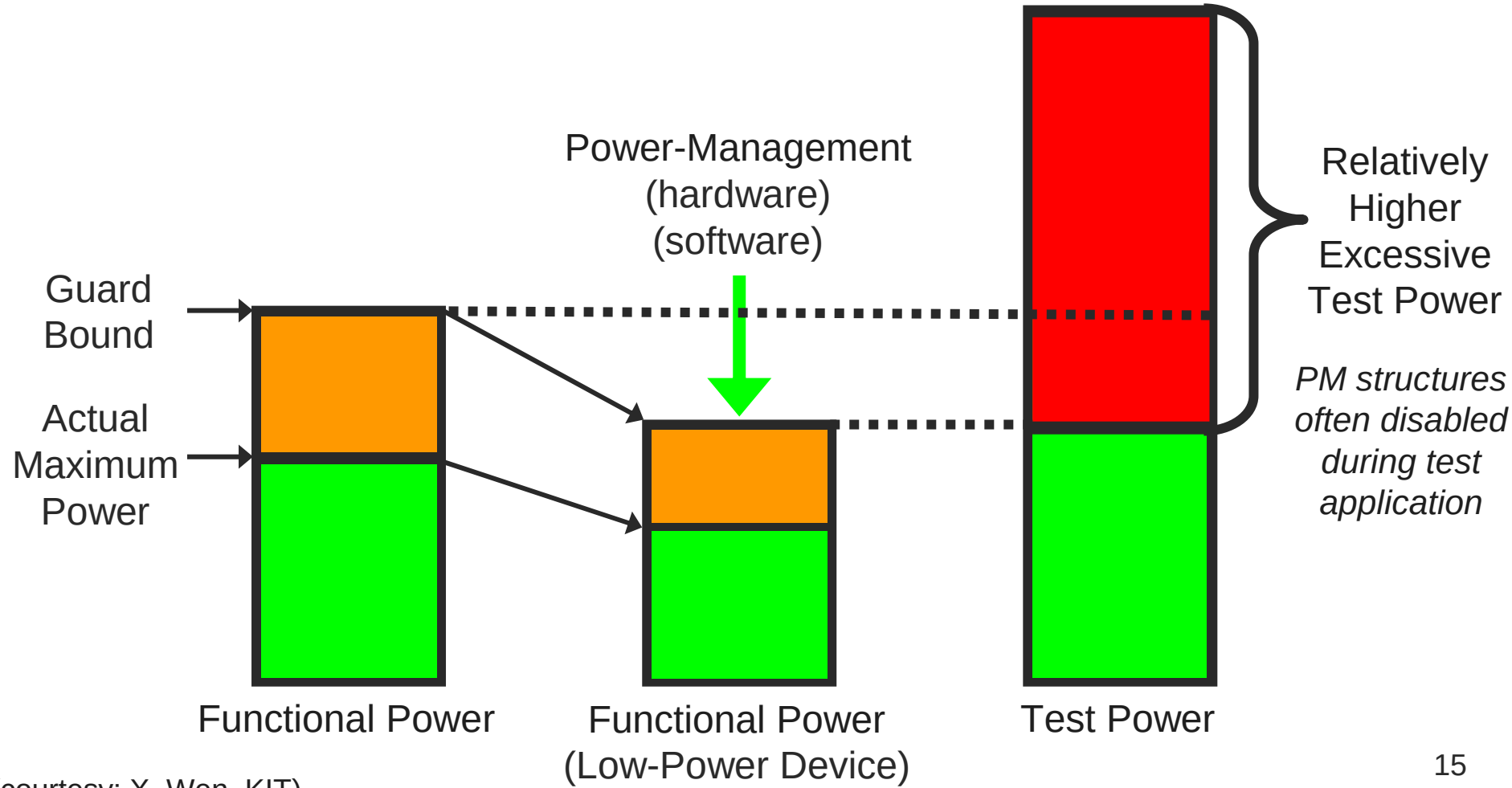
… Test Power Reduction Strategies

- Power reduction effectiveness — *High*
- Fault coverage impact — *Low*
- ATPG engine impact — *Minimum*
- Test data volume impact — *Low*
- Test time impact — *Low*
- Functional timing impact — *Low*
- Area overhead — *Low*
- Usability with test compression — *High*
- Design effort — *Minimum*
- Design flow change — *Low*

(source: S. Ravi, TI, ITC07)

Power During Test …

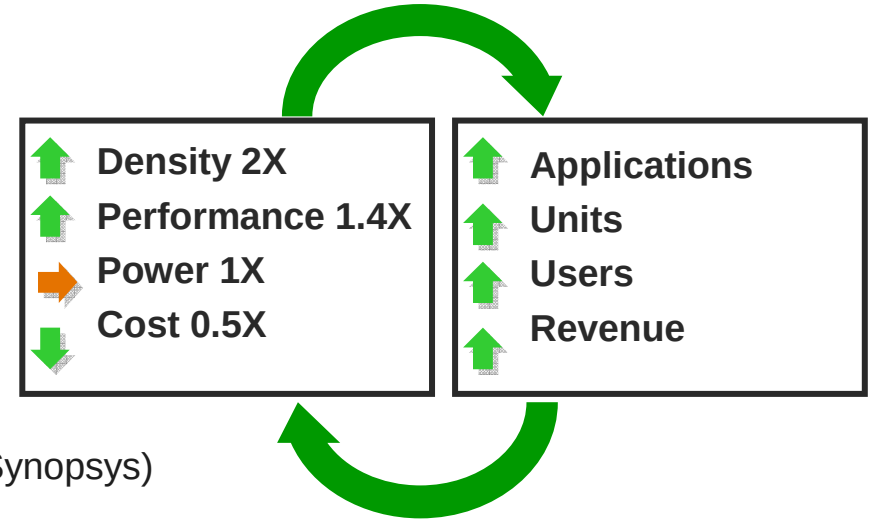
Even more critical for Low-Power Devices !!



(courtesy: X. Wen, KIT)

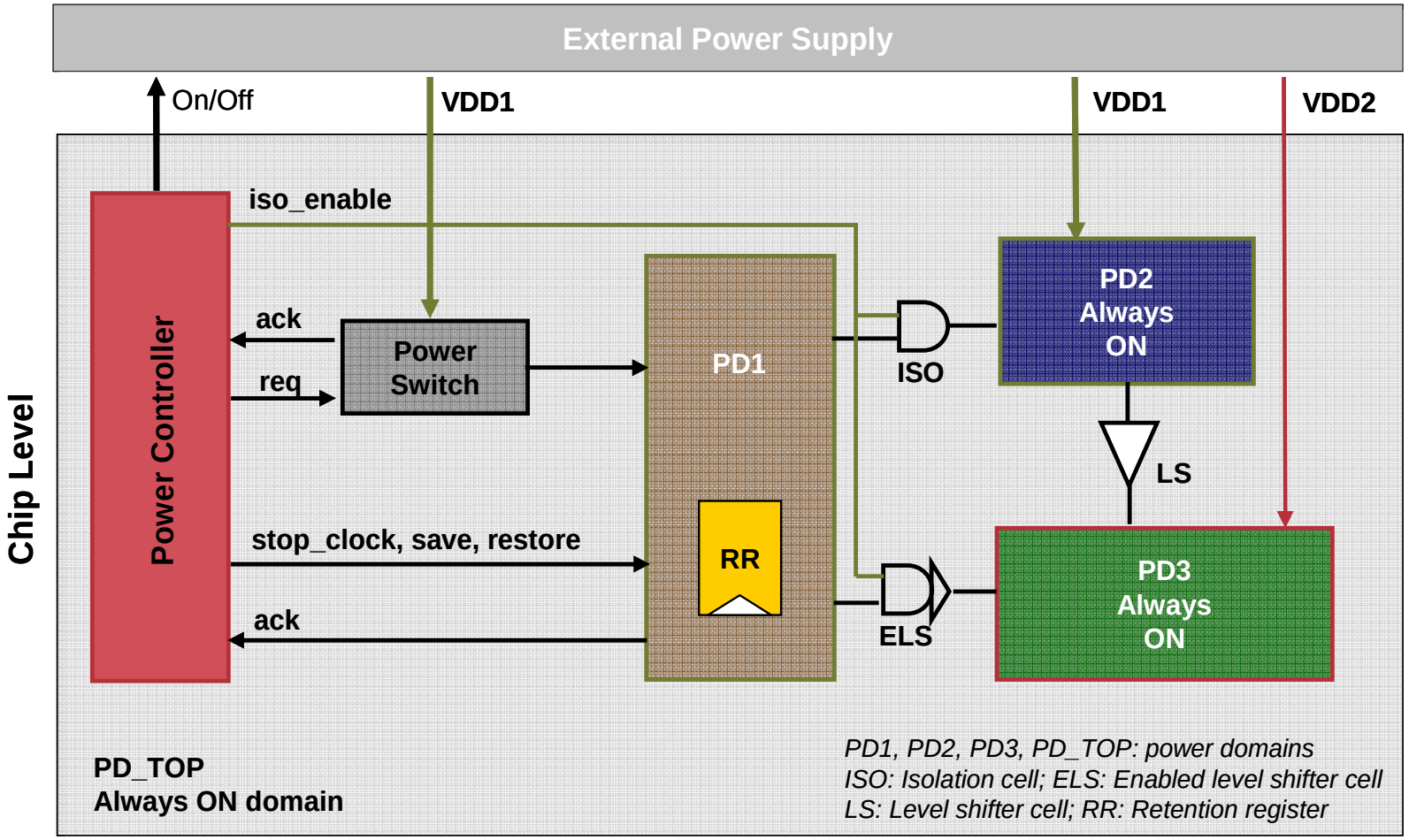
Low Power Design (LPD)

Main LPD techniques	Power reduction	
	Dynamic	Leakage
Clock gating	➨	
Power gating	➨	➨
Multi-Voltage domains	➨	
Multi-Threshold cells		➨



(courtesy: M. Hirech, Synopsys)

Power Management Infrastructure



(courtesy: M. Hirech, Synopsys)

Implications of LPD on Test

- Reduce (even more) test power by using the power management infrastructure (and/or applying the previous dedicated solutions)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures

And still target:

High fault coverage, short test application time, small test data volume, low area overhead, etc … while making test power dissipation (dynamic and leakage) comparable to functional power

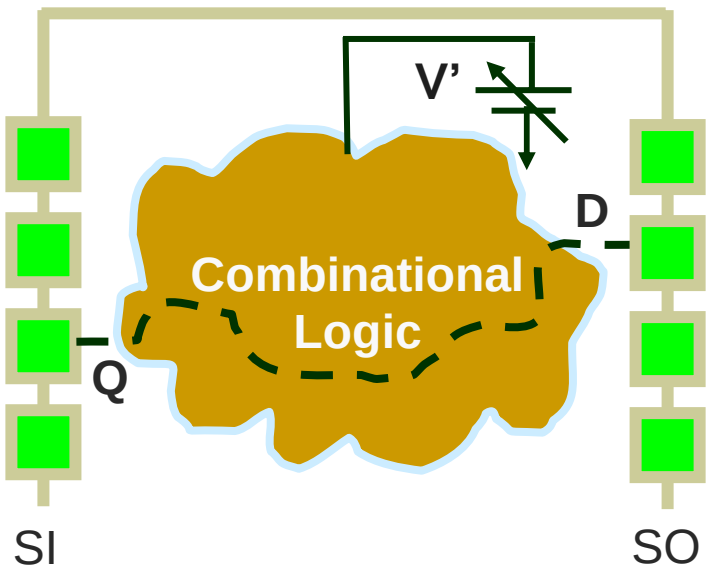
Use of PM Infrastructure

Some solutions exist to reduce test power by considering the PM infrastructure … but further developments are needed !

Dynamic Power Reduction	Leakage Power Reduction
• Test generation for multi-voltage designs • Test Relaxation and X-Filling for gated clock designs • DFT for gated clock designs • Test planning for multi-power domains architectures	• Low-power data retention scan cells
• DfT (scan) for multi-voltage designs (power-aware scan chain construction for MSMV and PSO–aware testing)	

Use of PM Infrastructure

Example 1: Voltage scaling in scan mode



Scaled voltage V' in Scan Mode gives a lower shift power : $(V'/V)^2$

- During scan shift, the combinational logic need not meet timing
- The scan shift speed is usually lower than the functional speed

Using a lower supply voltage during scan shifting to reduce dynamic and leakage power dissipation.

Done by re-using the voltage scaling infrastructure in test mode

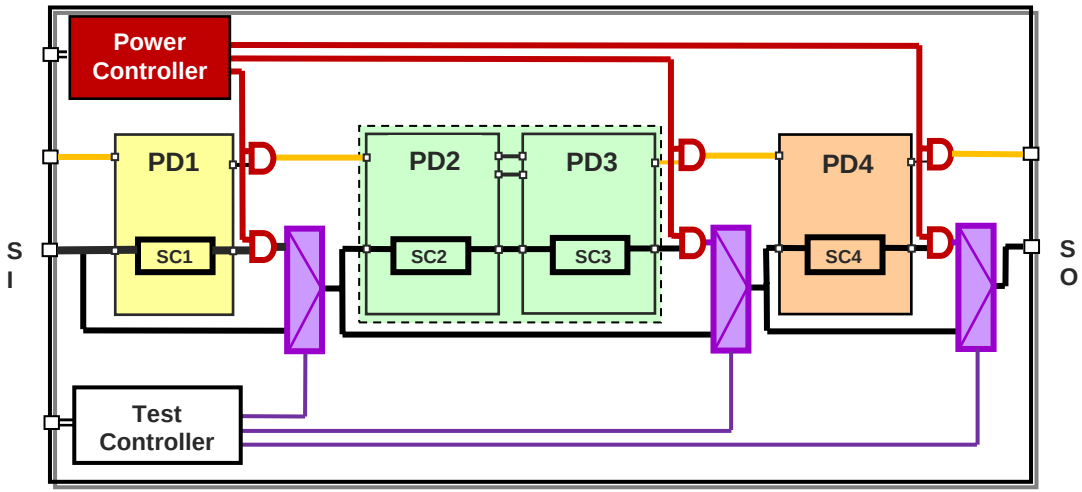
(source: C.P. Ravikumar et. al. – TI India, JOLPE, Vol. 1, N° 1, April 2005)

Use of PM Infrastructure

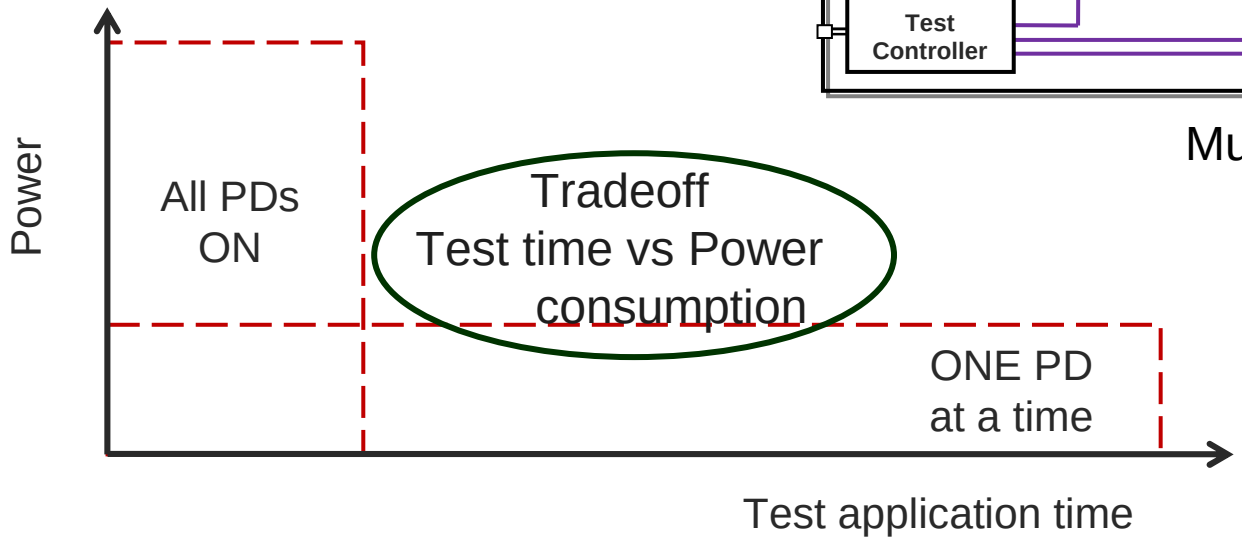
Example 2: Power Domain Test Planning

Objective:

Create distinct test modes (test partitioning) for power domains



Multi-mode DFT architecture



(Source: M. Hirech, Synopsys, DATE 2008)

Preserving Test Functionality

Main Challenge

- Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints

Specific test control strategies and extra DfT insertion are required for preserving functionality of the test infrastructure !

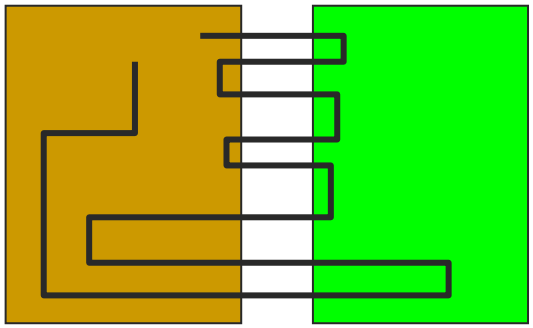
- Similar challenges exist for clock gating designs, though some of them are comprehended today by existing test methods and tools *

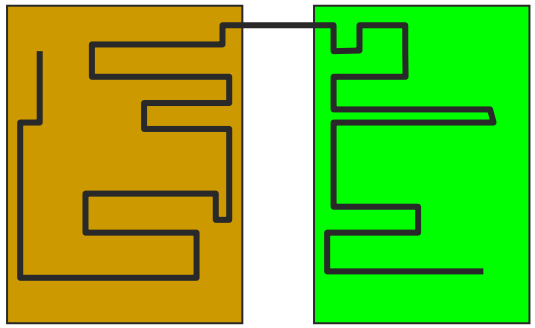
* S. Ravi, TI India, ITC 2007

Preserving Test Functionality

Example 1: MSMV-aware scan chain assembly

- Minimize the occurrence of chains that cross voltage domains





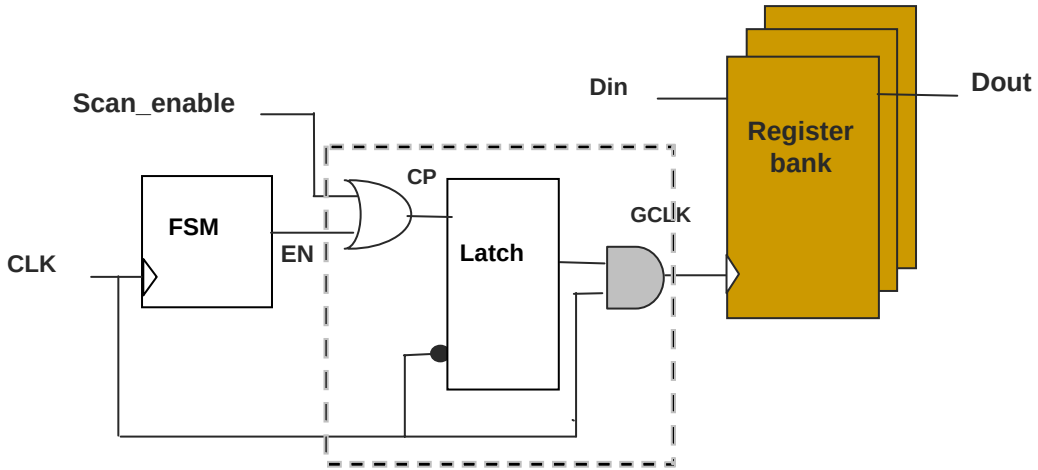
- Avoid unwanted power down during scan shift/capture
- Chain must not span domains that must be independently on/off
- Chains traversing through powered down domains must bypass them
- ...

(Source: M. Hirech, Synopsys, DATE 2008)

Preserving Test Functionality

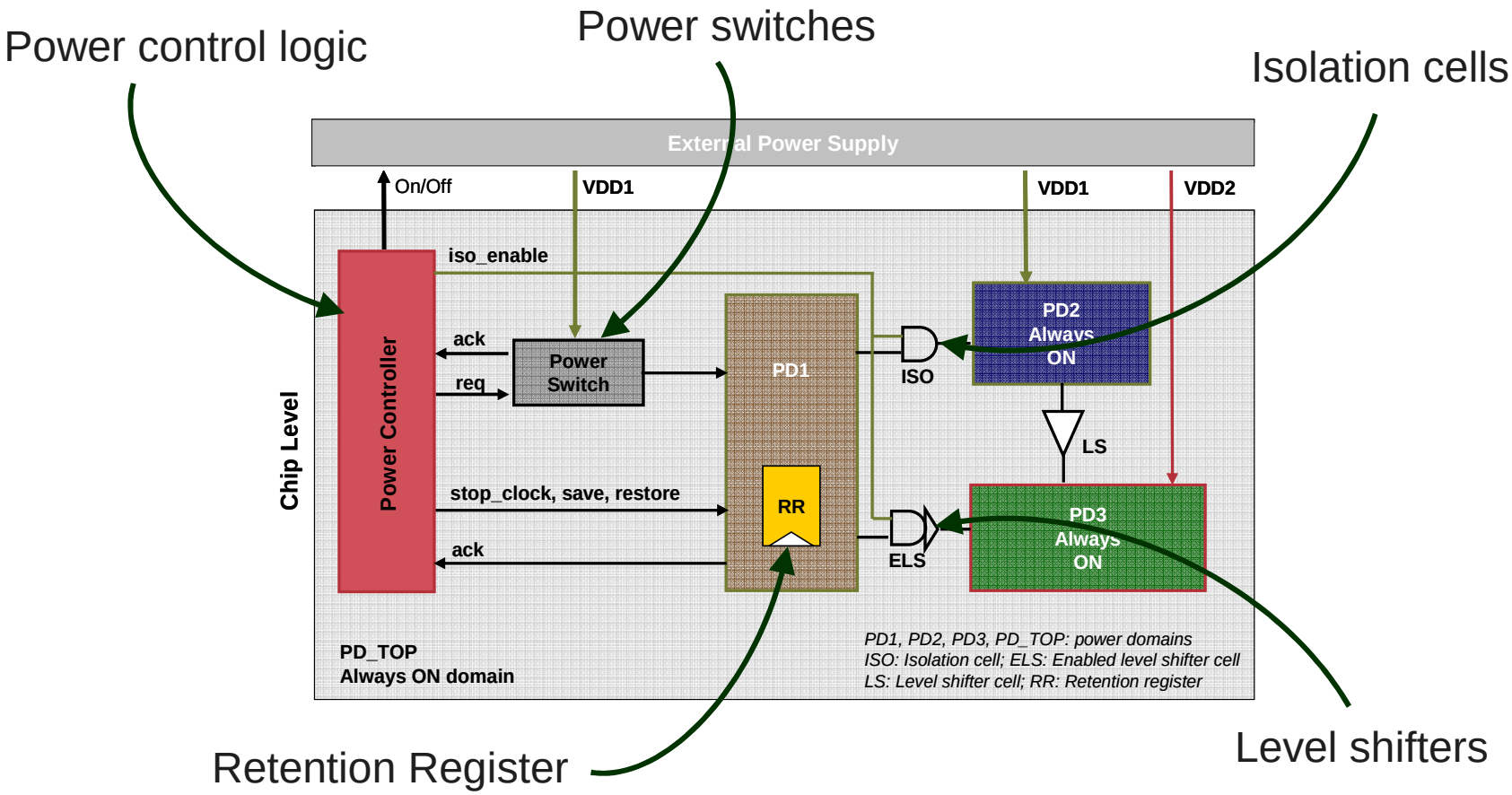
Example 2: Dedicated clock gating logic

- The clock gating logic may prevent scan registers from being fully controllable for the purpose of shifting test data through them
- The proposed logic overrides the clock control signal (EN) and allows for normal operation of the scan chains when shifting test data



(source: A. De Colle et al. - Synopsys, JOLPE, Vol. 1, N° 1, April 2005)

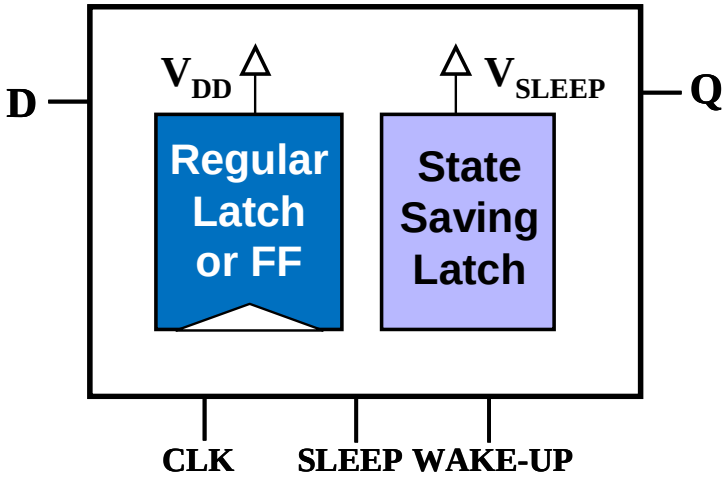
Test the PM Structures



PM structures require dedicated DFT methods and ATPG patterns, and need to consider power modes !

Test the PM Structures

Example 1: State Retention Cell



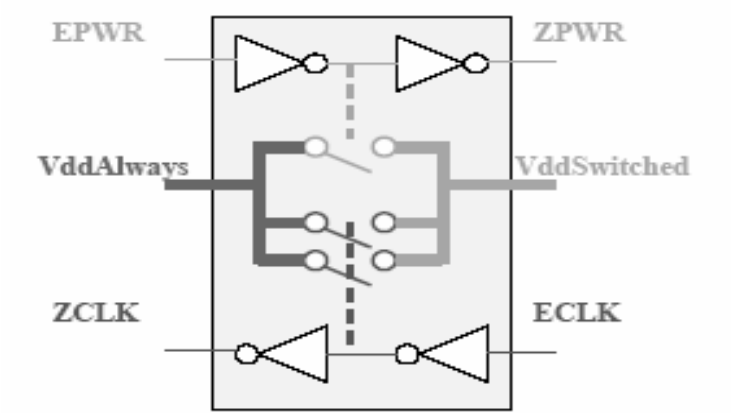
Main test challenges:

- Retention cells are usually tested as normal FFs by test generation
- Retention capability in power down mode has to be tested
- Impact of power domain switching on retention has to be tested
- Considering only the stuck-at fault model is not enough !

(source: K. Chakravadhanula et al. – Cadence, ATS 2008)

Test the PM Structures

Example 2: Power Switch



Main test challenges:

- Rush current during power up → specific functional mode → test mode has to map functional mode !
- Testing micro-switches individually → DfT needed to turn ‘on’ and ‘off’ each switch individually and allow R_{off}/R_{on} measurement
- Switches are usually daisy-chained → ensure the chain is not broken by adding control and observability to the ring control signals

(source: L. Souef et al. - ST NXP, ITC 2008)

One Step to the Future

- **New test solutions** for Low-Power Design using the PM infrastructure and preserving the test functionality will be needed
- **New test solutions** for PM structures will also be needed

Main accompanying challenges:

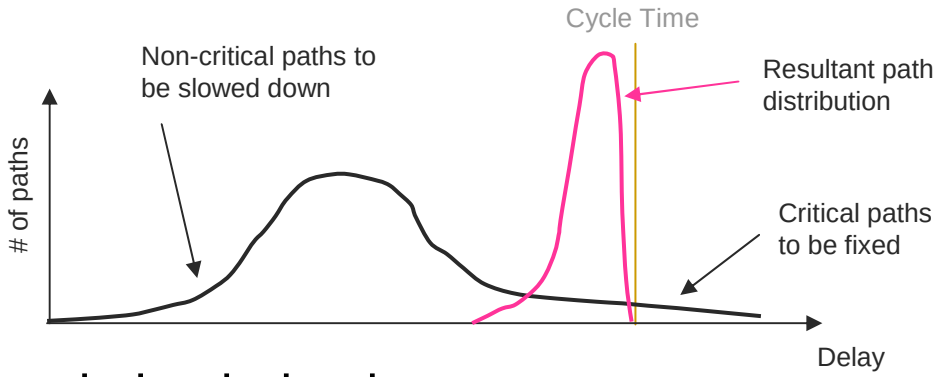
- High quality delay fault coverage will be mandatory !!
- Test power estimation needs improvements !

Test conditions may be influenced by LPD:

- Testing at only high T° for Fmax will be insufficient

Delay Fault Coverage

- To reduce leakage, multi-threshold voltage designs use high-Vt cells to decrease leakage current where performance is not critical
- By using such power optimization techniques, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations
  - PDF selection more complex
  - More test data are needed
  - Sensitivity to variations



- PSN has a significant impact on the timing behavior
  - Need to integrate PSN effects in delay test pattern generation

Solutions for high quality at-speed fault coverage are needed !

Test Power Estimation

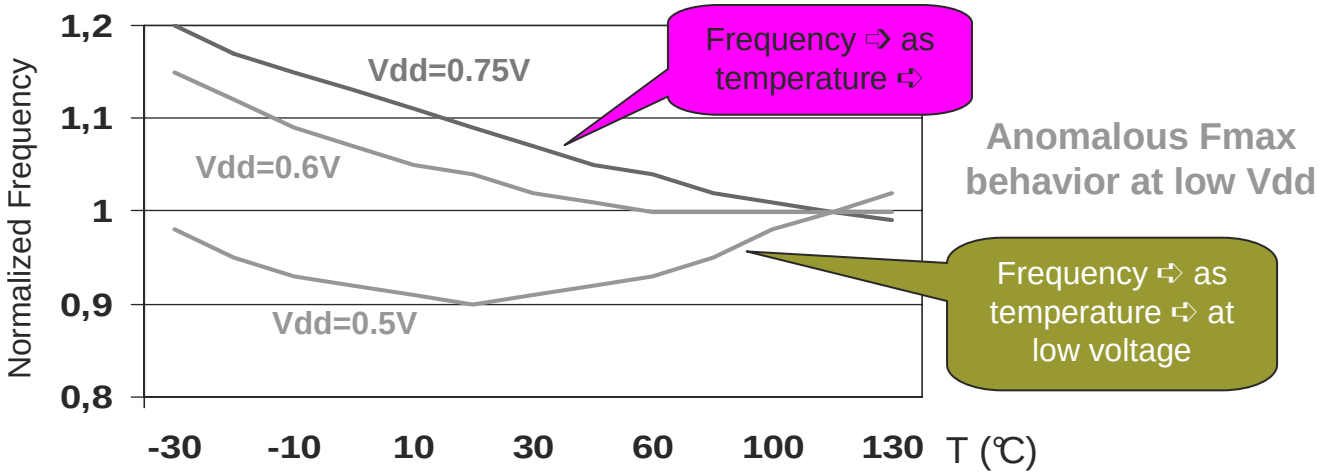
- Needed for test space exploration (DfT/ATPG) early in the design cycle
- Availability of scan enhanced design and ATPG patterns only at the gate level in today's design flows imposes the usage of gate-level estimators for test power
- Conventional flow adopted to perform estimation is simulation-based
- Challenges for multi-million gate SoCs
  - Time-consuming !!
  - Dump sizes can be very large !!
- The weighted transition model is widely used but not accurate enough

Faster and low cost solutions for test power estimation are needed !

(source: S. Ravi, TI, ITC07)

Test Conditions of LPD

- Different activity levels in different parts of a die causes T° variations. Circuit delay change non-linearly with V and T°.
- Defining the worst-case timing conditions during test will be even more a challenge !!



Traditional Methods of testing at only high temperature for Fmax will be insufficient for LP devices !

(Souce: G. Singer - Intel, ITC 2007)

Thank You !