Tutorial intitulé "Power-Aware Testing and Test Strategies for Low Power Devices"

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Full-day tutorial on

Power-Aware Testing and Test Strategies for Low Power Devices

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Power-Aware Testing and Test Strategies for Low Power Devices

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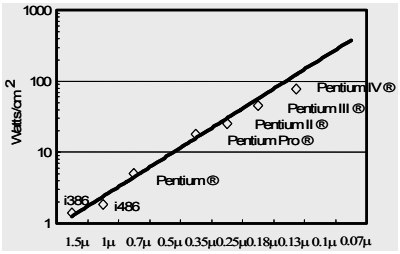
Motivation and Objectives

Power Consumption Trends

- Exponential growth in transistor density
  - More functionality
- But linear reduction in supply voltage
  - Not adequate to prevent power density to increase

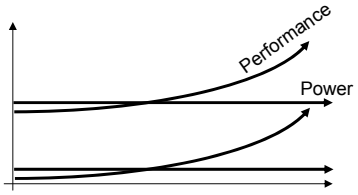


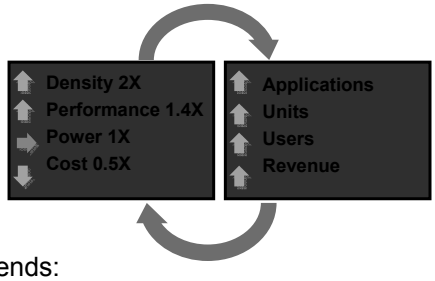
(Tirimurti et al., DATE, 2004)

Motivation and Objectives

Power Consumption Trends

- The new power-performance paradigm:





- By-product of power consumption trends:
  - Low (fixed) power budget to limit power density
  - But ever increasing integration and performance …
  - Adoption of low-power design and power management techniques

(courtesy: M. Hirech, Synopsys)

Motivation and Objectives

Power Impact on Test

- Power constraints have severe impact on test
- Implications to test and DfT engineers / test tool developers :
  - Reduce power consumption also in test mode
  - Dedicated test strategies for low-power devices are needed
- **Objectives of this tutorial:**
  - Learning more about the impact of power during test
  - How to alleviate test power issues
  - How low-power devices and power management structures can be tested safely

Outline

1. Introduction
2. Power Issues During Test

Part 1

3. Low-Power Test Pattern Generation
4. Power-Aware Design-for-Test
5. Power-Aware BIST and Test Data Compression
6. Power-Aware System-Level Test Planning

Part 2

7. Low-Power Design Techniques and Test Implications
8. Test Strategies for Multi-Voltage Designs
9. Test Strategies for Gated Clock Designs
10. Test of Power Management Structures

Part 3

11. EDA Solutions for Power-Aware Design-for-Test

Conclusion

1. Introduction

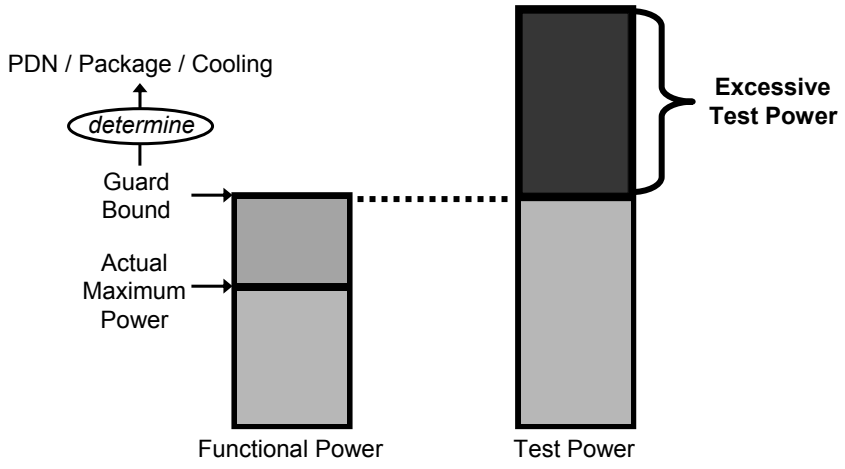
Part 1

Chapter 1

Introduction

1. Introduction

Power dissipation in the test mode is much higher than during functional operations



1. Introduction

Many industrial experiences reported in the literature

[ITC 2003] : Texas Inst. & Siemens AG
ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM

Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%

[ITC 2008] : Freescale
Power under test mode up to 3.8X power during functional mode

And many other experiences …

1. Introduction

Many reasons (i)

- **Switching activity may be higher during testing**
  - Structural testing is predominant and tends to produce more toggling than functional patterns because:
    - ✓ Conflict of objectives between test and functional mode
    - ✓ No correlation between consecutive test vectors
    - ✓ DFT (e.g. scan) circuitry is intensively used
  - Test compaction leads to higher switching activity due to parallel fault activation and propagation
  - Multiple cores in a SoC are tested in parallel to reduce test time

1. Introduction

Many reasons (ii)

- **Typical power management schemes are disabled during testing**
  - Clock gating is turned off to improve observability of internal nodes
  - Dynamic frequency scaling is turned off because:
    - ✓ The system clock is bypassed, or
    - ✓ The PLL suffers from a relocking time overhead during which no meaningful test can be conducted
  - Dynamic voltage scaling is usually avoided due to time constant in stabilizing supply voltage

1. Introduction

Power availability and quality may be limited during testing

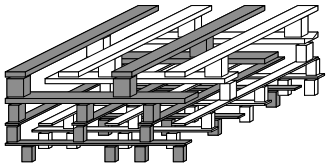
Main reasons

- Long connectors from Tester Power Supply (TPS) to probe-card often result in higher inductance on the power delivery path. This may lead to voltage drop during test power cycling
- During wafer sort test, all power pins may not be connected to the TPS, resulting in reduced power availability
- Current limiters placed on TPS to prevent burn-out due to short-circuit current may affect power availability and quality

1. Introduction

Straightforward solutions for reducing test power

- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing packages and use of cooling equipments
- Over sizing power distribution network (PDN)
  - Grid Sizing based on functional power requirements - all parts not active at a time
  - Grid Sizing for test purpose too expensive !!



Costly or longer test time

1. Introduction

~ Test in the Past ~

High Fault Coverage
Short Test Time
Small Test Data Volume
Low Test Development Efforts
Low Area Overhead

~ Test from Now ~

•
•
•
+

Low Test Power
(low average and peak power)

Make test power dissipation comparable to functional power

Chapter 2

Power Issues during Test

2.1 Power and Energy Basics

- Static Leakage Power
  - Power consumed when the circuit is idle
  - The static power dissipation of a circuit is given by

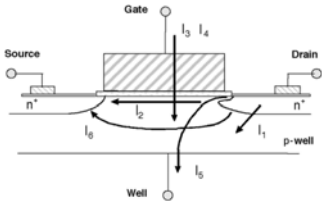
$$P_{stat} = \sum_{i=1}^{n} I_{stat_i} \cdot V_{DD}$$

where I_{stat} is the current that flows between the supply rails in the absence of switching activity and i is the index of a gate in a circuit consisting of n gates.

2. Power Issues during Test

2.1 Power and Energy Basics

- Static Leakage Power
  - Due to six components of leakage current



I_1: reverse-bias pn junction leakage current
I_2: sub-threshold leakage current
I_3: gate oxide tunneling current
I_4: gate current due to hot carrier injection
I_5: gate induced drain leakage current
I_6: channel punch-through current

  - Mainly due to sub-threshold leakage current (in cut-off region), which depends on channel doping concentration, length, Vt and T°
  - $P_{stat} = \sum_i V_{DD}. I_{SUB}$ where $I_{SUB} \propto V_{DD} / Vt$

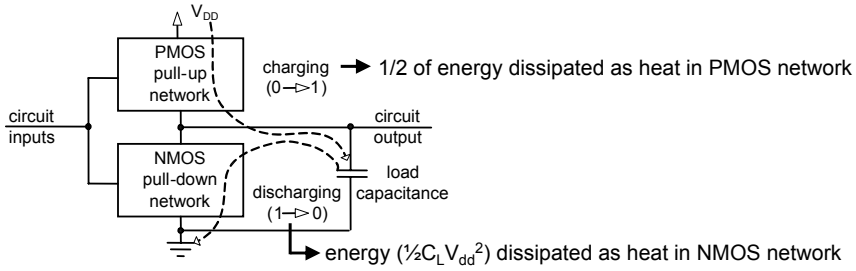
2. Power Issues during Test

2.1 Power and Energy Basics

- Dynamic Switching Power
  - Due to charge/discharge of load capacitance during switching

$$P_d = C_L V_{DD}^2 f_{0\to1}$$

where $f_{0\to1}$ is the number of output rising transitions per second

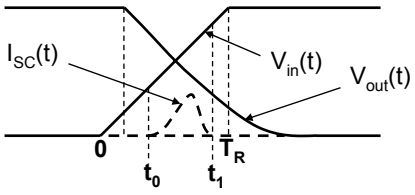


2. Power Issues during Test

2.1 Power and Energy Basics

- Dynamic Short-Circuit Power
  - Due to direct current path from V_{DD} to Gnd during output switching

$$P_{sc} = V_{DD} \int_{t_0}^{t_1} I_{sc}(\tau) d\tau / (t_1 - t_0)$$



  - $P_{SC} = \Sigma_i V_{DD}. I_{SC}$ with $I_{SC} \propto$ input_slew / C_{load}

2. Power Issues during Test

2.1 Power and Energy Basics

- Total Power Consumption

$$P_{total} = P_{stat} + P_d + P_{sc}$$

  - Switching power is still the main contributor, but leakage power may account for 25% in SoCs and 40% in high performance logic *
- Energy Dissipation
  - T is a given time period

$$E_{total} = \int_T P_{stat} d\tau + \int_T P_d d\tau + \int_T P_{sc} d\tau$$

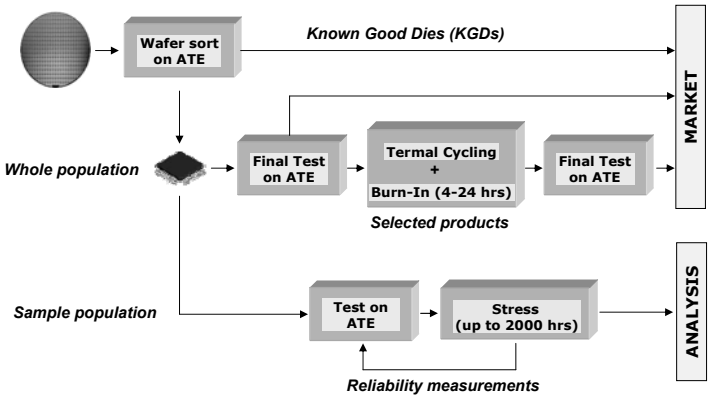
  - All power components are input state dependent !

* ITRS 2007

2. Power Issues during Test

2.2 Manufacturing Test Flow

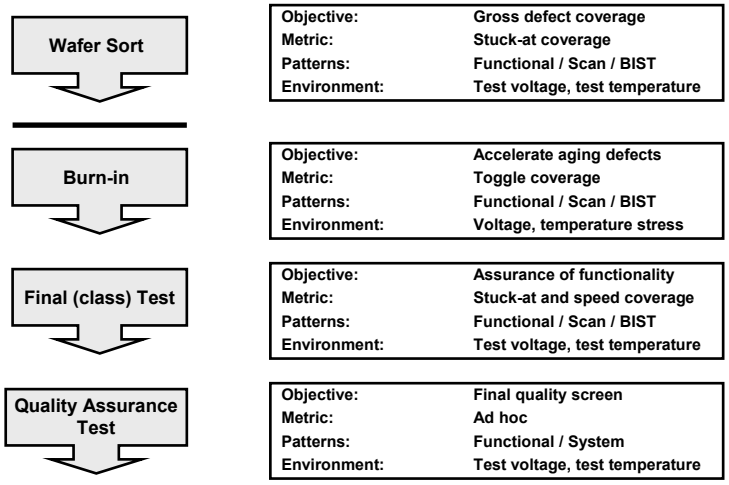
- A typical manufacturing test flow



(courtesy: Bernardi et al., ETS, 2009)

2. Power Issues during Test

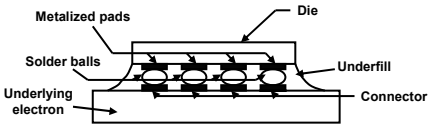
2.2 Manufacturing Test Flow

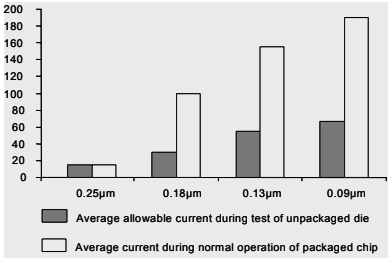


2. Power Issues during Test

2.3 Power Delivery Issues during Test

- Main packaging technologies
  - Wire-bonded packages
  - Flip-chip packages
- During wafer sort test
  - All power pads may not be contacted
  - Power delivery constraint arising out of this limitation is shown on the graph
  - A *larger inductance* on power delivery path is a second problem …



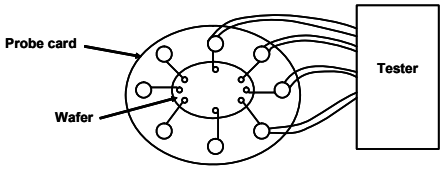


(Kundu et al., ITC, 2004)

2. Power Issues during Test

2.3 Power Delivery Issues during Test

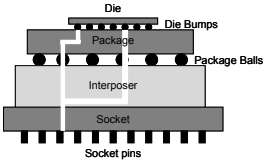
- Low-frequency power droop
  - Associated with inductance of off-chip power supply lines (L(di/dt))
  - Due to current variations (during switching) through inductive connections (ex.: connections from the tester to wafer metal pads)



- Depends on the level and change rate of current
- Can erroneously change the logic state of some circuit nodes or flip-flops, and cause test fail, thus leading to yield loss

2.3 Power Delivery Issues during Test

- **Mid-frequency power droop**
  - Associated with inductance at the package level (L(di/dt) event)
  - During execution of instructions, if power demand shifts from one area of the die to a different area, one area will experience a drop in voltage while the other will experience an increase voltage
  - These droops affect an entire region
  - Addressed at the functional level by introducing multiple sensors

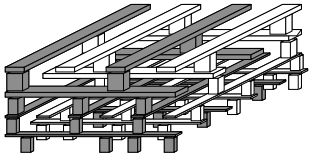


- MF power droop may lead to manufacturing yield loss if not properly addressed during test

2. Power Issues during Test

2.3 Power Delivery Issues during Test

- **High-frequency power droop**
  - Associated with the PDN on the die
  - Occurs when multiple cells drawing current from the same power grid segment suddenly increase their current demand. If the current cannot be provided quickly enough from other parts of the chip, power starvation results in a voltage drop
  - Handled in functional mode by adding a *frequency guard band*
  - A similar guard band is necessary during test mode

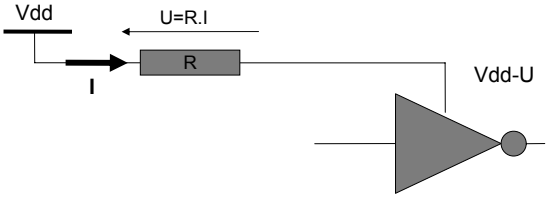


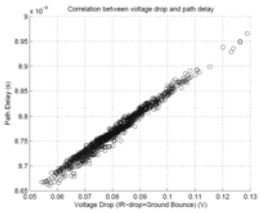
- May occur due to excess switching during at-speed scan test
- HF power droop may lead to manufacturing yield loss

2. Power Issues during Test

2.3 Power Delivery Issues during Test

• IR Drop refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a non negligible resistance between the rail and each node in the circuit under test





(Terhanipoor, WRTLT, 2008)

- With high peak current demands, gate voltages are reduced and gate delays increase
- IR Drop may lead to manufacturing yield loss

2. Power Issues during Test

2.4 Thermal Issues during Test

• Heat produced during the operation of a circuit is proportional to the dissipated power (Joule effect) and is responsible for die temperature increase

- $T_{die} = T_{air} + \theta \times P_{Average}$ where θ is the package thermal impedance

Elevated Average Power

↓

Temperature Increase

↓

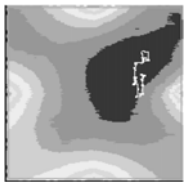
Excessive Heat Dissipation

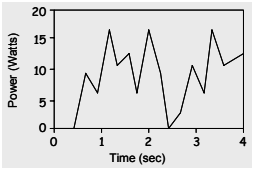
↓

Limits at-speed testing and concurrent testing due to thermal hot-spots

2.4 Thermal Issues during Test

- Thermal hot-spot results from localized overheating due to non-uniform spatial on-die power distribution
- Thermal hot-spot are likely to increase during package testing since test power dissipation can be high
- Main impact on the carrier's mobility $\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-k_1}$
- Slow down the device in the thermal hot-spot affected region of the chip
- Increase gate delays → yield loss
- May cause permanent damage !
  (Hot-Carrier-Induced Defects, Dielectric Breakdown)
- Arrange test patterns is a possible solution but it increases L(di/dt) !!





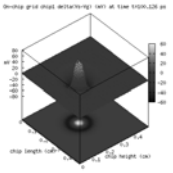
(Intel Technology Journal)

2.5 Test Throughput Problem

- Test throughput is defined as number of devices tested per test equipment over a given period
- Mainly due to:
  - Reduction in test frequency during package test (to avoid thermal or power delivery issues) or wafer sort test (due to limited power availability) that induces longer test time
  - Simultaneous testing of multiple cores placed in a SoC (to avoid thermal issues) is limited - longer test time

2. Power Issues during Test

2.6 Manufacturing Yield Loss



High Instantaneous Current

↓

Elevated Peak Power

↓

Power Supply Noise (IR-Drop, Ldi/dt)

↓

Significant Delay Increase due to Excessive PSN

↓

Erroneous Behavior Only During Testing (test fail)

↓

Manufacturing Yield Loss
(Over-Kill)

As huge designs can be manufactured today, most power-related test issues (during scan) are due to excessive peak power

2. Power Issues during Test

2.7 Test Power Metrics and Estimation

- Energy:
  - Total switching activity generated during test application
  - $E_{Total} = ½ \cdot c_0 . V^2_{DD} \cdot \sum_k \sum_i s_i(k) \cdot F_i$
  - $s_i(k)$ is the number of transitions provoked by V_k at node i
  - Impact the battery lifetime during power up or periodic self-test of battery operated devices
- Average Power:
  - Ratio between energy dissipated during test and test time
  - $P_{Average} = E_{Total} / (Length_{Test} \cdot T)$
  - Impact the thermal load of the device

2.7 Test Power Metrics and Estimation

- Instantaneous Power:
  - Power consumed at any given instant during test
- Peak Power:
  - Highest value of instantaneous power measured during test
  - $P_{Peak} = max_k\ P_{inst}(V_k) = max_k\ (\ E_{Vk}\ /\ t_{small}\ )$
  - Determines the thermal and electrical limits of components and the system packaging requirements
- Weighted Switching Activity (WSA):
  - $WSA_i = F_i\ .\ S_i$ where F_i is the fanout at node i and S_i is the switching activity factor (ave. # of transitions during a time interval)
  - Often used as a metric for test power evaluation

2. Power Issues during Test

2.7 Test Power Metrics and Estimation

- Impact of the various metrics:
  - The switching activity factor (s_i) affects E_{Total}, $P_{average}$ and P_{peak}
  - Clock frequency during test affects $P_{average}$ and P_{peak}
  - Test length affects E_{Total}
- Static power dissipation:
  - For a given technology, depends only on input patterns and T°
  - Static power dissipation is not a concern, except during during I_{DDQ} testing (reduced sensitivity) and during Burn-In test (can result in thermal runaway condition and yield loss)

2. Power Issues during Test

2.7 Test Power Metrics and Estimation

- Test power estimation:
  - Required for sign-off to avoid destructive testing and power-aware test space exploration during DfT or ATPG
  - Conventional flow adopted to perform test power estimation is simulation-based and performed at gate level
  - Estimation is performed at various PVT corners
  - Challenges for multi-million gate SoCs
    - ✓ Time-consuming
    - ✓ Memory sizes can be very large
  - The weigthed transition metric is quick but approximate

$$WeightedTransitions = \sum (ScanChainLength - TransitionPositionInVector)$$

3. Low-Power Test Pattern Generation

Part 2

Chapter 3

Low-Power Test Pattern Generation

3.1 Low-Power ATPG

Content

① **General Low-Power Test Generation**

② **Low-Shift-Power Scan Test Generation**

③ **Low-Capture-Power Scan Test Generation**
- Capture-Safety Checking
- LCP ATPG Technique: Reversible Backtracking

3.1 Low-Power ATPG

General Low-Power Test Generation

- Goal: To create a sequence of test vectors that cause a minimal number of transitions at inputs between any two consecutive cycles.
- Method: Modify PODEM with new cost functions.

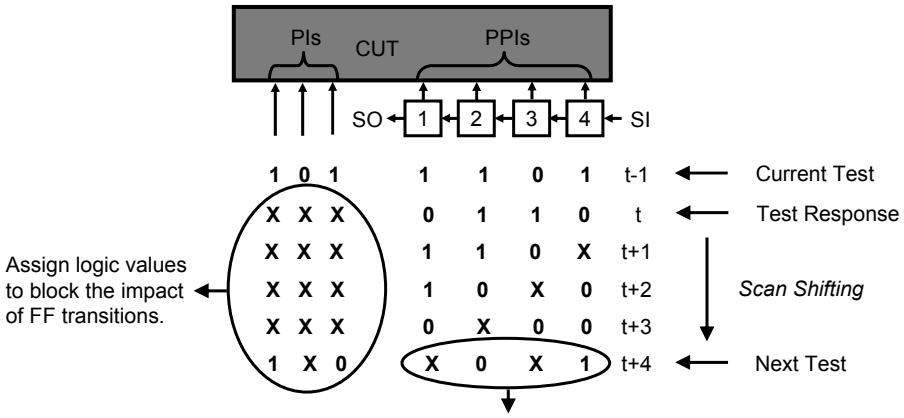
For each line *l* in a circuit and each logic value *s*, calculate:

- **Transition Controllability** *TCs*(*l*) to reflect the minimum numbers of weighted transitions required to set *l* to *s*.
  ➔ *Use TC to guide backtrace*
- **Transition Observability** *TOs*(*l*) to reflect the minimum numbers of weighted transitions required to propagate a fault effect (the corresponding fault-free value of which is *s*) from *l* to a primary output.
  ➔ *Use TO to guide D-frontier selection*
- **Transition Test Generation Cost** *TCs*(*l*) (= *TCs*(*l*) + *TOs*(*l*)) to reflect the transition level required to detect the stuck-at-$\bar{s}$ fault at *l*.
  ➔ *Use TC to guide target fault selection*

(*S. Wang et. al., IEEE Trans. on Computers, Vol. 47, No. 2, pp. 256–262, 1994*)

3.1 Low-Power ATPG

Low-Shift-Power Scan Test Generation



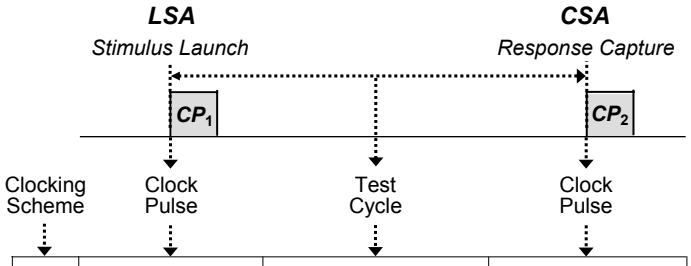
- Use modified PODEM to maximize the # of *X*s.
- Assign logic values to minimize FF transitions.

(*S. Wang et. al., Proc. DAC, pp. 614-619, 1997*)

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

Capture Operation in At-Speed Scan Testing



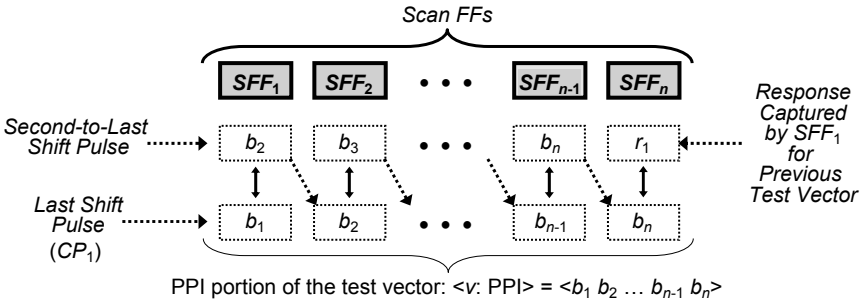
LOS	*last shift pulse*	*= functional cycle*	*capture pulse*
LOC	*1st capture pulse*	*= functional cycle*	*2nd capture pulse*

- LOS (Launch-on-Shift): easy ATPG (high coverage) but hard physical design
- LOC (Launch-on-Capture): easy physical design but hard ATPG (low coverage)
- LSA (Launch Switching Activity): affect timing / a more serious problem
- CSA (Capture Switching Activity): may cause FF malfunction / but may be rare

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

LOS-Type LSA Reduction in At-Speed Scan Testing

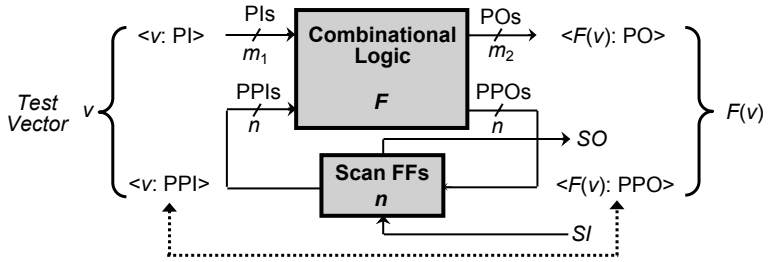


- LOS-type LSA for <*v*: PPI> = <*b*1 *b*2 … *bn*-1 *bn*> is dominated by $\Sigma(bi\text{-}1 \oplus bi)$ for $i = 2, \ldots, n$.
- LOS-type LSA can be readily reduced by minimizing the difference between neighbouring bits in <*v*: PPI>.
- *0-fill*,*1-fill*, etc. can be used for reducing LOS-type LSA.

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

LOC-Type LSA Reduction in At-Speed Scan Testing



- LOC-type LSA is dominated by $\Sigma(<v\text{: PPI}> \oplus <F(v)\text{: PPO}>)$.
- Test responses must be considered in order to reduce LOC-type LSA.
  ➔ *LOC-type LSA is hard to reduce than LOS-type LSA*

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

Overview of Capture-Safety Checking

- Not all test vectors generated by conventional ATPG, which does not try to minimize test power, suffer from excessive LSA.
- Capture-safety checking metrics are needed to judge if a test vector will cause any problem in capture mode due to excessive LSA.

- Non-Simulation-Based Metric
  - ➔ *FLIS*
- Simulation-Based Metrics
  - ➔ *Toggle*
  - ➔ *WSA*
- Region-Based Metrics
  - ➔ *Toggle-Based*
  - ➔ *WSA-Based*
- Timing-Based Metrics
  - ➔ *SCAP*
  - ➔ *CCT*

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

Simulation-Based Capture-Safety Checking Metrics

Toggle Count

- Calculated as the number of transitions in the whole circuit or a region.
- Logic simulation can be conducted with a zero-delay, a unit-delay, or even a timing model, resulting in trade-off between accuracy and CPU time.

WSA (Weighted Switching Activity)

- Calculated as the number of weighted transitions in the whole circuit or a region.
- Ideally, the weight of a node should be set to reflect its output capacitance.
- In practice, the weight of a node is often set as the number of its fanouts or the number of its fanouts plus 1.

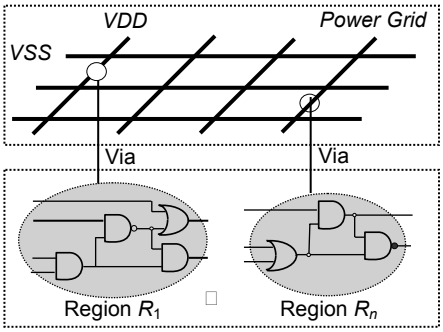
(*S. Wang et. al., Proc. ITC, pp. 250-258, 1994*)

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

Region-Based Capture-Safety Checking Metrics

- The Impact of switching activity is local and depends on power grid design.
- A circuit is divided into regions, bounded by power straps or with intersections of power straps as midpoints.



(*V. Devanathan et. al., Proc. ITC, Paper 13.1, 2007*) (*J. Lee et. al., Proc. DATE, pp. 1172-1177, 2008*)

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

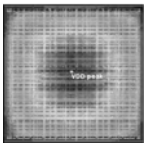
Region-Based Capture-Safety Checking Metrics

Toggle-Based-Metric

GTC (*Global Toggle Count*)
➔ *transitions in all regions throughout the test cycle*

GITC (*Global Instantaneous Toggle Count*)
➔ *transitions at any time instant in all regions*

RITC (*Regional Instantaneous Toggle Count*)
➔ *transitions at any time instant in a specific region*



50	50	50	50
50	45	45	50
50	45	45	50
50	50	50	50

WSA-Based Metric

$$WSA_{ij}(v) = \sum_{k \in R(i,j)} (t_k \times (g_{w_k} + f_k \times f_{w_k}))$$

gwk is the weight of gate *k* in *R*(*i*, *j*), *fk* is the number of its fanouts, *fwk* is its fanout load weight, and *tk* is 1 (0) if a transition occurs (does not occur) at gate *k*.

(*V. Devanathan et. al., Proc. ITC, Paper 13.1, 2007*) (*J. Lee et. al., Proc. DATE, pp. 1172-1177, 2008*)

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

LCP ATPG Technique: Reversible Backtracking

[Basic Concept]

D-Conflict

Current input assignments are found to be unable to detect the target fault.

↓

Conventional Backtrack

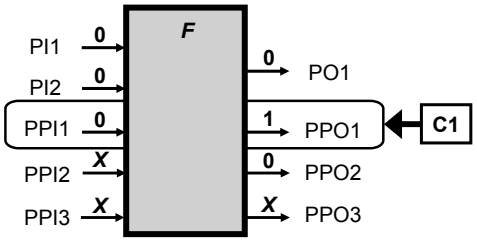
Ci-Conflict

Current input assignments cause different logic values between PPI*i* and PPO*i*.

↓

Reversible Backtrack

(Backtrack decision is reversed if it cause a fault to become undetected.)



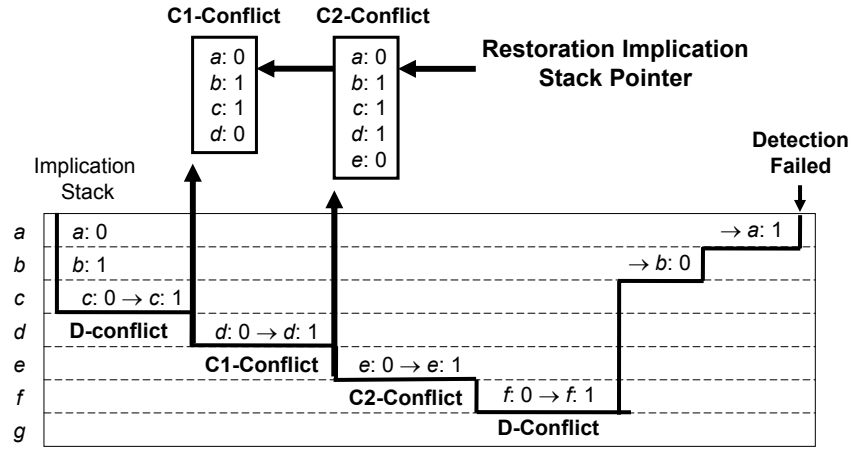
(*X. Wen et. al., Proc. VTS, pp. 58-63, 2006*)

3.1 Low-Power ATPG

Low-Capture-Power Scan Test Generation

LCP ATPG Technique: Reversible Backtracking

[Collecting Restoration Information]



(*X. Wen et. al., Proc. VTS, pp. 58-63, 2006*)

3.2 Low-Power Test Compaction

Content

① **Low-Shift-Power Static Dynamic Compaction**

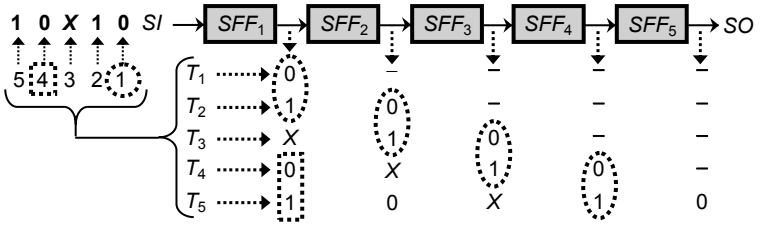
② **Low-Capture Static Compaction**

3.2 Low-Power Test Compaction

Low-Power Static Compaction

Low-Shift-Power Static Compaction

- Transitions at different bit positions in a test cube have different degrees of impact on shift-in power.



- The cost of merging two test cubes can be assessed by *Weighted Transitions*:

$$Weighted\_Transitions = \sum (Scan\_Chain\_Length - Transition\_Position)$$

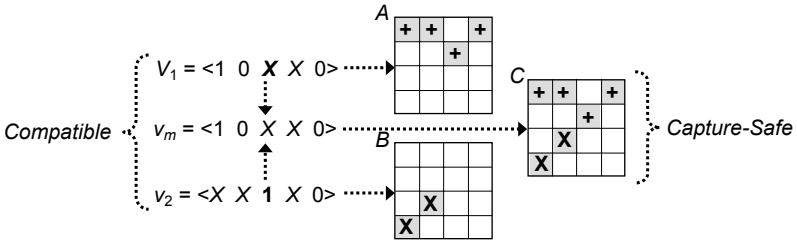
(*R. Sankaralingam et. al., Proc. VTS, pp. 35-40, 2000*)

3.2 Low-Power Test Compaction

Low-Power Static Compaction

Low-Capture-Power Static Compaction

- The goal is to evenly distribute the LSA of a test vector across the entire chip rather than allowing high LSA to occur in a small area.
- The chip is divided into regions, and the extended WSA metric is used to calculate the LSA profile for each region.



- Test cubes *v*1 and *v*2 are compatible. Since there is no overlapping of risky regions of their LSA profiles, the resulting merged test cube *vm* is capture-safe.

(*J. Lee et. al., Proc. VTS, pp. 227-232, 2008*)

3.3 Low-Power *X*-Filling

Outline

Low-Shift-Power *X*-Filling		
Shift-In Power Reduction	Shift-Out Power Reduction	Total Shift Power Reduction
0-fill *1-fill* *MT-fill* *adjacent fill / repeat fill*	*output-justification-based X-filling*	*MTR-fill*
Low-Capture-Power *X*-Filling		
FF-Oriented	Node-Oriented	Critical-Area-Oriented
PMF-fill *LCP-fill* *preferred fill* *JP-fill* *CTX-fill*	*PWT-fill* *state-sensitive X-filling*	*CCT-fill*
Low-Shift-and-Capture-Power *X*-Filling		
impact-oriented X-filling	*hybrid X-filling*	*bounded adjacent fill*
Low-Power *X*-Filling for Compressed Scan Testing		
0-fill	*PHS-fill*	*CJP-fill*

3.3 Low-Power *X*-Filling

Content

① Test Cube Preparation
- Direct Generation
- Test Relaxation

② Low-Shift-Power *X*-Filling
- Shift-In Power Reduction
- Shift-Out Power Reduction
- Total Shift Power Reduction

③ Low-Capture-Power *X*-Filling
- FF-Oriented *X*-Filling

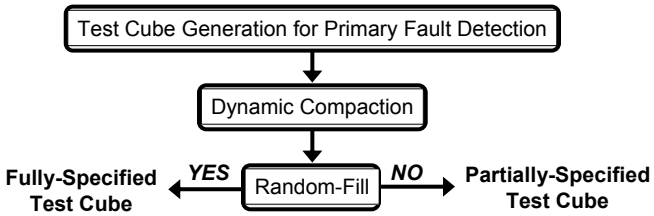
④ Low-Shift-and-Capture-Power *X*-Filling
- Bounded Adjacent Fill

⑤ Low-Power *X*-Filling for Compressed Scan Testing
- *X*-Filling in Broadcast-Based Test Compression
- *X*-Filling for Linear Decompressor-Based Test Compression

3.3 Low-Power *X*-Filling

Test Cube Generation

Direct Generation



- Random-fill increases the chances of accidental detection, resulting in smaller test vector count.
- Disabling random-fill may increase test vector count.
  → *For 7 industrial circuits (229K ~ 2.01M), test vector count increased by 144.8% on average when random-fill was not conducted*

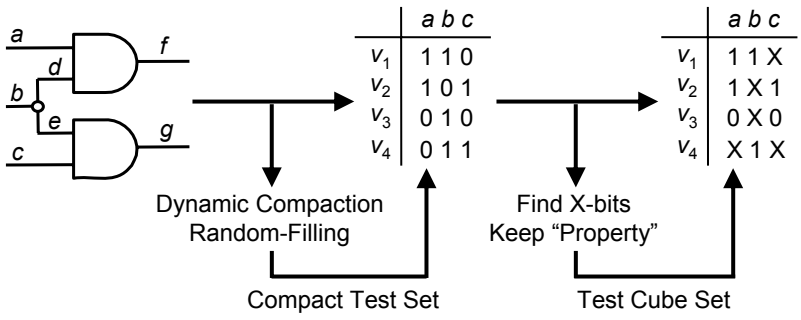
(*K. Butler et. al., Proc. ITC, pp. 355-364, 2004*)
(*N. Ahmed et. al., Proc. DAC, pp. 533-538, 2007*)
(*S. Romersaro et. al., Proc. ITC, Paper 32.2, 2006*)

3.3 Low-Power *X*-Filling

Test Cube Generation

Test Relaxation

[Concept]



- "Property" is usually the fault coverage for various fault models.
- Fault simulation, justification, and implication are used to find *X*-bits.
- 60%-80% of bits in a compact test set are usually identified as *X*-bits.

3.3 Low-Power *X*-Filling

Test Cube Generation

Test Relaxation

[Basic Procedure]

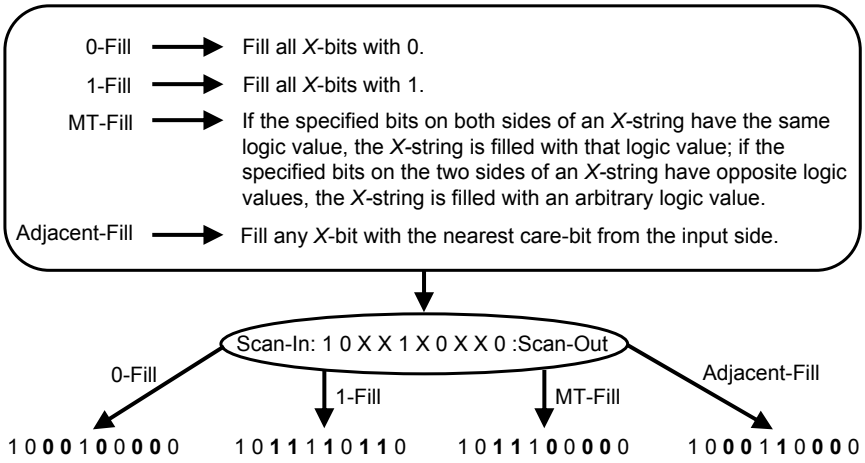
```
Procedure XID (C, T)
C: circuit model;
T: initial test vector set;
{
  /* Pass-1 */
  for each test vector v_i in T {
    EF = find_essential_fault (v_i);          /* Step-1 */
    initial_c_i = create_test_cube (EF);      /* Step-2 */
    3_valued_fault_simulation (initial_c_i);  /* Step-3 */
  }
  /* Pass-2 */
  for each test vector t_i in T {
    UF = find_undetected_fault (v_i, c_i);    /* Step-4 */
    final_c_i = adjust_test_cube (UF);        /* Step-5 */
    3_valued_fault_simulation (final_c_i);    /* Step-6 */
  }
}
```

(*K. Miyase et. al., IEEE Trans. on CAD, Vol. 29, No. 6, pp. 321-326, 2004*)

3.3 Low-Power *X*-Filling

Low-Shift-Power *X*-Filling

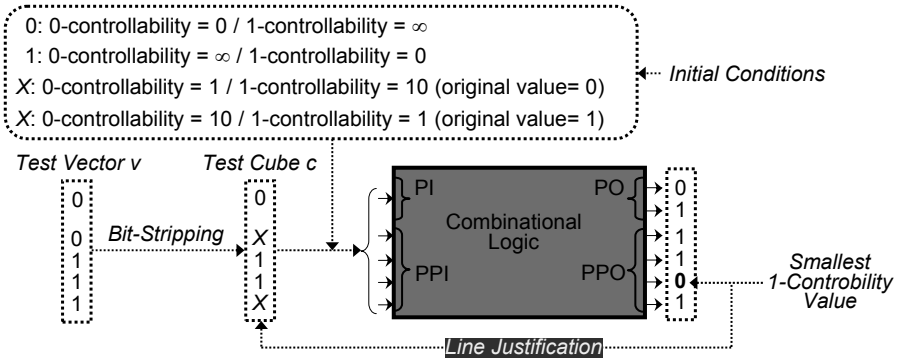
Shift-In Power Reduction



3.3 Low-Power *X*-Filling

Low-Shift-Power *X*-Filling

Shift-Out Power Reduction



- Create a test cube from a test vector by bit-stripping.
- Use justification to change values for some bits in the test response so as to reduce shift-out power.

(*R. Sankaralingam et. al., Proc. VTS, pp. 153-159, 2002*)

3.3 Low-Power *X*-Filling

Low-Shift-Power *X*-Filling

Total Shift Power Reduction

- Use a metric to estimate the total shift (shift-in and shift-output) switching activity.
- *TWTM* (*Total Weighted Transition Metric*)

$$TWTM(t_i, r_i) = \sum_{j=1}^{L-1} (t_{i,j} \otimes t_{i,j+1}) \times j + \sum_{j=1}^{L-1} (r_{i,j} \otimes r_{i,j+1}) \times j$$

Shift-In (Test Vector) Switching Activity Estimate

Shift-In (Test Response) Switching Activity Estimate

- MTR-fill (Minimum Transition Random *X*-filling)
  - ➔ First, fill a test cube *ci* with *n X*-bits by MT-fill to create an solution test vector *ti*.
  - ➔ Then, flip the *n* X-bit positions in *ci,* one by one, to see if it results in a test vector of a smaller TWTM. If so, replace *ti* by the test vector.

(*D. Song et. al., IEICE Trans on Information & System, Vol. E91-D, No. 4, pp. 1197-1120, 2008*)

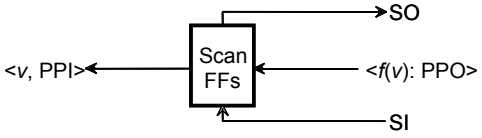
3.3 Low-Power *X*-Filling

Low-Capture-Power *X*-Filling

FF-Oriented X-Filling

[Basics]

- The basic idea is FF-silencing, i.e., trying to equalize the input and output of an FF.



- There are four types of PPI-PPO bit pairs.

Bit *p* in <*v*, PPI> \ Bit *q* in <*f*(*v*): PPO>	0 or 1	*X*
0 or 1	*Type-A*	*Type-C*
X	*Type-B*	*Type-D*

- Different FF-oriented *X*-filling methods handle Type-B, Type-C, and Type-D pairs differently.

(*X. Wen et. al., Proc. VTS, pp. 265-270, 2005*)

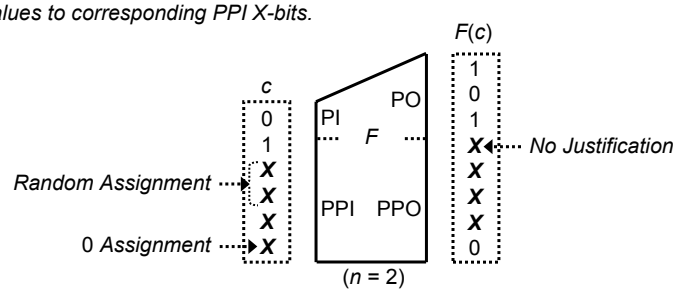
3.3 Low-Power *X*-Filling

Low-Capture-Power *X*-Filling

FF-Oriented X-Filling

[Random FF-Silencing]

- PMF-Fill (Progressive Match Filling):
  - ➔ *Use assignment for Type-B bit-pairs.*
  - ➔ *Use justification for Type-C bit-pairs.*
  - ➔ *Randomly select n Type-D bit-pairs, and randomly assign logic values to corresponding PPI X-bits.*



- A smaller *n* leads to a more effective reduction but at the cost of a longer execution time.

(*W. Li et. al., Proc. IEEE Annual Symp. on VLSI, pp. 151-161, 2005*)

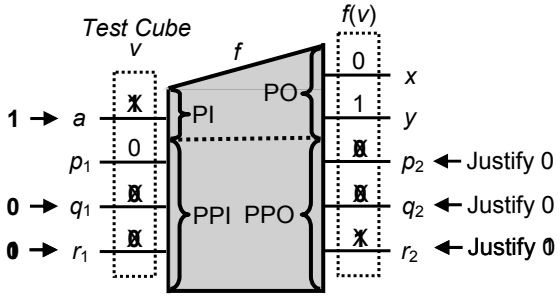
3.3 Low-Power *X*-Filling

Low-Capture-Power *X*-Filling

FF-Oriented X-Filling

[Justification-Based FF-Silencing]

- LCP-Fill (Low-Capture Power *X*-Filling):



- Highly effective due to the use of deterministic ATPG techniques.
- Relatively long CPU time due to multi-pass processing.

(*X. Wen et. al., Proc. VTS, pp. 265-270, 2005*)

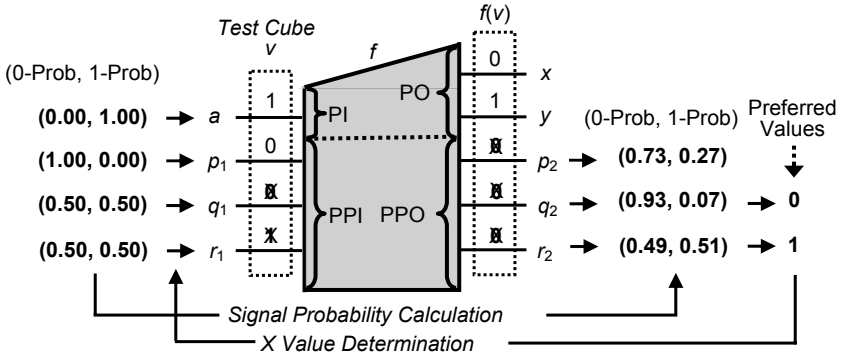
3.3 Low-Power *X*-Filling

Low-Capture-Power *X*-Filling

FF-Oriented X-Filling

[Probability-Based FF-Silencing]

- Preferred Fill:



- Relatively short CPU time due to single-pass processing.
- Effectiveness depends on the accuracy of probability calculation.

(*S. Romersaro et. al., Proc. ITC, Paper 32.2, 2006*)

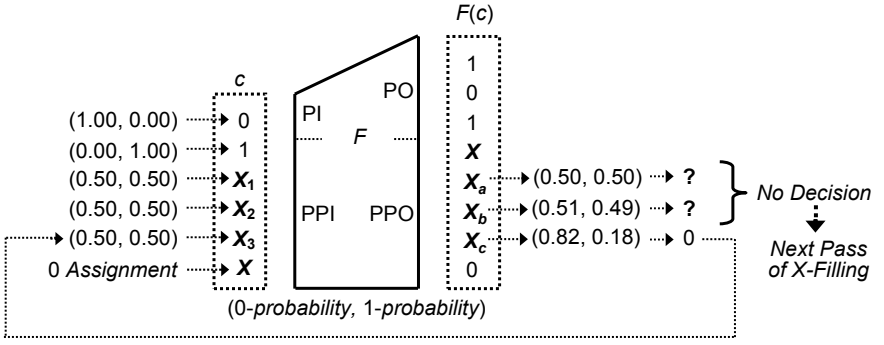
3.3 Low-Power *X*-Filling

Low-Capture-Power *X*-Filling

FF-Oriented X-Filling

[Justification-Probability-Based FF-Silencing]

- JP-Fill (Justification-Probability-Based *X*-Filling):



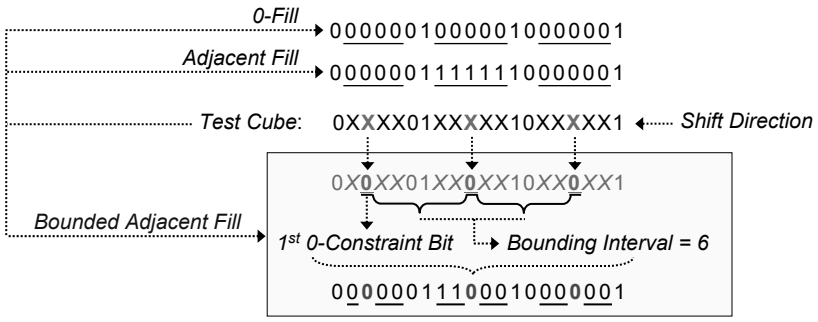
- Use justification and multiple passes to improve its effectiveness.
- Use probability-based parallel logic value determination to improve its scalability.

(*X. Wen et. al., Proc. ITC, Paper 25.1, 2007*)

3.3 Low-Power *X*-Filling

Low-Shift and-Capture-Power *X*-Filling

Bounded Adjacent Fill



- The basic idea is to first set several *X*-bits in a test cube to 0 and then conduct *adjacent fill*.

➔ *The occurrence of 0 in the resulting fully-specified test vector is increased, which helps reduce shift-out and capture power.*

➔ *At the same time, applying adjacent fill helps reduce shift-in power.*

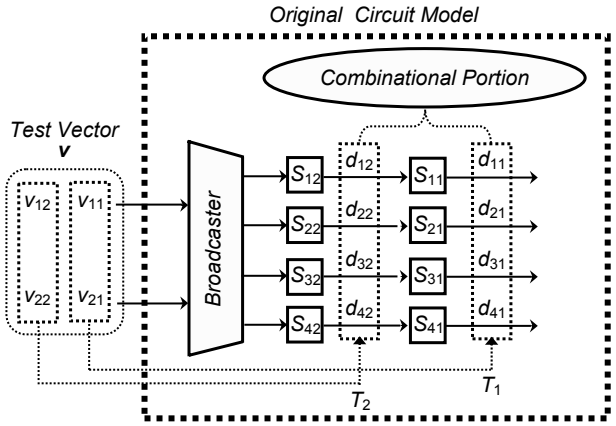
(*A. Chandra et. al., Proc. VTS, pp. 131-138, 2008*)

3.3 Low-Power *X*-Filling

Low-Power *X*-Filling for Compressed Scan Testing

X-Filling in Broadcast-Based Test Compression

[Original Circuit]



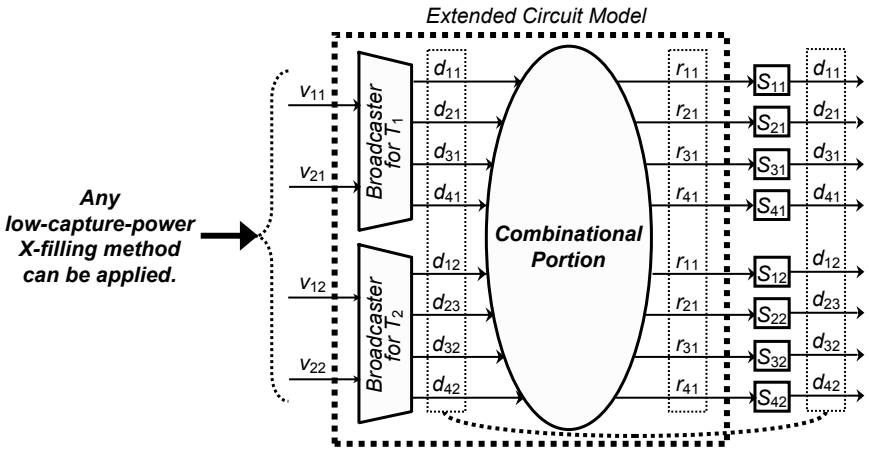
(*K. Miyase et. al., Proc. ICCAD, 2009*)

3.3 Low-Power *X*-Filling

Low-Power *X*-Filling for Compressed Scan Testing

***X*-Filling in Broadcast-Based Test Compression**

[Circuit Model]



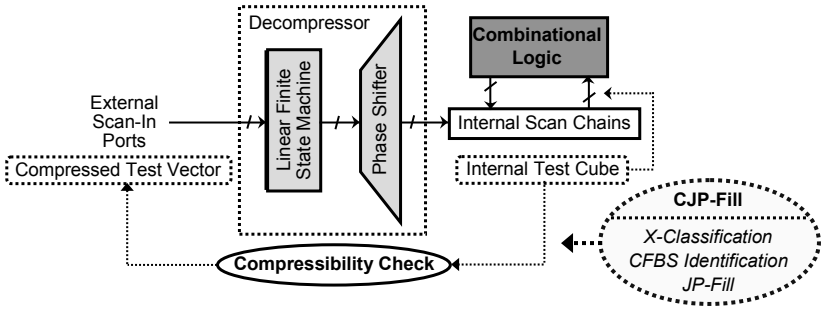
(*K. Miyase et. al., Proc. ICCAD, 2009*)

3.3 Low-Power *X*-Filling

Low-Power *X*-Filling for Compressed Scan Testing

***X*-Filling for Linear Decompressor-Based Test Compression**

- CJP-Fill (Compressible JP-Fill):



- ***X*-classification** is to separate **implied *X*-bits** (which must have certain logic values) from **free *X*-bits** (which can have any logic values, provided that they are filled one at time).
- ***Compatible free bit set*** (CFBS) identification is to find a set of free *X*-bits that can be filled with any logic values simultaneously without affecting compressibility.

(*M. Wu et. al., Proc. ITC, Paper 13.1, 2008*)

3.4 Low-Power Test Ordering

Content

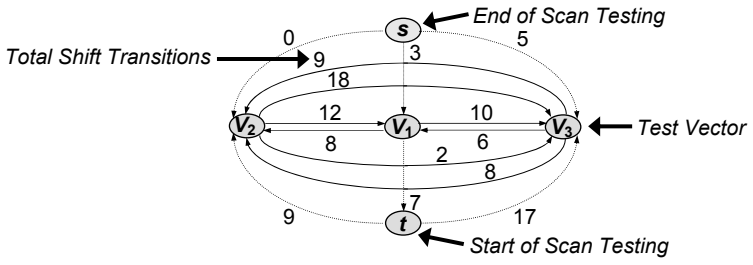
① **Internal-Transition-Based Ordering**

② **Inter-Vector-Hamming-Distance-Based Ordering**

3.4 Low-Power Test Ordering

Internal-Transition-Based Ordering

- Guide test vector ordering by transitions at internal nodes (FFs and/or gates).
- A complete graph, called transition graph (TG), is used to represent transitions.



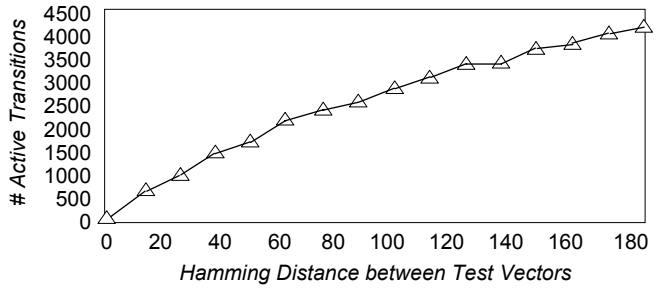
- A optimal test vector order is obtained by finding a node sequence with the smallest edge-weight sum.
  ➔ *NP-complete traveling salesman problem*
- A good test vector order is obtained by finding a Hamiltonian path with the smallest edge-weight sum.
  ➔ *Time complexity: $O(n^2 \log n)$*

(*S. Chakravarty et. al., Proc. ATS, pp. 324-329, 1994*)

3.4 Low-Power Test Ordering

Inter-Vector-Hamming-Distance-Based Ordering

- Building a TG needs $n \times (n - 1)$ logic simulations for a circuit of n nodes, which can be prohibitively time-consuming for a large circuit.
- Using the Hamming distance between Vi and Vj as the weight of the edge from Vi to Vj will greatly reduce the CPU time needed for building a TG.
- There is a good correlation between Hamming distance and circuit activity.



(*P. Girard et. al., Proc. ISCAS, pp. 296-299, 1998*)

3.5 Low-Power Memory Test Generation

Content

① **Address Switching Activity Reduction**

② **Precharge Restriction**

3.5 Low-Power Memory Test Generation

Address Switching Activity Reduction

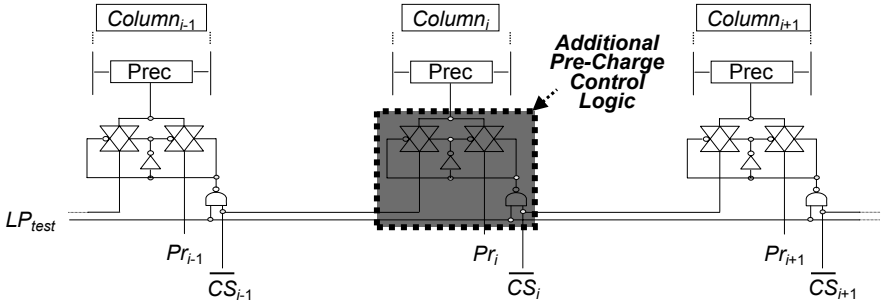
	Original Test Algorithm	Low-Power Test Algorithm
Zero-One	↕ (W0); ↕ (R0); ↕ (W1); ↕ (R1);	$\updownarrow_s$ (W0, R0, W1, R1);
Checker Board	↕ (W($1_{odd}/0_{even}$)); ↕ (R($1_{odd}/0_{even}$)); ↕ (W($0_{odd}/1_{even}$)); ↕ (R($0_{odd}/1_{even}$));	$\updownarrow_s$ (W($1_{odd}/0_{even}$), R($1_{odd}/0_{even}$), -W($0_{odd}/1_{even}$),R($0_{odd}/1_{even}$));

- Reorder test patterns to minimize switching activity on address lines without any fault coverage loss.
- Original test algorithm's addressing order: ↕
- Low-power test algorithm's addressing order: $\updownarrow_s$ (*single bit change*)
  Example: **00 → 0<u>1</u> → <u>1</u>1 → 1<u>0</u>**

(*H. Cheung et. al., Proc. ITC, pp. 22-32, 1996*)

3.5 Low-Power Memory Test Generation

Precharge Restriction



- Precharge circuitry in SRAM precharges and equalizes long and high capacitive bit lines for correct memory operations, and may take 70% of power dissipation.
- The test addressing sequence is fixed, and there is no need to precharge all columns.
- Add to precharge control logic (MUX + NAND) to precharge only the current column and the next column to be accessed.

(*P. Dilillo et. al., Proc. DATE, pp. 1159-1165, 2006*)

Chapter 4

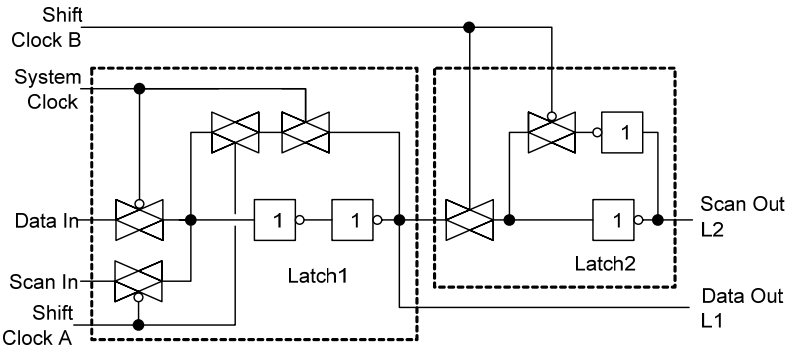
Power-Aware Design-for-Test

4.1 Overview of Power-Aware DFT

- Low-power scan cells
- Scan path organization
- Partitioning for low power

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

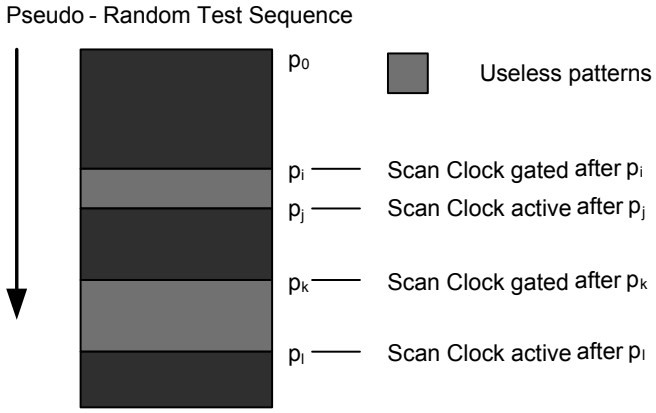


- Level sensitive scan design (LSSD) cell
  - Non-overlapping clocks
  - Robustness against shift-power violations

(*Stojanovic and Oklobdzija., JSSCC, pp. 536□548, 1999.*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

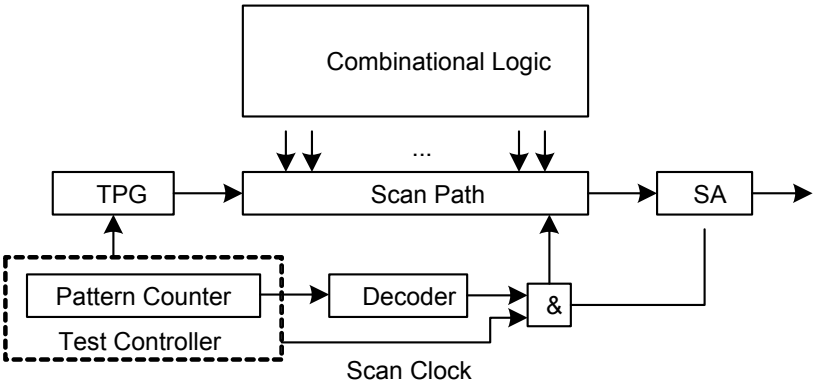


- Useless patterns do not detect any faults
  - Pattern suppression
  - Deactivate scan clocks when no fault coverage improvement

(*P. Girard et al., Proc. VTS, pp. 407-412, 1999.*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating



- Decoder used for pattern suppression
  - Fault simulation
  - Logic minimization

(*S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

index	binary	# faults
0	0000	17
1	0001	9
2	0010	4
3	0011	0
4	0100	5
5	0101	2
6	0110	3
7	0111	0

index	binary	#faults
8	1000	2
9	1001	0
10	1010	0
11	1011	1
12	1100	0
13	1101	0
14	1110	0
15	1111	0

```
{0000 , 0001 , 0010 , 0100 , 0101,
 0110 , 1000 , 1011 , 1100}
```
on-set

```
{0011 , 0111 , 1001 , 1010}
```
off-set

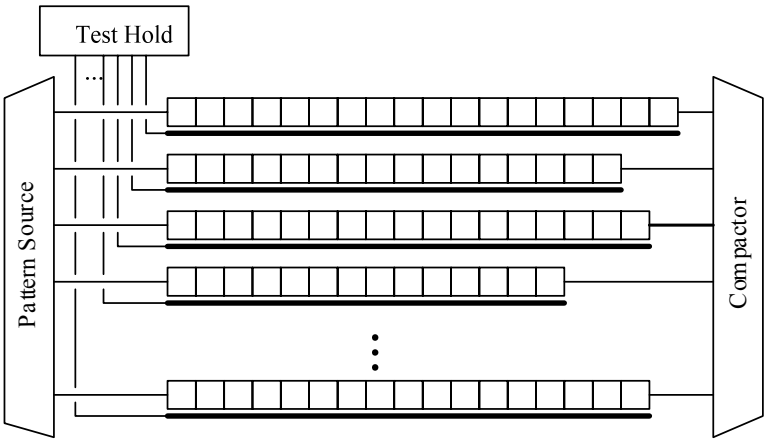
```
{1101 , 1110 , 1111}
```
dc-set

Implementing the pattern decoder

(*S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

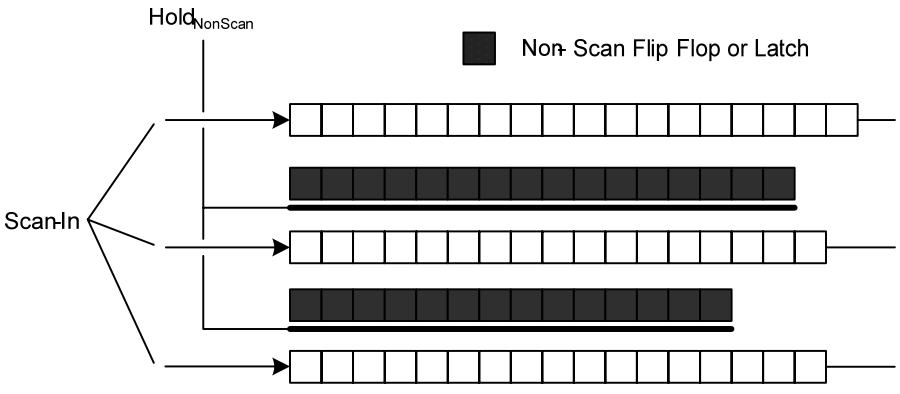


- DFT with parallel scan chains
  - Clock gating per chain (for better granularity)
  - Test hold register and local clock buffers

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

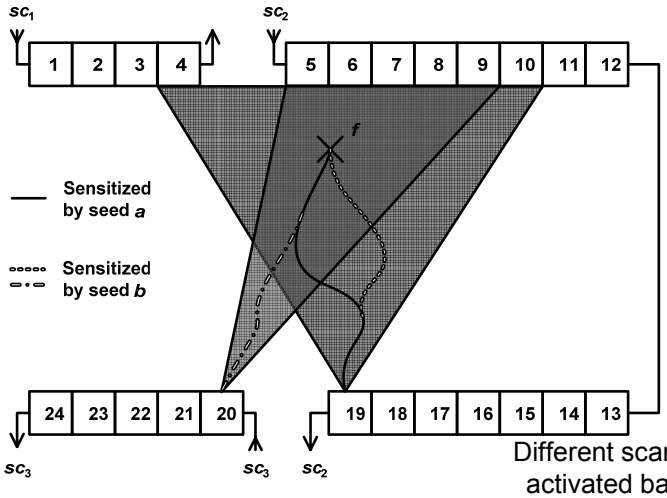


- Partial scan
  - Disable clocks on non-scan flip-flops or latches

(*C. Zoellin et al., Proc. ITC, paper 32.3, 2006*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

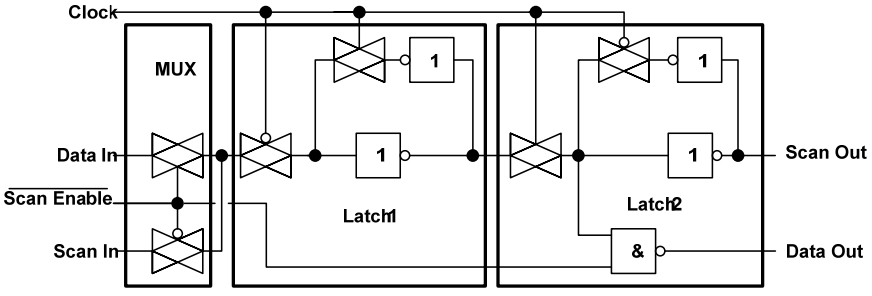


Different scan chains can be activated based on multiple sensitizations of the same fault

(*C. Zoellin et al., Proc. ITC, paper 32.3, 2006*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

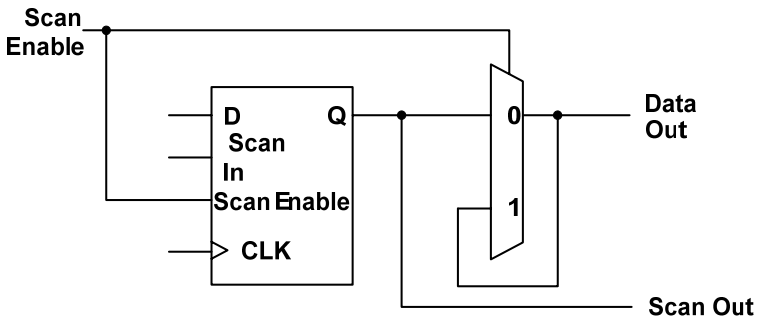


- Toggle suppression during shift
  - Master-slave structure of a mux-D flip-flop is modified
  - Gate the data output during shift

(*A. Hertwig and H.-J. Wunderlich, Proc. ETW, pp. 49-53, 1998*)

4. Power-Aware Design-for-Test

4.2 Low-power scan cells / clock gating

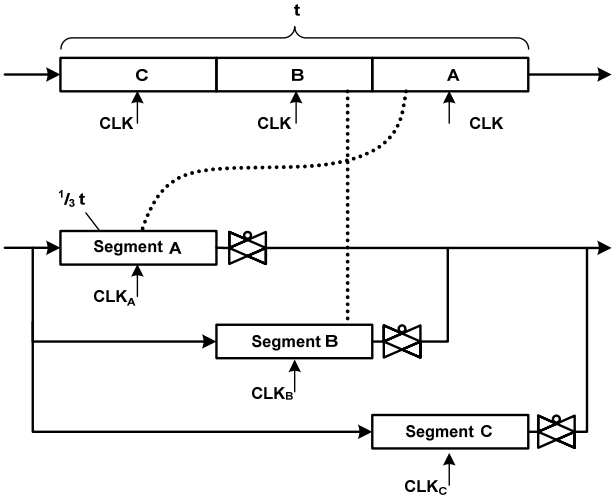


A different implementation of toggle suppression during shift using a latch at the output of the mux-D flip-flop with scan

(*X. Zhang and K. Roy., Proc. IOLTW, pp. 133-138, 2000*)

4. Power-Aware Design-for-Test

4.3 Scan path organization

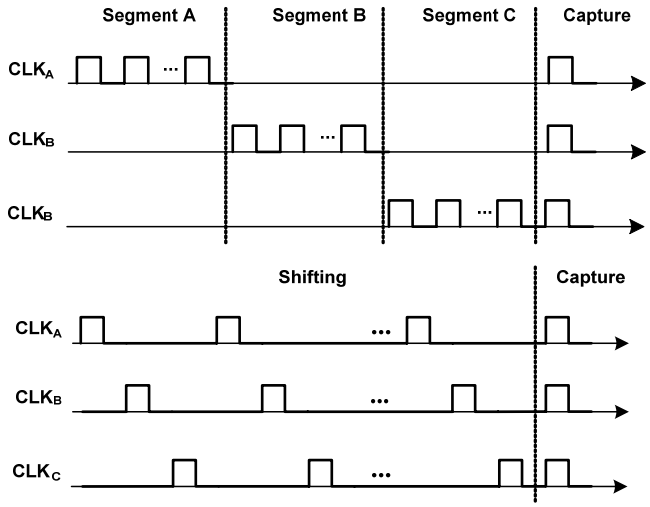


Only one scan segment is activated at a time

(*L. Whetsel, Proc. ITC, pp. 853-872, 2000*)

4. Power-Aware Design-for-Test

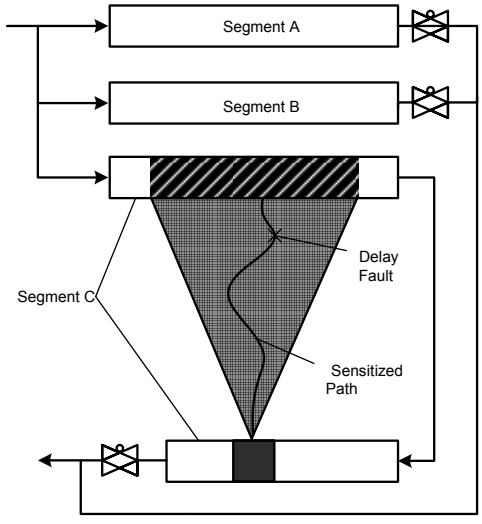
4.3 Scan path organization



(*L. Whetsel, Proc. ITC, pp. 853-872, 2000*) and (*Y. Bonhomme et al, Proc. ATS, pp. 253-258, 2001*)

4. Power-Aware Design-for-Test

4.3 Scan path organization

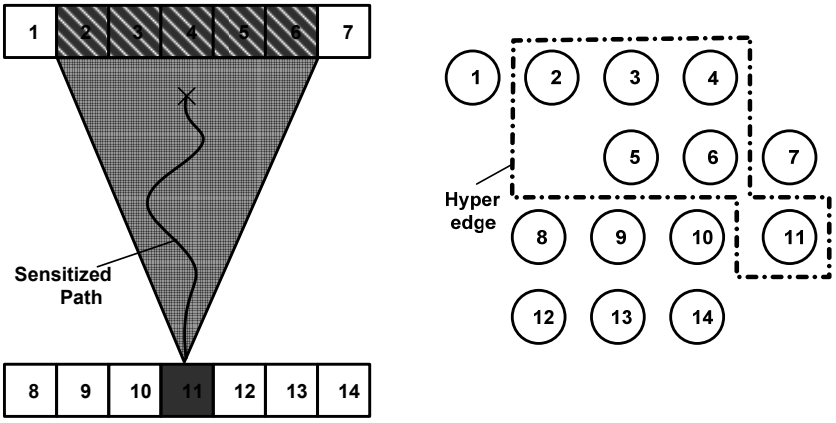


- Scan segmentation
- Partitioning scan cell in multiple scan chains such that only one of them is activated at a time
- Applicable also launch-off-shift and launch-off-capture

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.3 Scan path organization

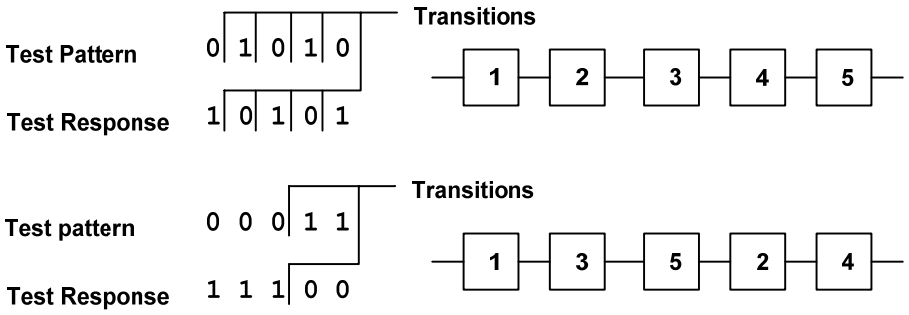


• Scan cell clustering using hyper-graph partitioning

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.3 Scan path organization

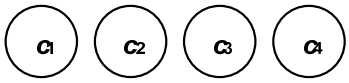


• Scan cell order and its influence on the number of transitions

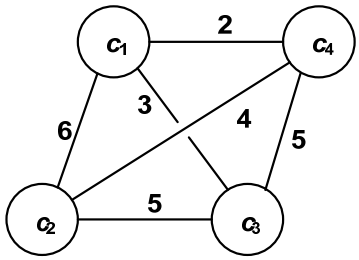
(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.3 Scan path organization



v_1 =	1	0	0	1
r_1 =	0	1	0	0
v_2 =	0	1	0	1
r_2 =	0	0	1	0
v_3 =	1	1	1	1
r_3 =	1	0	1	1
v_4 =	1	0	1	0
r_4 =	1	0	0	1

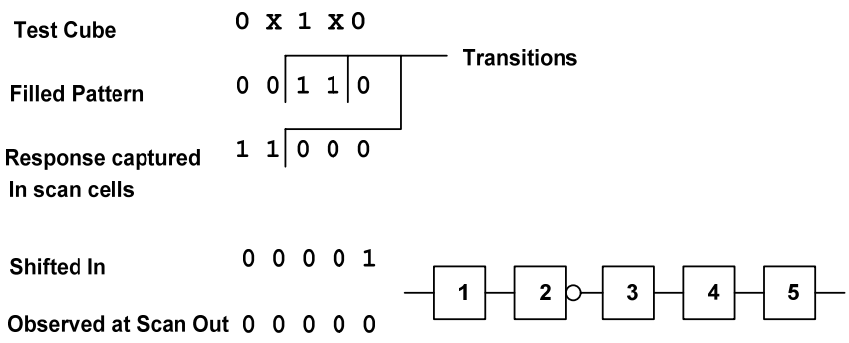


Using vectors and responses to compute edge weights before tackling scan cell ordering through the travelling salesman problem

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.3 Scan path organization

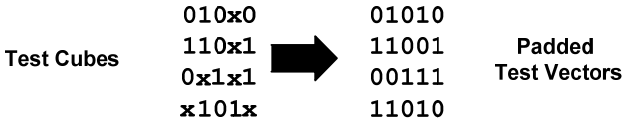


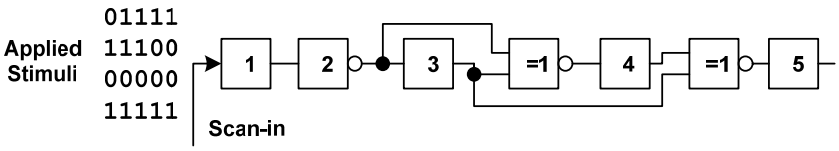
Inserting logic into scan chains to modify the transition count during shift

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.3 Scan path organization



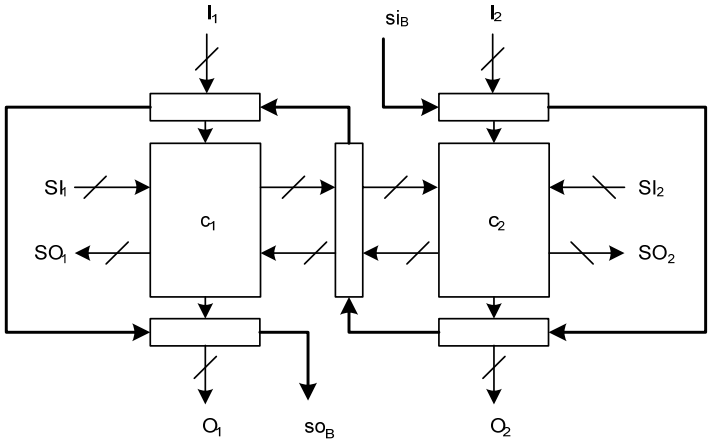


Scan segment inversion by embedding a linear function in the scan path

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ Stuttgart)

4. Power-Aware Design-for-Test

4.4 Partitioning for low-power



Isolating multiple cores of logic using boundary registers

(*P. Girard et. al., Proc. ITC, pp. 652-661, 2000*)

Chapter 5

Power-Aware BIST and Test Data Compression

5.1 Overview of power-aware BIST and compression

- Coding-based compression methods
- LFSR-decompression-based compression methods
- Low-power BIST techniques

5.2 Coding-based compression

Group	Run-Length	Group Prefix	Tail	Codeword
A_1	0	0	00	000
	1		01	001
	2		10	010
	3		11	011
A_2	4	10	00	1000
	5		01	1001
	6		10	1010
	7		11	1011
A_3	8	110	00	11000
	9		01	11001
	10		10	11010
	11		11	11011

Golomb code

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ)

5. Power-Aware BIST and Test Data Compression

5.2 Coding-based compression

Group	Run-Length	Group Prefix	Tail	Codeword
A_1	0	0	0	00
	1		1	01
A_2	2	10	00	1000
	3		01	1001
	4		10	1010
	5		11	1011
A_3	6	110	000	110000
	7		001	110001
	8		010	110010
	9		011	110011
	10		100	110100
	11		101	110101
	12		110	110110
	13		111	110111

Frequency-directed run-length (FDR) code

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ)

5. Power-Aware BIST and Test Data Compression

5.2 Coding-based compression

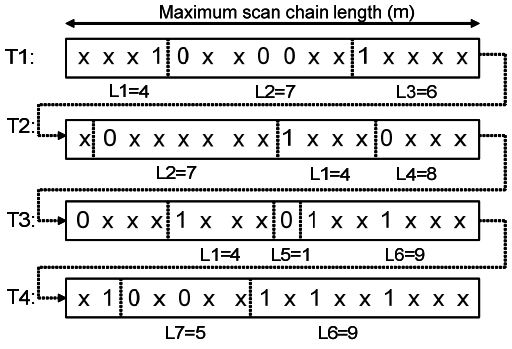
Group	a =0 Run-Length of 0s	a=1 Run-Length of 1s	Group Prefix	Tail	Codeword
A_1	0	0	0	0	00
	1	1		1	01
A_2	2	2	10	00	1000
	3	3		01	1001
	4	4		10	1010
	5	5		11	1011
A_3	6	6	110	000	110000
	7	7		001	110001
	8	8		010	110010
	9	9		011	110011
	10	10		100	110100
	11	11		101	110101
	12	12		110	110110
	13	13		111	110111

Alternating run-length code

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ)

5. Power-Aware BIST and Test Data Compression

5.2 Coding-based compression



Characters (Block Sizes) (Li)	Occurrence Frequency (fi)
1	1
4	3
5	1
6	1
7	2
8	1
9	2

(N_1)

Final Sequence (Li[v]):

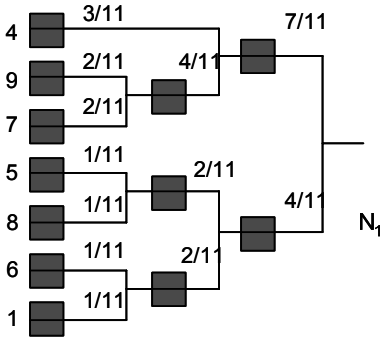
4[1] 7[0] 6[1] 7[0] 4[1] 8[0] 4[1] 1[0] 9[1] 5[0] 9[1]

The application of run-length coding

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ)

5. Power-Aware BIST and Test Data Compression

5.2 Coding-based compression



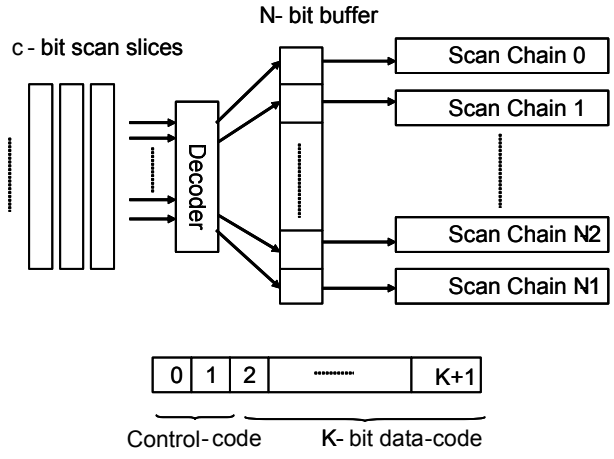
Characters (Li)	Occurrence Frequency (fi)	Huffman Code (Ci)	Saving (Si)
4	3	00	+6
9	2	010	+12
7	2	011	+8
5	1	100	+2
8	1	101	+5
6	1	110	+3
1	1	111	-2
			S=+34

The application of Huffman coding

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ)

5. Power-Aware BIST and Test Data Compression

5.2 Coding-based compression



Selective encoding - concept

(Z. Wang and K. Chakrabarty, Proc. ITC, paper 24.3, 2005)

5. Power-Aware BIST and Test Data Compression

5.2 Coding-based compression

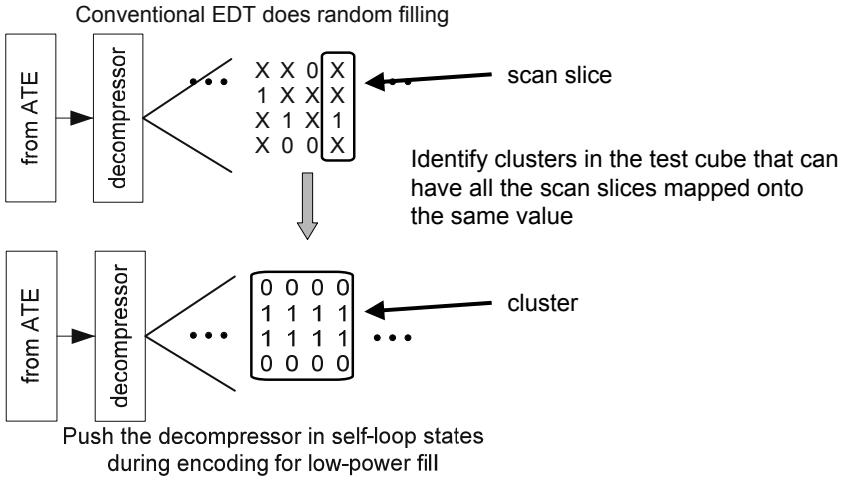
Slice	Slice code		Description
	Control code	Data code	
XX00 010X	00	0101	Start a new slice, map X to 0, set bit 5 to 1
1110 0001	00	0111	Start a new slice, map X to 0, set bit 7 to 1
	11	0000	Enter group-copy-mode, starting from bit 0 (i.e., group 0)
	11	1110	The data is 1110
XXXX XX11	01	1000	Start a new slice, map X to 1, no bits are set to 0

Selective encoding - example

(*Z. Wang and K. Chakrabarty, Proc. ITC, paper 24.3, 2005*)

5. Power-Aware BIST and Test Data Compression

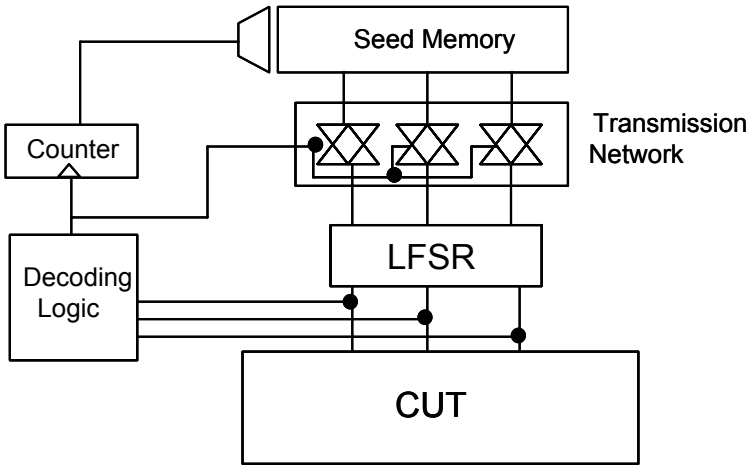
5.3 LFSR-based compression



(*F. Czyusz et. al., Proc. VTS, pp. 75-83, 2007*)

5. Power-Aware BIST and Test Data Compression

5.4 Low-power BIST

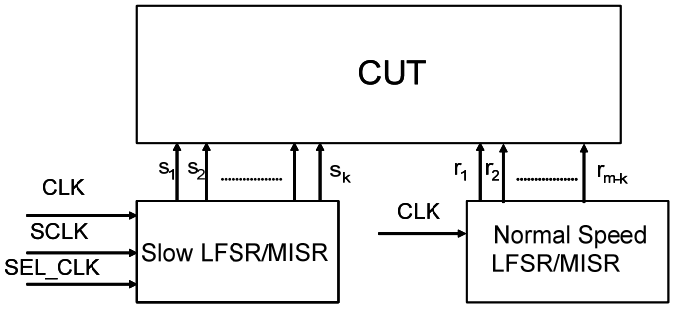


Pattern suppression during BIST with re-seeding

(*S. Manich et. al., JETTA, vol, 16, issue 3, 2000*)

5. Power-Aware BIST and Test Data Compression

5.4 Low-power BIST



Dual-speed LFSR - concept

(*S. Wang and S. Gupta., Proc. ITC, pp. 848-857, 1997*)

5.4 Low-power BIST

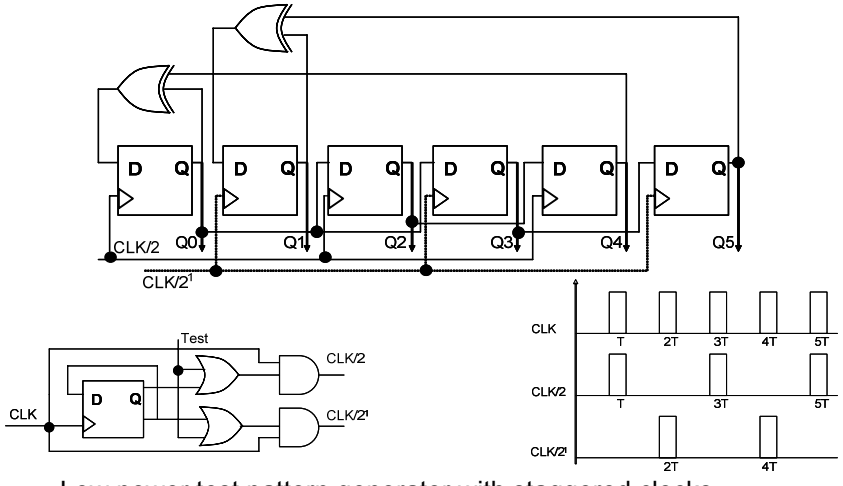
		S	N		S	N
0001		00	01		01	01
1000		10	00		01	10
0100		01	00		01	11
0010		00	10		01	00
1001		10	01		10	01
1100	Partitioned	11	00	Reordered	10	10
0110	→	01	10	→	10	11
1011		10	11		10	00
0101		01	01		11	01
1010		10	10		11	10
1101		11	01		11	11
1110		11	10		11	00
1111		11	11		00	01
0111		01	11		00	10
0011		00	11		00	11
0000		00	00		00	00

Dual-speed LFSR - example

(*S. Wang and S. Gupta., Proc. ITC, pp. 848-857, 1997*)

5. Power-Aware BIST and Test Data Compression

5.4 Low-power BIST

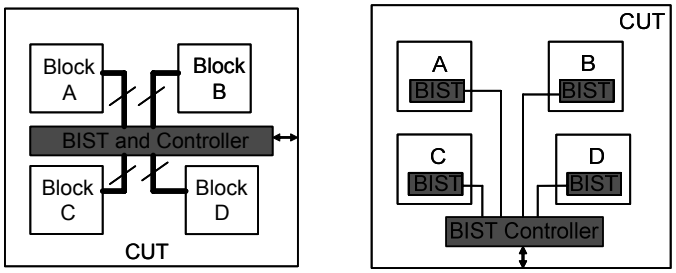


Low power test pattern generator with staggered clocks

(*P. Girard et. al., Proc. VTS, pp. 306-311, 2001*)

5. Power-Aware BIST and Test Data Compression

5.4 Low-power BIST



•Circuit partitioning for low-power BIST
- Centralized BIST and controller
- Distributed approach where BIST sessions are power-conscious

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ)

6. Power-Aware System-Level Test Planning

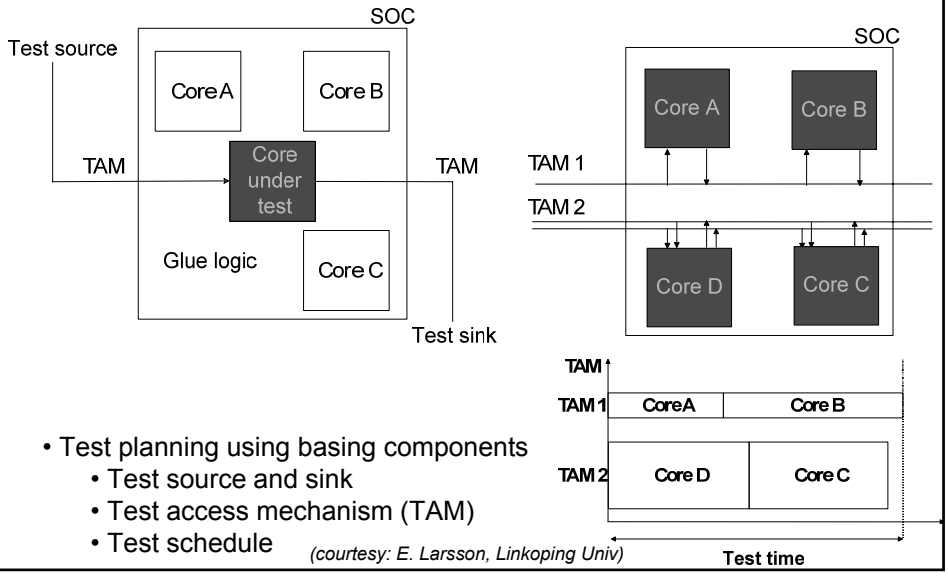
Chapter 6

Power-Aware System-Level Test Planning

6.1 Overview of power-aware system test

- Core-based test architecture and planning
- Power modeling and estimation
- Power-constrained test planning

6.2 Core-based test architecture

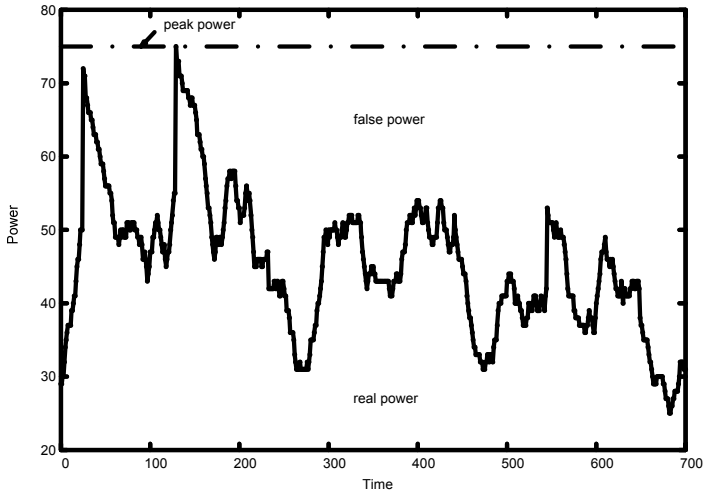


- Test planning using basing components
  - Test source and sink
  - Test access mechanism (TAM)
  - Test schedule

(courtesy: E. Larsson, Linkoping Univ)

6. Power-Aware System-Level Test Planning

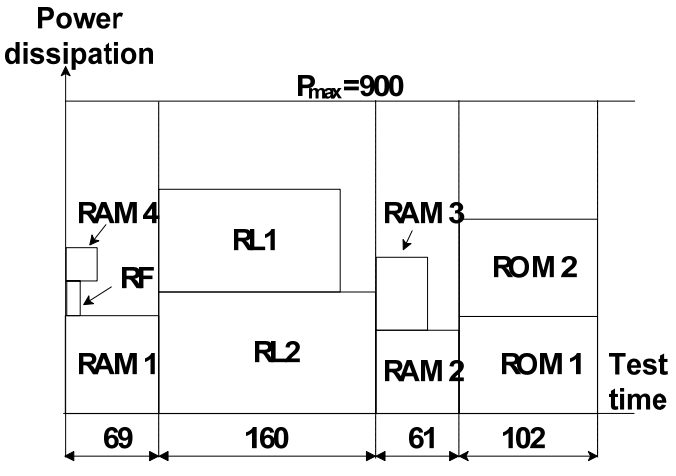
6.3 Power modeling and estimation



(courtesy: E. Larsson, Linkoping Univ)

6. Power-Aware System-Level Test Planning

6.3 Power modeling and estimation

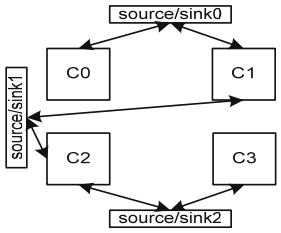


A sample test schedule

(courtesy: E. Larsson, Linkoping Univ)

6. Power-Aware System-Level Test Planning

6.4 Power-constrained test planning

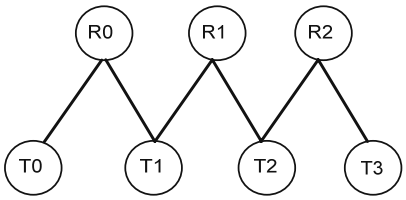


test sessions/test time

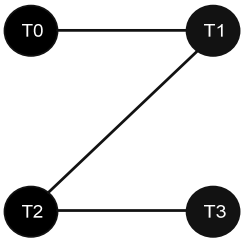
{T0, T2} {T1, T3}

0.5s 0.3s 0.8s 0.3s

resource allocation graph



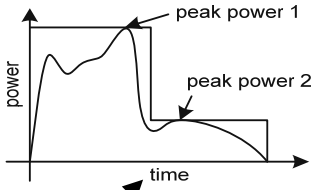
test incompatibility graph



(*R. Chou et. al, IEEE Trans on VLSI, Vol. 5, No. 2, pp. 175-185 , 1997*)

6. Power-Aware System-Level Test Planning

6.4 Power-constrained test planning

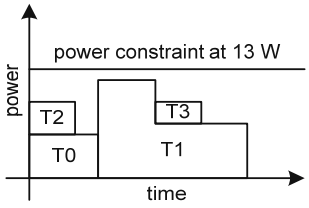


Power profile can be modified by pattern modification and/or test set reordering

test power

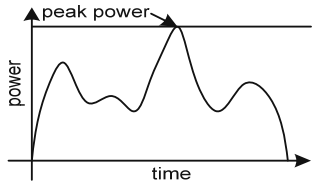
T1 12W for 0.3s

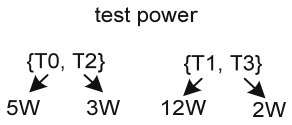
6W for 0.5s

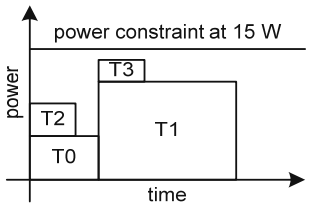


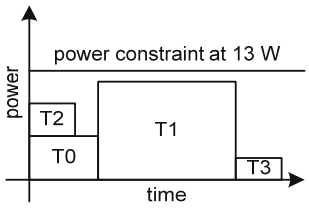
6. Power-Aware System-Level Test Planning

6.4 Power-constrained test planning



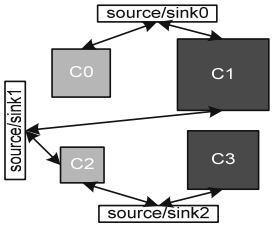






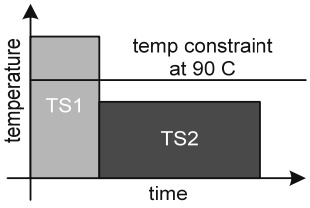
6. Power-Aware System-Level Test Planning

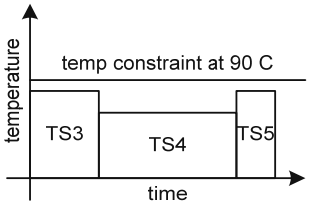
6.4 Power-constrained test planning



temperature dependent test

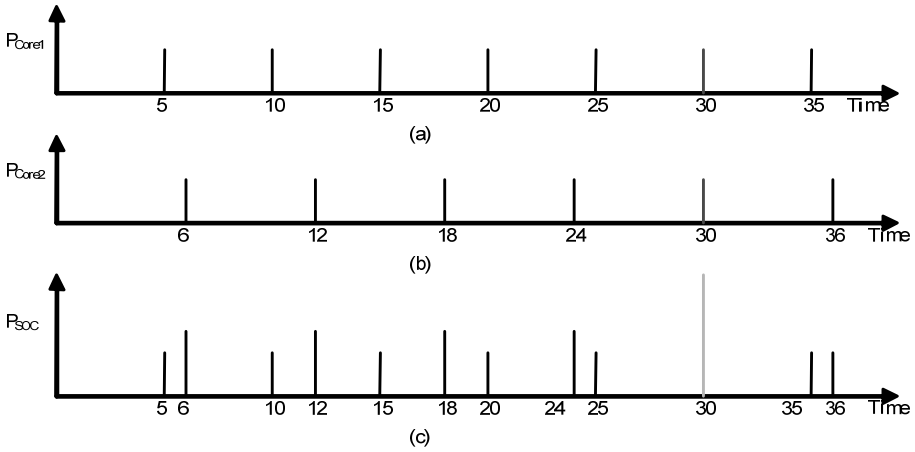
TS1 = {T0, T2} → 130 C
TS2 = {T1, T3} → 70 C
TS3 = {T0, T3} → 80 C
TS4 = {T1} → 60 C
TS5 = {T2} → 80 C





6. Power-Aware System-Level Test Planning

6.4 Power-constrained test planning



Avoiding peak capture power violations by skewing the shift cycles

(courtesy: E. Larsson, Linkoping Univ)

7. Low-Power Design Techniques and Test Implications

Part 3

Chapter 7

Low-Power Design Techniques

and Test Implications

7.1 Low Power Design Trends

System & Architecture	IC Design & Implementation
▪ Voltage / Frequency Scaling ▪ Architecture (parallel, well managed pipeline, etc.) ▪ Others (H/S partitioning, instruction set, algorithms, etc.)	▪ Clock Gating ▪ Multiple Supply Voltage ▪ Multiple Threshold Voltage ▪ Substrate-Bias ▪ Power Gating ▪ Others
Circuit (Logic) Design	**Process Technology**
▪ Low Power Cell Library ▪ Gate sizing (to equalize paths) ▪ Buffer insertion to reduce slew ▪ Logic restructuring to avoid hazards ▪ Memory Bit Cell and Compiler ▪ Others	▪ Reduce Vdd ▪ Threshold Voltage Option ▪ Low Capacitance Dielectric ▪ New Gate Oxide Material ▪ Transistor Sizing ▪ Others

7. Low-Power Design Techniques and Test Implications

7.1 Low Power Design Trends

Efficiency of LPD Techniques *

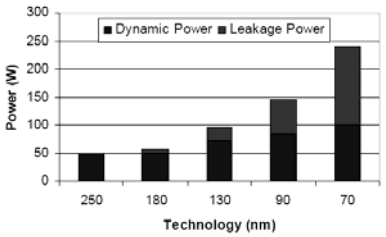
▪ Micro architecture (pipelining, parallelism)	50%
▪ Clock gating and power gating	40%
▪ Logic design	20%
▪ Technology mapping	30%
▪ Cell sizing and wire sizing	30%
▪ Voltage scaling, multi-Vdd, multi-Vth	75%
▪ Floor planning and placement	25%
▪ …	

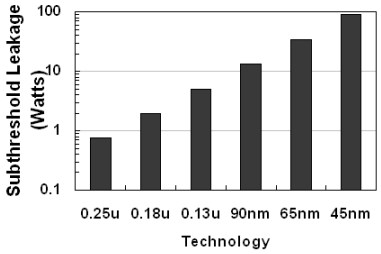
(K. Keutzer, UC Berkeley, SDC panel, 2005)

7.1 Low Power Design Trends

Leakage dominates Power equation beyond 70nm

* Today, leakage power amounts to almost 40% of the total power of a microprocessor





(source: INTEL)

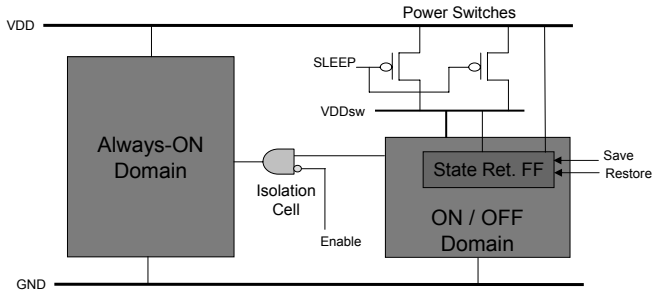
7. Low-Power Design Techniques and Test Implications

7.1 Low Power Design Trends

Main LPD techniques	Power reduction	
	Dynamic	Leakage
Clock gating	✓	
Power gating	✓	✓
Multi-Voltage domains	✓	
Multi-Threshold cells		✓

These techniques are often combined together to achieve the maximum power optimization value

7.1 LPD Trends - PM infrastructure

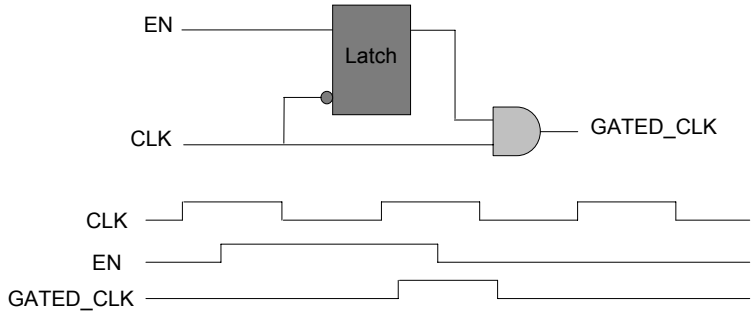


PM Structure	Usage
Gated Clocks	Gates clock going to a sequential block
Power Switches	(SLEEP=1) cuts off VDD from going to core
Isolation Cells	(Enable=1) sets output of domain to 0 when power is shut down
State Retention FF	(Save=1) ensures that data is saved when power domain is OFF. (Restore=1) Restores the saved data when power domain wakes up

(courtesy: Srivaths Ravi, TI)

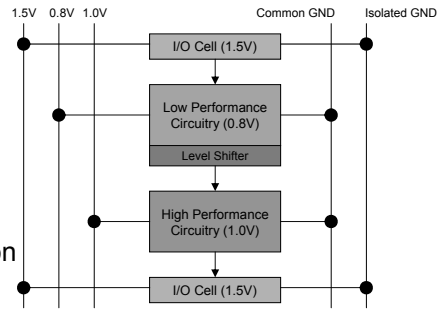
7.1 LPD Trends - Clock Gating

- Reduces dynamic power by restricting clock distribution (clock switching in idle logic blocks is shut off)
- Low overhead technique
- Widely adopted and supported by existing EDA tools



7.1 LPD Trends - Multiple Supply Voltage

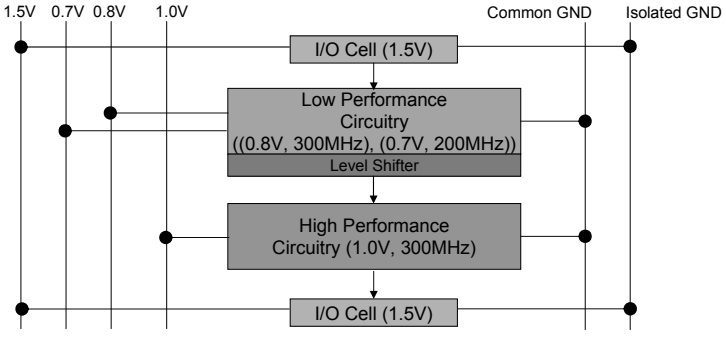
- Vdd scaling results in quadratic power reduction ($P=kCV^2f$)
- Adopted techniques are:
  - Static voltage scaling →
  - Dynamic voltage scaling
  - DVFS
- Creation of "power islands"
- Reduces dynamic power dissipation
- Requirement / implications:
  - Level shifters to let signals cross power domain boundaries
  - Lower margin for IR drops / increased noise susceptibility



7. Low-Power Design Techniques and Test Implications

7.1 LPD Trends - Multiple Supply Voltage

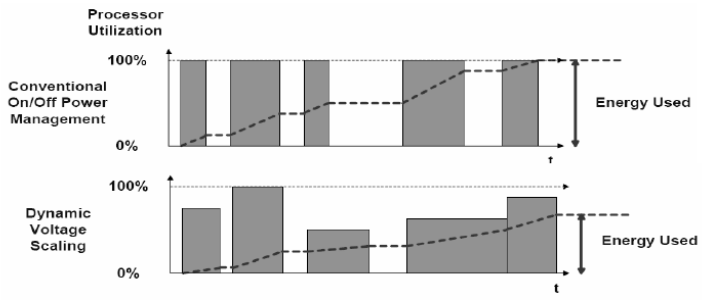
- When high performance is not required, voltage and frequency can be scaled down
  - Dynamic voltage and frequency scaling (DVFS)



(source: CADENCE, 2007)

7.1 LPD Trends - Multiple Supply Voltage

- Dynamic voltage and frequency scaling (example)

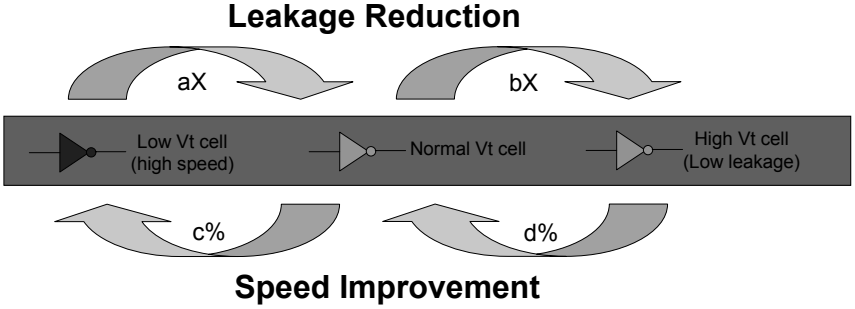


- Design flow is similar to MSV flow, but more complex control mechanism and more complicated timing analysis

(R. Aitken, ARM, SDC panel, 2005)

7.1 LPD Trends - Multiple Threshold Voltage

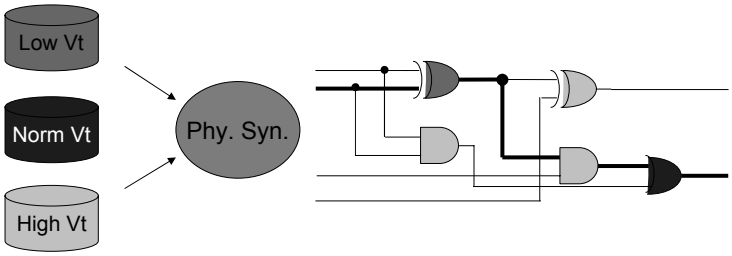
- Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction
- Speed cost to decrease leakage !!



(source: CADENCE, 2007)

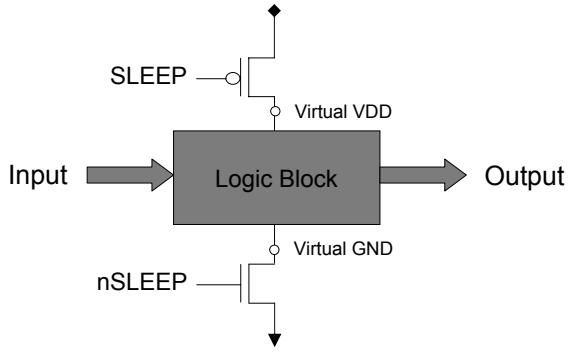
7.1 LPD Trends - Multiple Threshold Voltage

- MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)
- Leakage power reduction while meeting timing and no area overhead
- Well established and supported by existing EDA tools



7.1 LPD Trends - Power Gating

- Used to shut down blocks (power domains) that are not in used (idle mode) hence reducing leakage power and dynamic power
- Done by using Multiple-Threshold CMOS (MTCMOS) switches



7.1 LPD Trends - Power Gating

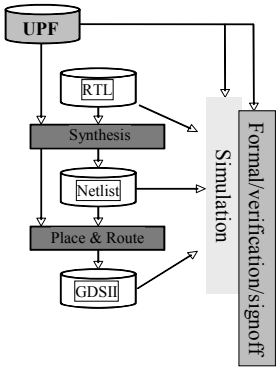
- Adopted in regular structures (data paths) where the gating transistor can be easily shared
- Power gating cells usually cost 10% area overhead and about 2% performance degradation
- Power-on and power-down sequences can be extremely complex to design and verify
- Careful sizing of gating transistors (wide enough to sustain worst-case switching condition)
- Impact on the design flow may be high

7.2 Power Specification Formats

- Need of specifying properties of a circuit block wrt power dissipation during design, verification and implementation
- Interpreted by designers and design automation tools
- To achieve a unified and efficient design flow, various EDA tools need to use a common language
  - *Common Power Format* (CPF) created by Cadence
  - *Unified Power Format* (UPF) supported Synopsys, Mentor and Magma and standardized by IEEE (P1801 std. working group)
- 90% same concepts, but different syntaxes
- Both formats are based on the *Tool Control Language* (TCL) embedded in most EDA tools

7.2 Power Specification Formats

- Used to describe the following specifications:
  - Voltage domains, Power domains, Isolation logic, Retention registers, Always-on cells, Power switches
  - The various power modes also need to be specified
  - Operating environment details (process, temperature, operating voltage data, and leakage calculation) are not part of UPF
  - UPF-based low power design flow →

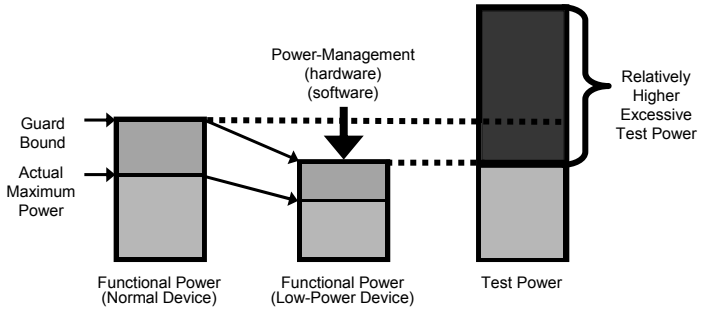


- Example: creation of power domains

```
create_power_domain pdTOP
create_power_domain pd1 □elements U1
create_power_domain pd2 □elements U2
create_power_domain pd3 □elements U3
```


7.3 Implications to Test Requirement and Cost

- Power management techniques are attractive since they can achieve maximum performance under a power-temperature envelope
- But they can have undesirable consequences on Test !!!



Power during test is even more critical for low-power devices !!

7.3 Implications to Test Requirement and Cost

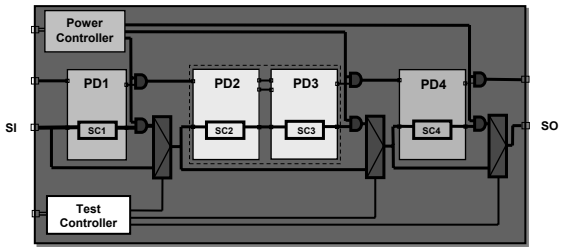
- Reduce (even more) test power by using the PM infrastructure and/or applying the previous dedicated solutions (chapters 3 to 6)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures
- Consider the influence of LPD on test conditions
- Provide high quality delay fault coverage

And still target:

High fault coverage, short test application time, small test data volume, low area overhead, etc … while making test power dissipation (dynamic and leakage) comparable to functional power

7.3 Implications use of PM infrastructure

- Existing solutions
  - ATPG and DfT for multi-voltage designs (addressed in Chapter 8)
  - ATPG and DfT for gated clock designs (addressed in Chapter 9)
  - Test planning for multi-power domains architectures (addressed in Chapter 11)



7.3 Implications □ Preserving Test Functionality

Main Challenge

- Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints

Specific test control strategies and extra DfT insertion are required for preserving functionality of the test infrastructure !

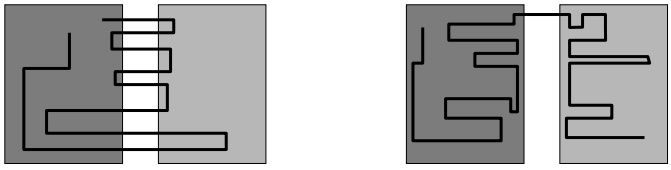
- Similar challenges exist for gated clock designs (addressed in Chapter 9)

7. Low-Power Design Techniques and Test Implications

7.3 Implications □ Preserving Test Functionality

Example: MSMV-aware scan chain assembly

- Minimize the occurrence of chains that cross voltage domains

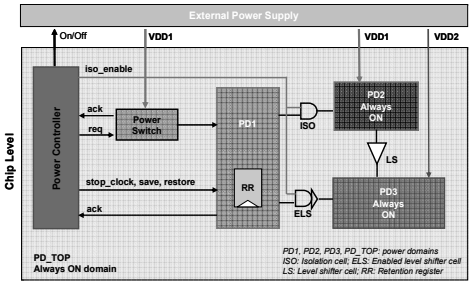


- Avoid unwanted power down during scan shift/capture
- Chain must not span domains that must be independently on/off
- Chains traversing through powered down domains must bypass them
- ...

(M. Hirech, Synopsys, DATE 2008)

7.3 Implications – Test the PM Structures

- **Power management structures have to be tested and need dedicated test / DfT / ATPG methods for:**
  - Level shifters
  - Isolation cells
  - State retention registers
  - Power controller
  - Power switches (by far the most challenging task !!)



(Addressed in Chapter 10)

(courtesy: M. Hirech, Synopsys)

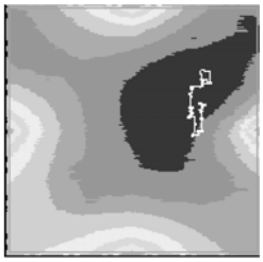
7. Low-Power Design Techniques and Test Implications

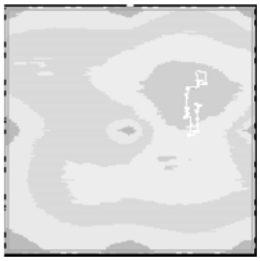
7.3 Implications – Adapt Test Conditions

- Combined impact of advanced PM techniques and process-induced uncertainty in device parameters (transistor length, width, oxide thickness, random dopant fluctuations, etc. that have a great impact, especially on the threshold voltage) imposes a large number of test conditions to ensure correct timing operation (ex. speed binning based on structural delay testing)
  - Testing at multiple Vdd (when DVS in used) (chapter 8)
  - Testing at multiple frequencies for a each Vdd (for DVFS)
  - Testing at multiple temperatures …

7.3 Implications Adapt Test Conditions

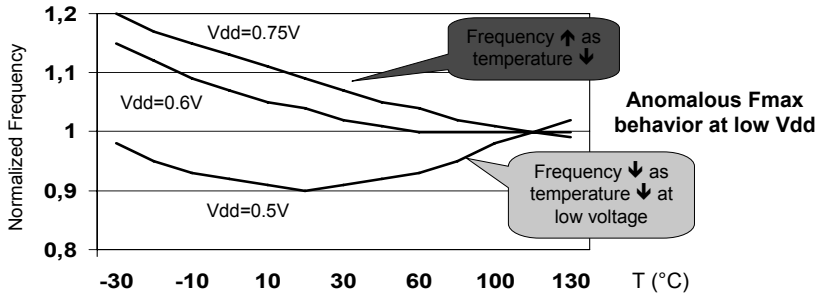
- Different activity levels in different parts of a die causes T° variations. Circuit delay change non-linearly with voltage and temperature.
  - Defining the worst-case timing conditions during test will be even more a challenge !!





7. Low-Power Design Techniques and Test Implications

7.3 Implications Adapt Test Conditions



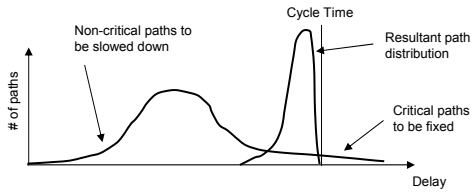
- Traditional Methods of testing at only high temperature for Fmax will be insufficient for low power devices
  - Testing at additional temperatures will increase test time

(G. Singer, Intel, ITC, 2007)

7. Low-Power Design Techniques and Test Implications

7.3 Implications □ Delay Fault Coverage

- By using power optimization techniques such as gate downsizing or MTV, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations
  - PDF selection more complex
  - More test data are needed
  - Sensitivity to variations



- PSN has a significant impact on the timing behavior
  - Need to integrate PSN effects in delay test pattern generation

High quality at-speed (delay) test becomes more complex

8. Test Strategies for Multi-Voltage Designs

Chapter 8

Test Strategies for Multi-Voltage Designs

8. Test Strategies for Multi-Voltage Designs

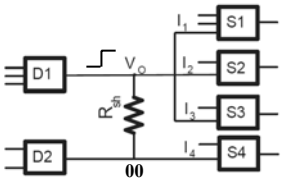
8.1 Test for Multi-Voltage (MV) Design

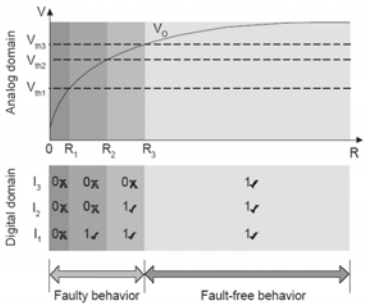
- Multi-Voltage design
  - Use dedicated multiple power supplies on chip, or adaptive voltage scaling circuitry consisting of DC-DC converters and voltage controlled oscillators.
- MV design and Test
  - Some manufacturing defects have Vdd-dependency
  - Impact on defect coverage
  - Testing at all Vdd settings is costly !!
  - Multi-Vdd Test determines the minimum number of voltage settings to ensure the highest level of defect coverage

8. Test Strategies for Multi-Voltage Designs

8.1 Test for MV Design □ Bridge Defects

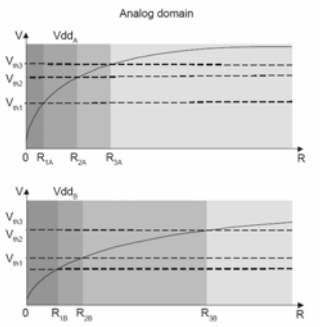
- Bridge defects
  - Most of them are resistive
  - Hard-shorts ~ stuck-at faults → detection is independent of Vdd
- Resistive bridge defects
  - A finite number of discrete intervals can be used to deal with all bridge R_{sh} values





8.1 Test for MV Design – Bridge Defects

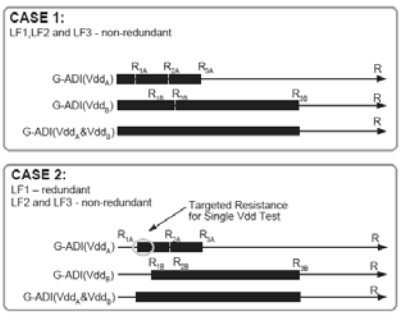
- Resistive bridge behavior at MV settings
  - Voltage Vo does not scale linearly with the input threshold voltage of S1, S2 and S3 when changing Vdd
  - Resistance intervals differ from one voltage setting to another
  - Example: a bridge with $R_{sh} = R_{3B}$ will cause a logic fault at V_{ddB} but not at V_{ddA}
  - A test pattern targeting a particular logic fault will detect different ranges of defects at different MV settings



8. Test Strategies for Multi-Voltage Designs

8.1 Test for MV Design – Bridge Defects

- Resistive bridge behavior at MV settings
  - Case 1: a test set detecting LF1, LF2 and LF3 will achieve full fault coverage when applied at V_{ddB}
  - Case 2: testing at both Vdd settings is required !



8. Test Strategies for Multi-Voltage Designs

8.1 Test for MV Design □ Bridge Defects

- Goal of test generation for MV settings
  - Generate test patterns for MV settings to maximize coverage of Resistive Bridging Faults (RBF) while minimizing test sequence length
  - Identification of Vdd specific test patterns for a given fault f
  - Example*: for a given circuit, 621 test patterns are needed at three Vdd settings with a commercial tool (207 at each Vdd), while only 391 test patterns applied at two Vdd settings (0.8V and 1.2V) are needed with the proposed technique (to achieve 100% fault coverage)

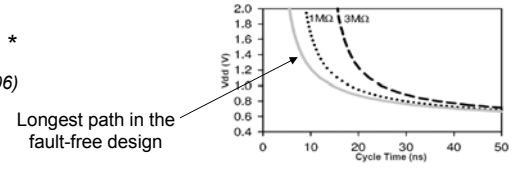
(U. Ingelson et. al., ATS, 2007)

8. Test Strategies for Multi-Voltage Designs

8.2 Test for MV Design □ Open Defects

- Open defects
  - Due to unconnected nodes
  - Full opens → logic failures tested using static faults
- Transmission gate opens
  - Better detectability at low Vdd settings *(N. Zain Ali et. al., ETS, 2006)*
- Interconnect resistive opens
  - Resistive opens → time-dependent → tested using delay tests
  - Better detectability at elevated Vdd settings *

(B. Kruseman et. al., DATE, 2006)*

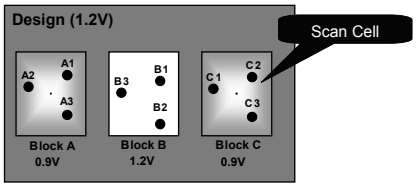


Longest path in the fault-free design

8.3 DfT for Multi-Voltage Designs

Multi-Voltage Aware Scan Cell Ordering

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93%)



Scan chain assembly

Ordering / Position	Logical	Physical	Multi-Voltage
1	A1	A2	A2
2	A2	A1	A1
3	A3	A3	A3
4	B1	B3	C1
5	B2	B1	C2
6	B3	B2	C3
7	C1	C1	B2
8	C2	C2	B3
9	C3	C3	B1

Level shifter

- Implemented in Synopsys Design Compiler

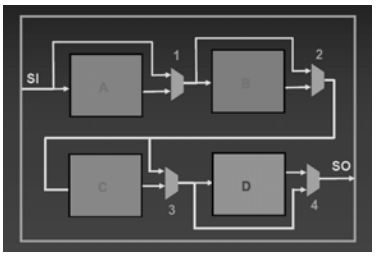
(A. De Colle et. al., JOLPE Vol. 1, N°1, April 2005)

8. Test Strategies for Multi-Voltage Designs

8.3 DfT for Multi-Voltage Designs

Power-Aware Scan Chain Assembly for MV Designs

- Bypass multiplexers allow testing of specific power domains in MSMV environment (switched-off power domains are bypassed)
- Preserve test functionality !



- Implemented in Cadence *Encounter*™

(V. Chickermane et. al., ITC 2008)

8.3 DfT for Multi-Voltage Designs

Power-Managed Scan Using AVS

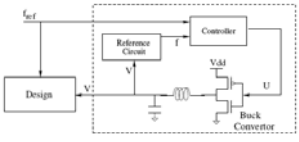
- Adaptive Supply Voltage (AVS) Scaling infrastructure for DVS is widely used in modern SoCs to reduce dynamic and leakage power
- Re-use of this infrastructure in the test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
- At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
  - Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan FFs (V_t) = 0.35 V, shift Frequency (F_{shift}) = 125 MHz → V_{shift} = 0.635 V

(V.R. Devanathan et. al., ITC 2007)

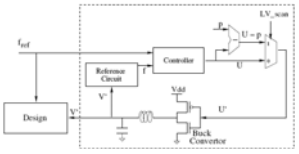
8. Test Strategies for Multi-Voltage Designs

8.3 DfT for Multi-Voltage Designs

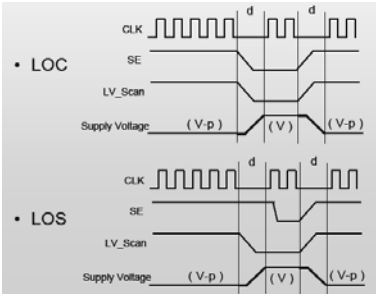
Power-Managed Scan Using AVS



Conventional Voltage Scaling Apparatus



PMScan: Shift Voltage Scaling Apparatus



LV_scan: Control signal from tester for low-voltage scan

● Around 45% reduction of dynamic (average and peak) power and 90% reduction of leakage power, with negligible physical design impact and minimum area overhead

Chapter 9

Test Strategies for Gated Clock Designs

9. Test Strategies for Gated Clock Designs

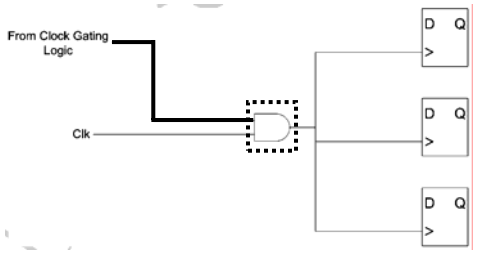
Content

9.1 Functional Clock Gating

Basic Concept

- In a CMOS circuit, state changes at FFs triggered by clocks propagate to logic gates, resulting switching activity in the whole circuit.
- No all FFs need to be triggered in order to perform a function (e.g., in a mobile-phone SoC, camera control logic needs not to be active when a call is being made).
- "Stopping" the clock to functionally-noncontributing FFs reduce dynamic power dissipation, *not only in logic portions and also in clock trees (> 50%)*.
- "Stopping" of clocks should be conditional.

Basic Clock Gating

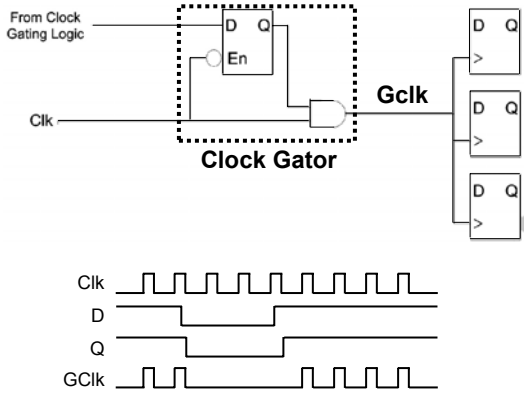


9.1 Functional Clock Gating

Glitch-Free Clock Gating

- Simply gating a clock *Clk* with a clock gating signal from the clock gating logic (not controlled by *Clk*) may create glitches.

Safe Clock Gating

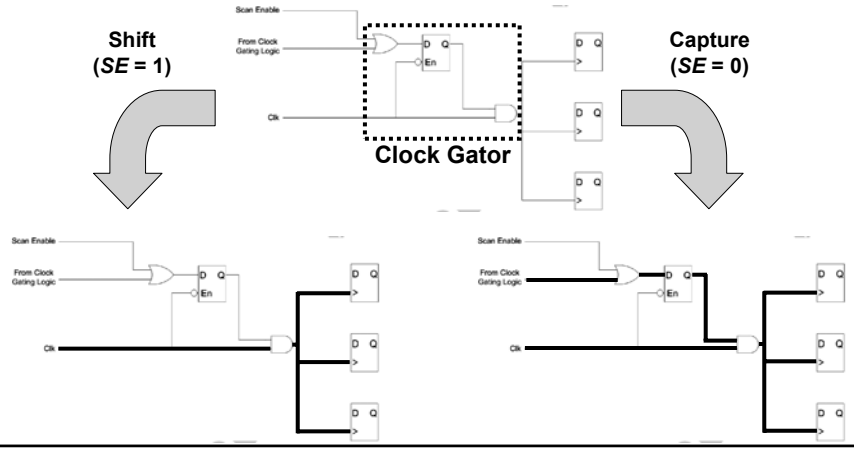


9.2 DFT for Clock Gating Logic

Case of MUXed Scan

Guaranteeing Correct Scan Test Operations

- Disable clock gating in shift mode (*SE* = 1): Unconditionally-ON Clock
- Enable clock gating in capture mode (*SE* = 0): Conditionally-ON Clock

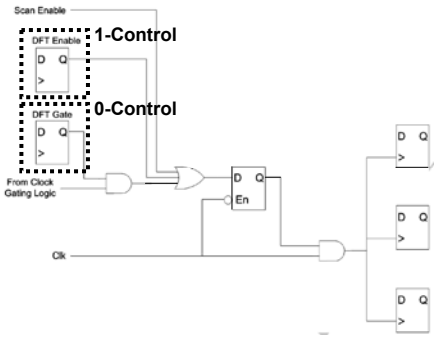


9.2 DFT for Clock Gating Logic

Case of MUXed Scan

Technique for Improving ATPG Efficiency

- If ATPG needs to easily generate a test to gate-off or enable a clock in capture mode, one can improve the 0-controllabilty and 1-controllablity of the clock gating signal.



9.3 Capture Power Reduction Through Clock Gating

Static In-ATPG Technique

Basic Flow

- A **default value** is a value assignment to be made on a bit if ATPG does not requires a different value on the bit.
  - ➔ *A preset value to be used to fill an X-bit in a test cube*.
- Flow for obtaining default values for clock gating:
  - ➔ *Identify all clock gators*.
  - ➔ *For each clock gator, calculate a set of bits settings that can set the clock off*. (*This process only needs to be conducted once up front.*)
  - ➔ *The values in each bit setting are default values.*
- Flow for using default values for clock gating:
  - ➔ *Generate a test cube for fault detection*.
  - ➔ *Assign default values to the X-bits in the test cube*. (*If there are multiple choices of default values, use the one that can turn-off more FFs.*)

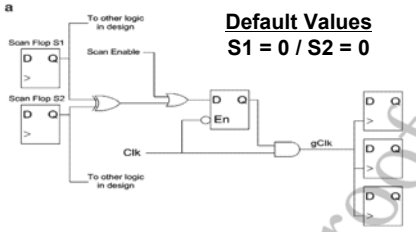
(*R. Illman et. al., Proc. LPonTR, pp. 45-46, 2008*)

9.3 Capture Power Reduction Through Clock Gating

Static In-ATPG Technique

Example

a



Default Values
S1 = 0 / S2 = 0

Test Cubes after ATPG

Test Cubes	Scan flops in design					
	S0	**S1**	**S2**	S3	S4	S5
T1	X	**0**	**X**	1	0	X
T2	0	**1**	**X**	X	X	0
T3	X	**X**	**0**	1	0	X

Test Cubes after Adding Default Values

c

Test Cubes	Scan flops in design						Merge "default values"?
	S0	**S1**	**S2**	S3	S4	S5	
T1	X	**0**	**0**	1	0	X	Yes
T2	0	**1**	**X**	X	X	0	Conflict
T3	X	**0**	**0**	1	0	X	Yes

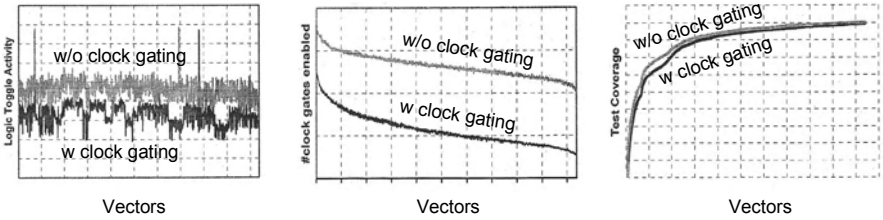
(*R. Illman et. al., Proc. LPonTR, pp. 45-46, 2008*)

9.3 Capture Power Reduction Through Clock Gating

Static In-ATPG Technique

Experimental Results

Circuit Statistics
89K FFs
6 Scan Clocks
2200 Clock Gators



- The number of active clocks are reduced by > 50%.
- Capture toggle activity is reduced by 35%.
- Fault coverage and test set size remain almost unchanged.

(*R. Illman et. al., Proc. LPonTR, pp. 45-46, 2008*)

9.3 Capture Power Reduction Through Clock Gating

Dynamic In-ATPG Technique

- Generate a test cube for primary fault detection.
- Conduct dynamic compaction to secondary fault detection.
- Identify the clocks that can be turned off without any impact of the fault detection capability of the test cube.
- Order the clocks by the decreasing number of FFs that are controlled by each clock.
- Justify 0 to clock gators of the clocks in the pre-determined order.

↓

A Low-Capture-Power Test Cube for Fault Detection

9.3 Capture Power Reduction Through Clock Gating

Post-ATPG Techniques

Goals of CTX

CTX (**C**lock-Gating-Based **T**est Relaxation and **X**-Filling)

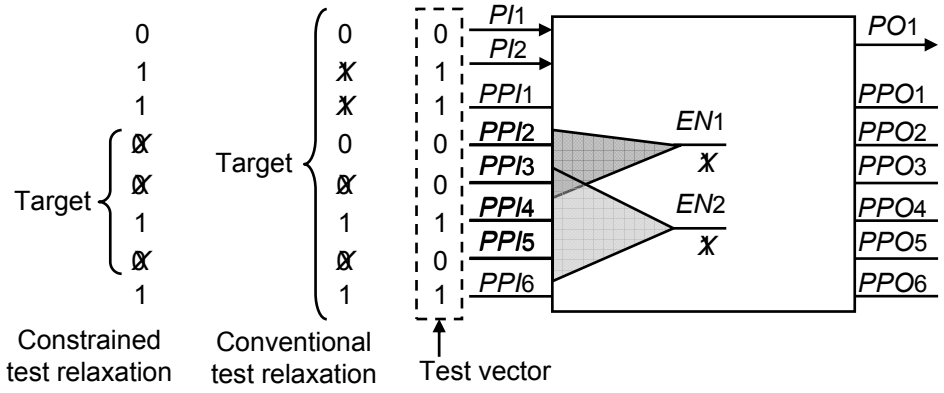
- To explore the collective LSA-reducing capability of clock-gating in at-speed scan testing.
- To further reduce LSA by equalizing the input and output values of FFs.
- To avoid ATPG change, test data inflation, and fault coverage loss.
- To reduce LSA with as few *X*-bits as possible.

(*H. Furukawa et. al., Proc. ATS, pp. 397-402, 2008*)

9.3 Capture Power Reduction Through Clock Gating

Post-ATPG Techniques

Constrained Test Relaxation for Neutralizing Clock Gators



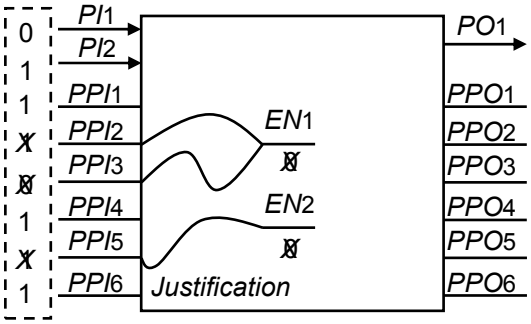
☺ Try to turn as many clock control signals into *X*'s as possible.

(*H. Furukawa et. al., Proc. ATS, pp. 397-402, 2008*)

9.3 Capture Power Reduction Through Clock Gating

Post-ATPG Techniques

X-Filling for Disabling Clock Gators



☺ Try to justify 0 on each neutral clock control signals.

(*H. Furukawa et. al., Proc. ATS, pp. 397-402, 2008*)

10. Test of Power Management Structures

Chapter 10

Test of Power Management Structures

10. Test of Power Management Structures

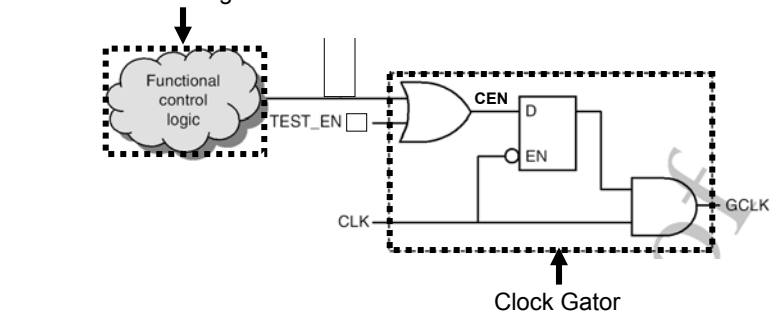
Content

10.1 Clock Gating Logic

Clock Gator and Control Logic

- Clock Gator for enabling/disabling a clock in a glitch-free clock manner.
- Functional Control Logic for implementing clock gating conditions.

Determine *CEN* when *TEST_EN* = 0

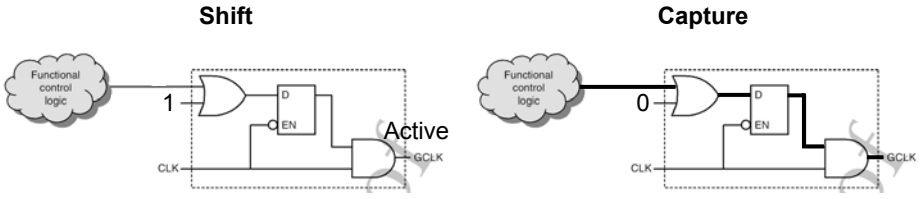


Enable *GCLK* when *CEN* = 1
Disable *GCLK* when *CEN* = 0

10.1 Clock Gating Logic

Testing of the Clock Gator and its Control Logic

TEST_EN = 1 for Shift and TEST_EN = 0 Capture

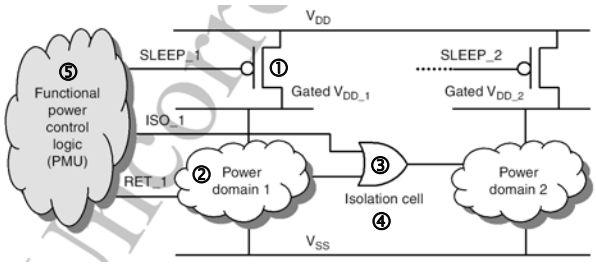


- In shift mode, *GCLK* is always active, allowing the correct shift operation.
- In capture mode, the functional control logic controls the clock gator.
- Chances are high that faults in the clock gator and its functional control logic are detected.
- No need to add any observe point.
- Larger test vector count / lower capture power.

10.2 Power Control Logic

Power Gating Basics

- Power gating = conditional turning on or off the power supply of a logic block (power domain) in order to reduce both dynamic and static (leakage) power.



- Power gating is implemented by adding

  (1) power switches ①

  (2) low-power cells (state retention register ②, isolation cell ③, level shifter ④)

  (3) power management unit (PMU) ⑤

10.2 Power Control Logic

Power Gating Logic

① → **Power Switch** for connecting or disconnecting a power supply or ground of a logic block (power domain).

② → **State Retention Register** for retaining its state when the corresponding power domain is powered-off.

③ → **Isolation Cell** for providing a reliable voltage level and corresponding logic value into a power-on power domain when the source power domain is powered-off.

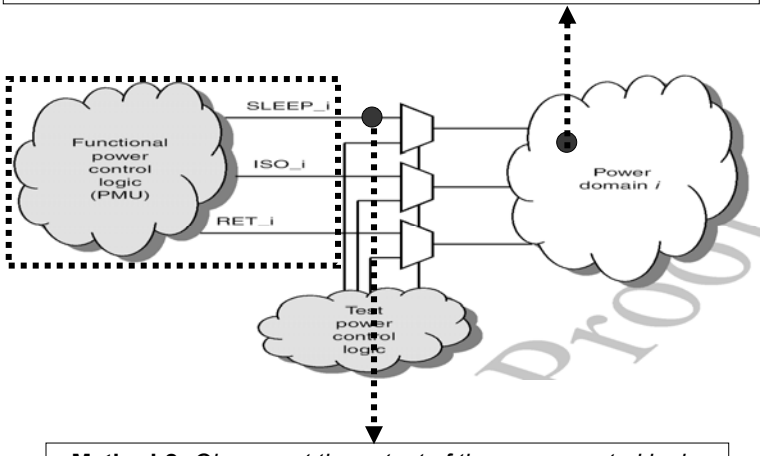
④ → **Level Shifter** for connecting power domains that operate at different voltage levels and converting the voltage levels up or down as needed by the driven power domain.

⑤ → **Power Management Unit (PMU)** for controlling power modes and provide safe transition sequences between power modes.

10.2 Power Control Logic

Testing of Power Control Logic

Method-1: *Observe the logic controlled by the power control logic.*

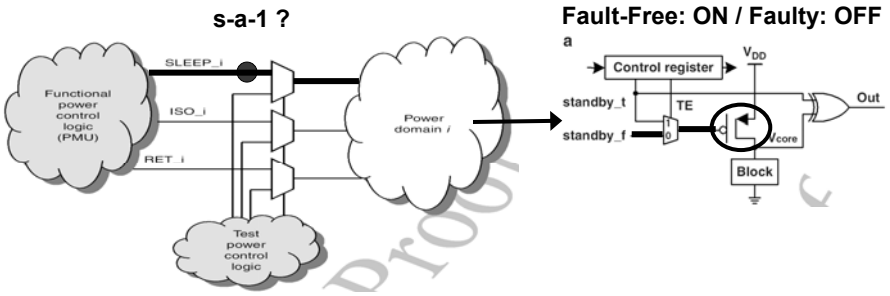


Method-2: *Observe at the output of the power control logic.*

10.2 Power Control Logic

Testing of Power Clock Control Logic

Observing the Logic Controlled by the Power Control Logic

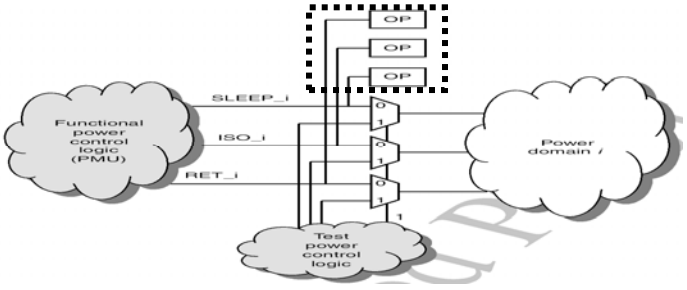


- Observe faulty effects in the downstream logic.
- Advantages:
  - ➔ *Minimizing additional test logic and thus area overhead.*
  - ➔ *Allowing at-speed testing of the power control logic.*
- Disadvantage:
  - ➔ *Causing difficulty in fault diagnosis.*

10.2 Power Control Logic

Testing of Power Clock Control Logic

Observing at the Output of the Power Control Logic

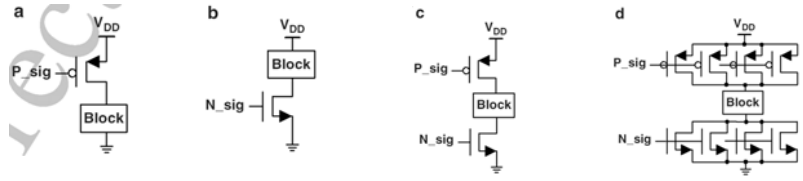


- Add test points to make the outputs of the power control logic observable.
- Advantage:
  - ➔ *Easy to observe faulty effects.*
- Disadvantage:
  - ➔ *Hard to conduct at-speed testing of the power control logic.*

10.3 Power Switches

Types of Power Switches

Header Switch ***Footer Switch*** ***Symmetric Switch*** ***Segmented Switch***



Header Switch / Footer Switch / Symmetric Switch

- Also called sleep transistors.
- Should be large enough to provide sufficient current to the circuit.

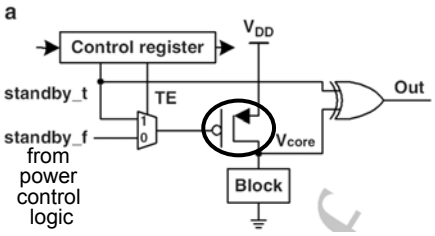
Segmented Switch

- Individual transistors can be small.
- Preferable in practice due to concerns about layout, design for manufacturability, and limiting inrush current when switching on a power domain.

10.3 Power Switches

Techniques for Testing Power Switches

Test for Header Switch with Comparator --- Basic Method



Pattern 1: *TE* = 1 / *standby_t* = 1 (test for short)

➔ Turn-off the power switch. After sufficient discharge, Vcore should be much lower than VDD.
Out (fault-free) = 1 / *Out* (faulty) = 0

Pattern 2: *TE* = 1 / *standby_t* = 0 (test for open)

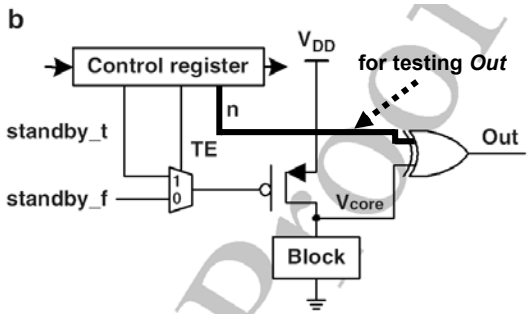
➔ Turn-on the power switch. Vcore should be close to VDD.
Out (fault-free) = 1 / *Out* (faulty) = 0

(*Goal et. al., Proc. ETS, pp. 145-150, 2006*)

10.3 Power Switches

Techniques for Testing Power Switches

Test for Header Switch with Comparator --- Improved Method

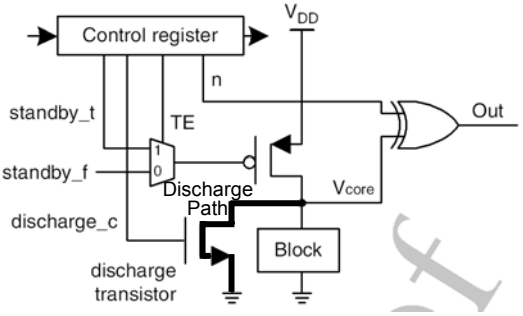


- Use a separate signal *n* to provide comparison data.
- Make it possible to test for both stuck-at-1 and stuck-at-0 of *Out*.
- Two dedicated test signals, *standby_t* and *n*, are needed.
  ➔ *Large number of additional test signals when there are many power switches.*

10.3 Power Switches

Discharge Circuitry

The Design



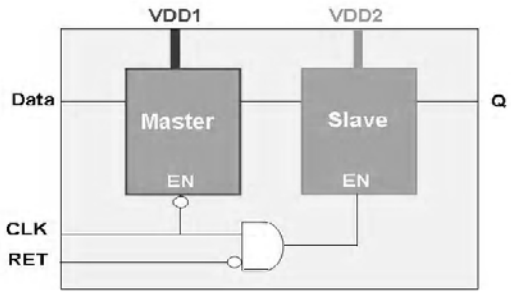
- Discharge Control: power switch = OFF / discharge transistor = ON
- Need an additional control test signal *discharge_c*.

(Peng et. al., Technical Report, CADT-12□01□2008, 2008)

10.4 Low-Power Cells

State Retention Register

Basic Design

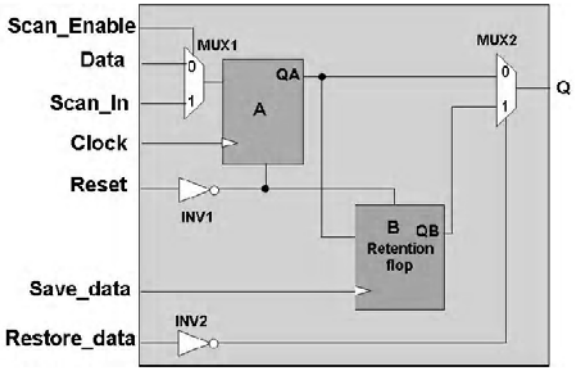


- A SRR cell is for keeping its state when the power supply is turned off.
- Normal Mode: *VDD1* = ON / *VDD2* = ON / *RET* = 0
- Retention Mode: *VDD1* = OFF / *VDD2* = ON / *RET* = 1

10.4 Low-Power Cells

State Retention Register

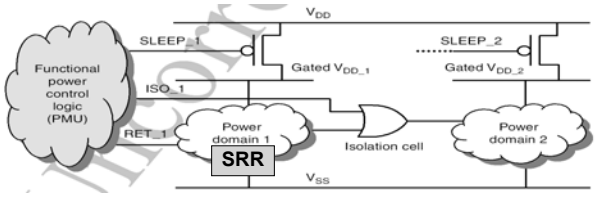
Design with Scan Function



10.4 Low-Power Cells

State Retention Register

Test Method

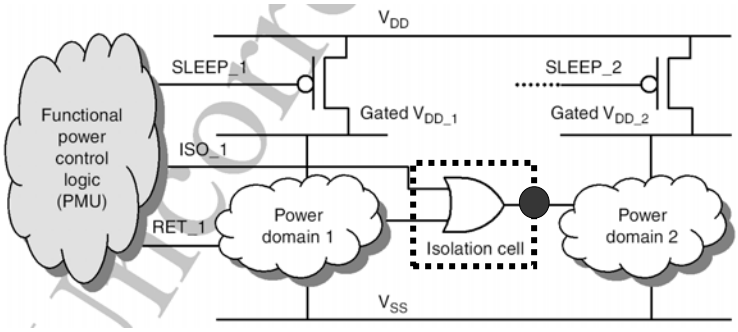


Repeat for *V* = 0 and *V* = 1

- Turn Power Domain 2 on (*SLEEP_2* = 0).
- Shift in value *v* to SRR.
- Enable retention (*RET_1* = 1).
- Enable the isolation cell (*ISO_1* = 1).
- Turn Power Domain 1 off (*SLEEP_1* = 1).
- Turn Power Domain 1 on (*SLEEP_1* = 0).
- Disable the isolation cell (*ISO_1* = 0).
- Disable retention (*RET_1* = 0).
- Shift out the value of SRR and see if its is value *v*.

10.4 Low-Power Cells

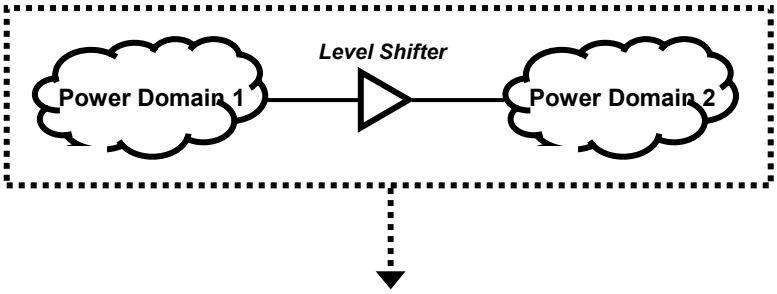
Isolation Cell



- Turn Power Domain 1 off (*SLEEP_1* = 1).
- Turn Power Domain 2 on (*SLEEP_2* = 0).
- Apply a test to detect the stuck-at-0 at the output of the isolation cell *(ISO_1* = 1).

10.4 Low-Power Cells

Level Shifter



Test as a whole under all power supply voltage combinations of Power Domain 1 and Power Domain 2.

11. EDA Solutions for Power-Aware Design-for-Test

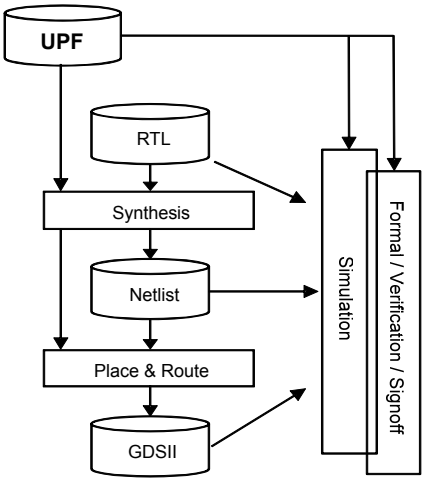
Chapter 11

EDA Solutions for Power-Aware Design-for-Test

11.1 Overview of EDA solutions

- Design flow for power management
- Test automation objectives
- Integration of power management techniques
- Test planning

11.2 Design flow for power management

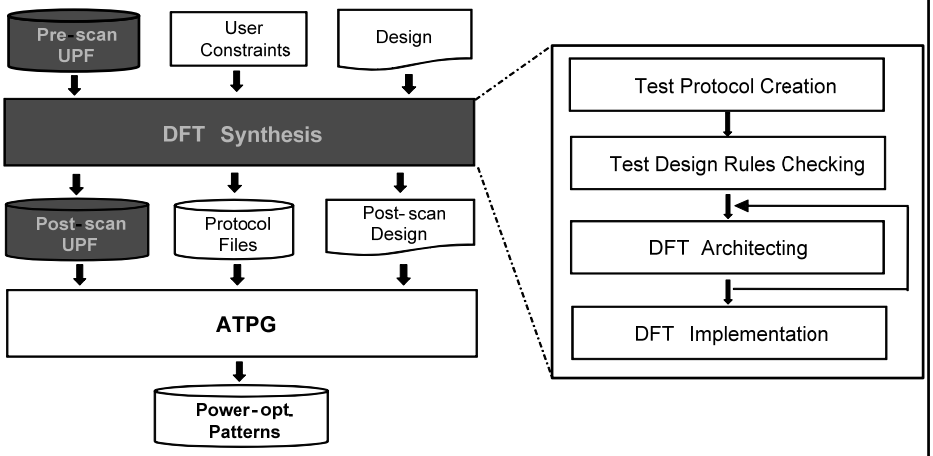


UPF-based low-power design flow

(courtesy: M. Hirech, Synopsys)

11. EDA Solutions for Power-Aware Design-for-Test

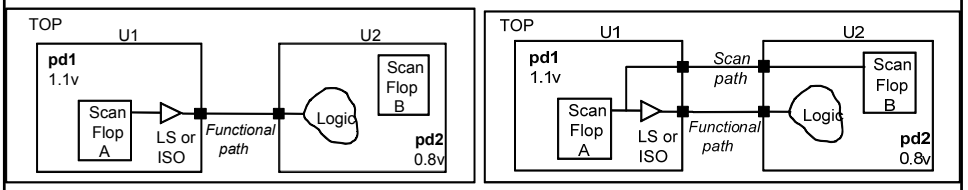
11.3 Test automation objectives



(courtesy: M. Hirech, Synopsys)

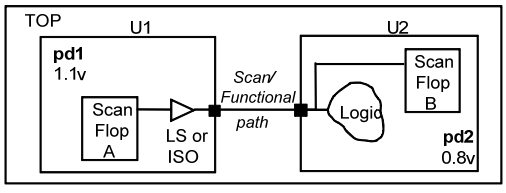
11. EDA Solutions for Power-Aware Design-for-Test

11.4 Integration of power management techniques



(a) Before stitching A to B

(b) Non power aware stitching



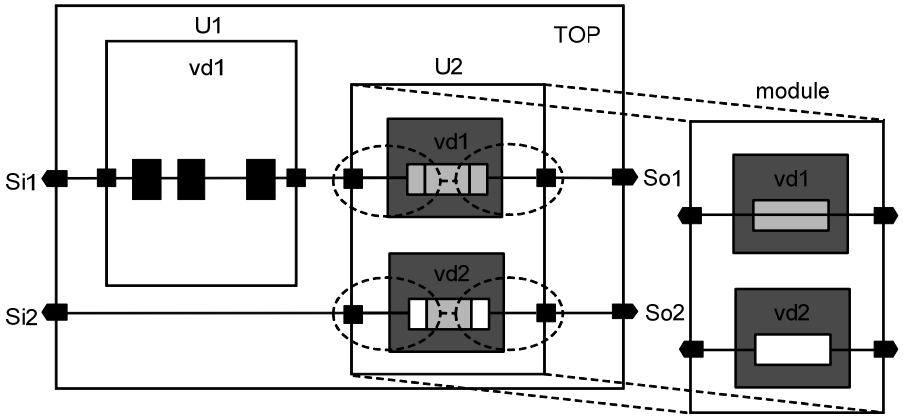
(c) Power aware stitching

Level shifter / isolation cell reuse after scan stitching

(courtesy: M. Hirech, Synopsys)

11. EDA Solutions for Power-Aware Design-for-Test

11.4 Integration of power management techniques

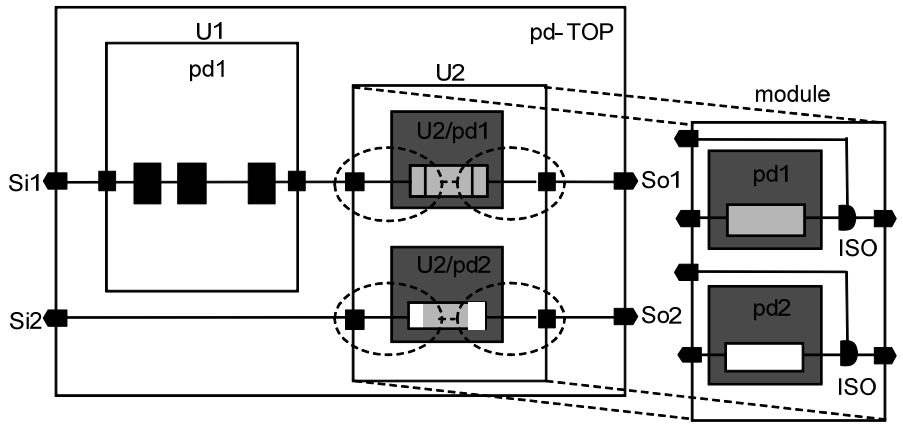


Voltage annotation and scan segment modeling

(courtesy: M. Hirech, Synopsys)

11. EDA Solutions for Power-Aware Design-for-Test

11.4 Integration of power management techniques

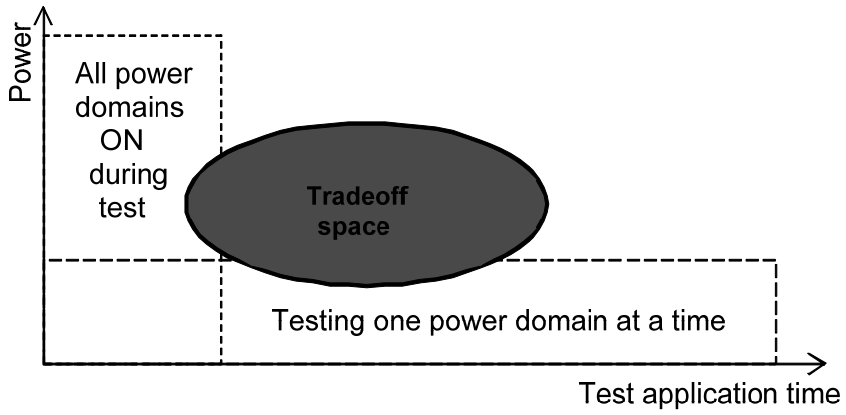


Power-domain annotation and scan segment modeling

(courtesy: M. Hirech, Synopsys)

11. EDA Solutions for Power-Aware Design-for-Test

11.5 Test planning



Power dissipation vs test application time

(courtesy: M. Hirech, Synopsys)

11. EDA Solutions for Power-Aware Design-for-Test

11.5 Test planning

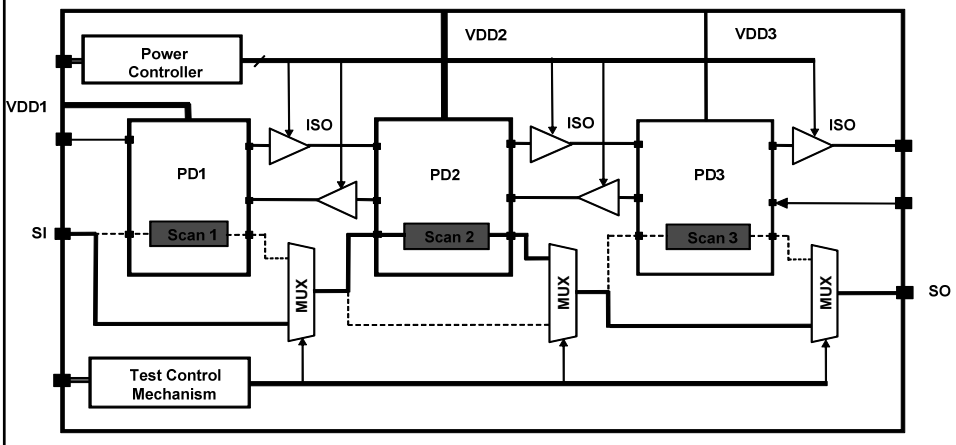


Illustration of multi-mode DFT architecture

(courtesy: M. Hirech, Synopsys)

Summary and Conclusions

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- Reliability, test throughput and manufacturing yield may be affected by excessive test power
- Therefore, lowering test power has been and is still a focus of intense research and development
- Following points have been surveyed:
  - Test power parameters and contributors
  - Problems induced by an increased test power
  - Structural and algorithmic solutions for low power test along with their impacts on parameters such as fault coverage, test time, area overhead, circuit performance penalty, and design flow modification
  - Test implications of low power design and emerging test strategies for low-power devices

Summary and Conclusions

- Past work explored primarily four directions:
  - ATPG-based low power test approaches are not intrusive; they are pattern dependent and may incur additional computational cost in the design flow.
  - DFT-based low power test approaches change the scan infrastructure; can be pattern independent and hence can guarantee power reduction in a certain range.
  - Low power test data compression techniques combines reduction of test data volume and test application time with power consumption during test
  - System-level low power test considerations can be combined with any of the above and improve test concurrency.
- Future work will be mainly on:
  - Test strategies for low power designs

THANK YOU!

And let us make testing "*cool*".