Power-Aware Testing and Test Strategies for Low Power Devices

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Proposal for a full-day (6 hours) or half-day (3 hours) tutorial on
« **Power-Aware Testing and Test Strategies for Low-Power Devices** »
To be delivered at ICM, Cairo, Egypt, 19-22 December 2010

Title of the Tutorial:
Power-Aware Testing and Test Strategies for Low-Power Devices

Area of the Tutorial:
Integrated circuits and systems

Abstract:
Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low-power devices.

This tutorial provides the fundamental and advanced knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during manufacturing test. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low-power design techniques and shows how low-power circuits and systems can be tested safely without affecting yield and reliability. Electronic Design Automation (EDA) solutions for testing low-power devices are also covered in the last part of the tutorial.

Keywords:
Power-aware Testing, Low-Power Design, Power-Constrained Testing, Power Management, Test Power Issues, Design-for-Test, Scan Testing, Built-In Self-Test, Test Data Compression, Automatic Test Pattern Generation

Format of the Tutorial:
The tutorial can be delivered either as a full-day (6 hours) or a half-day (3 hours) tutorial. The description given at the end of this file is for a full-day (6 hours) tutorial, but can be easily shortened for a half-day (3 hours) tutorial.

Target audience and prerequisite knowledge of audience:
VLSI design or test professionals, EDA tool developers, academics who are planning to develop or update their course material on advanced VLSI testing, and students who are entering into the VLSI design, test or EDA fields. The prerequisite knowledge of audience only includes basic understanding of VLSI design and test, although fundamentals of manufacturing test and low-power design will also be covered in this tutorial.

Learning objectives:
This tutorial provides a comprehensive course on the established interrelationships between low-power design and manufacturing test of integrated circuits. It deals with both power-aware testing and test challenges posed by the power-management techniques. It covers the fundamentals, the established techniques that have been adopted in practice, and the latest research results in the field. The learning objectives of this tutorial are to understand i) the impact of test power and various techniques for test power reduction, ii) the impact of low-power design on testing and various test techniques targeted at power management structures, and iii) the latest trends in low-power test research and development for low-power devices.

Previous offerings of the tutorial:
This tutorial has been given as a half-day tutorial at the IEEE/ACM Design Automation and Test in Europe (DATE) conference in Munich, Germany, on March 10th, 2008, at the IEEE Asian Test Symposium (ATS), Taichung, Taiwan, on November 23rd, 2009, at the IEEE Latin American Test Workshop (LATW) in Punta del Este, Uruguay, on March 28th, 2010, at the IEEE International NEWCAS Conference, in Montreal, Canada, on June 20th, 2010, and at the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) in Seattle, USA, on August 1st, 2010. It was also given as a full- day tutorial at the IEEE International Test Conference (ITC) in Austin, USA, on November 2nd, 2009.

Proposed book for handout:
Patrick Girard, Nicola Nicolici, and Xiaoqing Wen, editors, Power-Aware Testing and Test Strategies for Low Power Devices, Springer, ISBN: 978-1-4419-0927-5, November 2009.
http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4419-0927-5

Speakers:
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- Prof. Nicola NICOLICI, McMaster University, Department of Electrical and Computer Engineering, 1280 Main Street West, Hamilton, Ontario L8S 4K1, Canada, nicola@ece.mcmaster.ca
- Prof. Xiaoqing WEN, Kyushu Institute of Technology, Department of Computer and Systems Engineering, Kawazu 680-4, Iizuka, Fukuoka 820-8502, Japan, wen@cse.kyutech.ac.jp

Biographies of each Speaker:
Patrick GIRARD received a M.S. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research), and Head of the Microelectronics Department of the LIRMM (Laboratory of Informatics, Robotics and Microelectronics of Montpellier - France). His research interests include all aspects of digital testing and memory testing, with emphasis on critical constraints such as timing and power.
From 2006 to 2010, Patrick Girard was Vice-Chair of the European Test Technology Technical Council (ETTTC) of the IEEE Computer Society. He has served on numerous conference committees including ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design Automation and Test in Europe (DATE), IEEE International Test Conference (ITC), IEEE International Conference on Computer Design (ICCD), IEEE VLSI Test Symposium (VTS),

IEEE European Test Symposium (ETS), IEEE Asian Test Symposium (ATS), and ACM/IEEE International Symposium on Low Power Electronic Design (ISLPED).
Patrick Girard is the founder and Editor-in-Chief of the ASP Journal of Low Power Electronics (JOLPE). He is an Associate Editor of the IEEE Transactions on VLSI Systems and the Journal of Electronic Testing – Theory and Applications (JETTA - Springer). From 2005 to 2009, he was an Associate Editor of the IEEE Transactions on Computers. He is a co-editor of the book "Power-Aware Testing and Test Strategies for Low Power Devices", Springer, 2009, and a co-author of the book "Advanced Test Methods for SRAMs – Effective Solutions for Dynamic Fault Detection in Nanoscale Technologies", Springer, 2009.
Patrick Girard has been involved in several European research projects (ESPRIT III ATSEC, EUREKA MEDEA, MEDEA+ ASSOCIATE, IST MARLOW, MEDEA+ NanoTEST, CATRENE TOETS) and has managed industrial research contracts with major companies like Infineon Technologies, Atmel, STMicroelectronics, etc. He has supervised 22 PhD dissertations and has published 6 books or book chapters, 34 journal papers, and more than 110 conference and symposium papers on these fields. He received two Best Paper Awards (ETS 2004 and DDECS 2005). Patrick Girard is a Senior Member of IEEE.

Nicola NICOLICI is an Associate Professor in the Department of Electrical and Computer Engineering at McMaster University, Canada. He received the Dipl. Ing. degree in Computer Engineering from the "Politehnica" University of Timisoara, Romania (1997), and a Ph.D. in Electronics and Computer Science from the University of Southampton, U.K. (2000). His research interests are in the area of computer-aided design and test. He has authored over seventy research papers and one book in this area and received the IEEE TTTC Beausang Award for the Best Student Paper at the International Test Conference (ITC 2000) and the Best Paper Award at the IEEE/ACM Design Automation and Test in Europe Conference (DATE 2004). He served on the technical program committees for DATE, IEEE/ACM Design Automation Conference (DAC), IEEE European Test Symposium (ETS), IEEE Defect and Fault Tolerance Symposium (DFT), IEEE Asian Test Symposium (ATS), IEEE International Conference on Computer Design (ICCD), IEEE/ACM International Symposium on Networks-on-Chip (NOCS), IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), IEEE Workshop on Silicon Debug and Diagnosis (SDD), and he served as the Co-Founder, Program Co-Chair and General Chair for the Diagnostic Services in Network-on-Chips Workshop. He was the guest co-editor for a special issue on Silicon Debug and Diagnosis (published by IETProceedings on Computers and Digital Techniques in November 2007) and a special issue on Low Power Test (published by for the Journal of Electronic Testing – Theory and Applications in August 2008). He currently serves on the Editorial Boards of JETTA, IET Computers and Digital Techniques and Integration, the VLSI Journal. He is a member of the ACM SIGDA, the IET and the IEEE Computer and Circuits and Systems Societies.

Xiaoqing WEN received a B.E. degree from Tsinghua University, Beijing, China, in 1986, a M.E. degree from Hiroshima University, Hiroshima, Japan, in 1990, and a Ph.D degree from Osaka University, Osaka, Japan, in 1993. From 1993 to 1997, he was a Lecturer at Akita University, Akita, Japan. He was a Visiting Researcher at University of Wisconsin, Madison, U.S.A., from October 1995 to March 1996. He joined SynTest Technologies, Inc., U.S.A., in 1998, and served as its CTO until 2003. In January 2004, he joined the Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor. He was the Program Committee Co-Chair of the Sixteenth IEEE Asian Test Symposium and the Eighth IEEE Workshop on RTL and High Level Testing. In addition, he served on the program committees of IEEE Asian Test

Symposium (ATS), IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC), IEEE Int'l Symposium on Electronic Design, Test, & Applications (DELTA), IEEE Int'l Conf. on Design & Test of Integrated Systems in Nanoscale Technology (DTIS), IEEE Int'l Test Conference (ITC), IEEE Workshop on RTL and High Level Testing (WRTLT), and IEEE Workshop on Defect-Based Testing (DBT). His research interests include low-power test generation, high-quality test generation, test compression, fault diagnosis, and testable design. He is the Co-Editor of the book "VLSI Test Principles and Architectures: Design for Testability" (Elsevier, 2006), 32 journal papers, and 60 conference and symposium papers. He is a senior member of the IEEE, a member of the IEICE, and a member of the REAJ.

Tutorial Program:

1. Fundamentals on VLSI Testing

1.2 Fault Models
1.3 Design for Testability
1.4 Logic Testing

2. Power Issues during Test

2.1 Power and Energy Basics
- 2.1.1 Static Dissipation
- 2.1.2 Dynamic Dissipation
- 2.1.3 Total Power Dissipation
- 2.1.4 Energy Dissipation

2.2 Manufacturing Test Flow
2.3 Power Delivery Issues during Test
- 2.3.1 Packaging
- 2.3.2 Power Grid Issues
- 2.3.3 Power Supply Noise

2.4 Thermal Issues during Test
2.5 Test Throughput Problem
2.6 Manufacturing Yield Loss
2.7 Test Power Metrics and Estimation
- 2.7.1 Power Metrics
- 2.7.2 Estimation of Power and Energy Metrics
- 2.7.3 Test Power Estimation

3. Low-Power Test Pattern Generation

3.1 Low-Power ATPG
- 3.1.1 General Low-Power Test Generation
- 3.1.2 Low-Shift-Power Scan Test Generation
- 3.1.3 Low-Capture-Power Scan Test Generation

3.2 Low-Power Test Compaction
- 3.2.1 Low-Power Dynamic Compaction
- 3.2.2 Low-Power Static Compaction

3.3 Low-Power X-Filling
- 3.3.1 Test Cube Preparation

7. Low-Power Design Techniques and Test Implications

8. Test Strategies for Multi-Voltage Designs

9. Test Strategies for Gated Clock Designs

10. Test of Power Management Structures

11. EDA Solution for Power-Aware Design-for-Test

11.1 Design Flows for Power Management
11.2 Test Automation Objectives
11.3 Integration of Power Management Techniques in Design-for-Test Synthesis Flows
11.4 Test Planning

General Conclusion