Power-Aware Testing and Test Strategies for Low Power Devices

Patrick Girard, Nicola Nicolici, Xiaoqing Wen

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Patrick GIRARD
LIRMM / CNRS
France

Nicola NICOLICI
McMaster University
Canada

Xiaoqing WEN
Kyushu Institute of Technology
Japan

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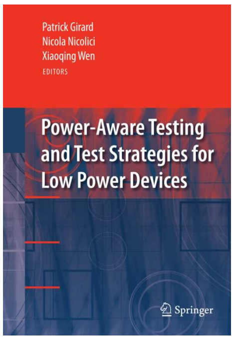

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Outline

1. Basics on Test
2. Relevance of power during test
3. Main test power issues
4. Reducing test power by dedicated techniques
5. Low Power Design and its implications on test
6. Reducing test power of low power circuits
7. Conclusion

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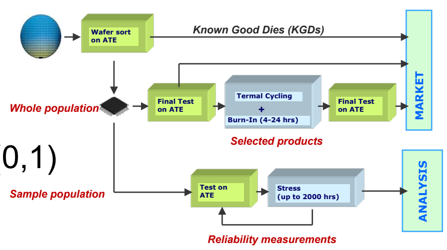
Context

- Manufacturing test
- Digital circuits and systems
- Test stimuli are logic values (0,1)
- Test is an experiment !

✓If responses meet expectations, chip may be good … or stimuli are not sufficient (test escape)

✓If responses fail, chip may be faulty … or measurement may be erroneous (yield loss)

- Test costs can now amount to 40% of overall product cost



(courtesy: Bernardi et al., ETS, 2009)

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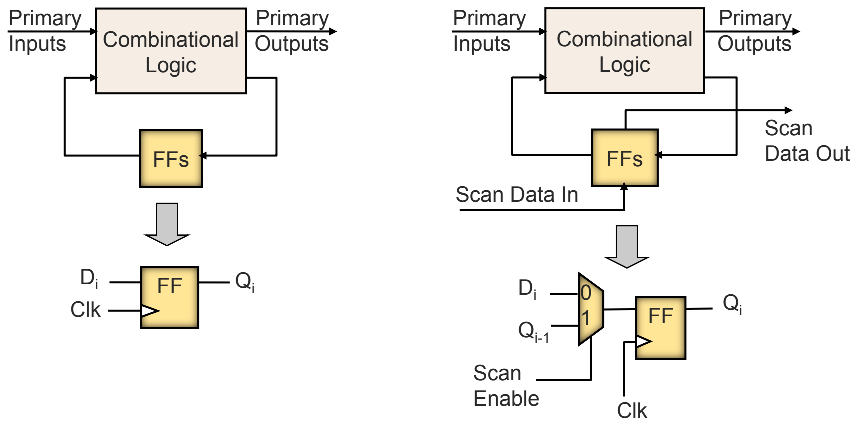
Basics on Test - DfT

- Functional test is used … but structural test is dominant !
- Use of fault models … and DfT (Design-for-Test)



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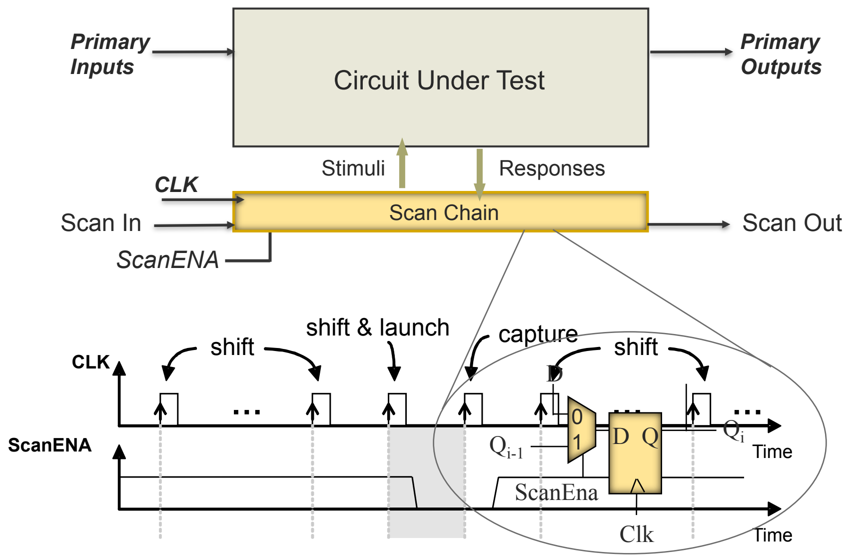
Basics on Test - DfT



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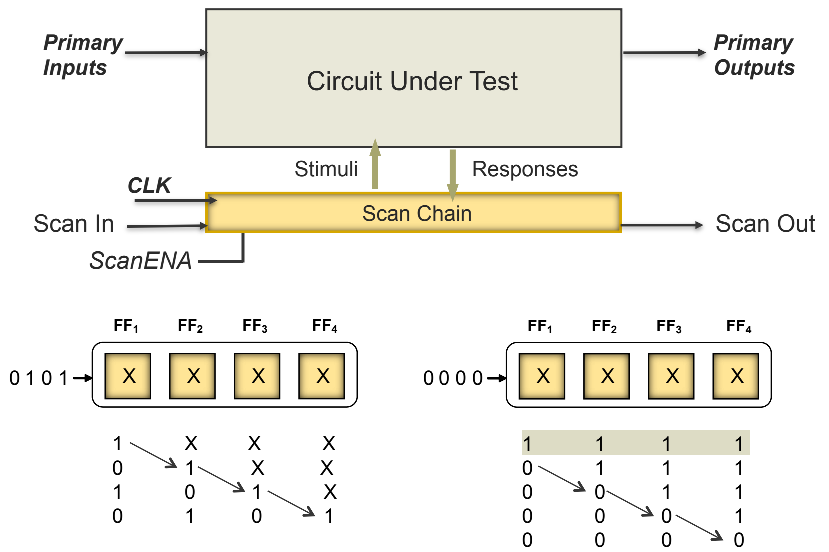
Basics on Test - DfT



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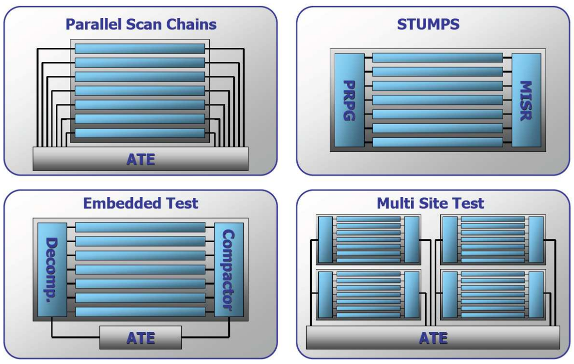
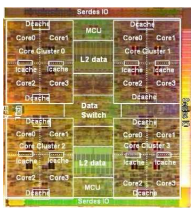
Basics on Test - DfT





Example (presented @ ITC 2008):

- 16 core CMT microprocessor from Sun Microsystems
- 410 millions of transistors, 250W @ 2.3GHz, 1.2V
- **1.35 millions of flip-flops, all are scannable !!**

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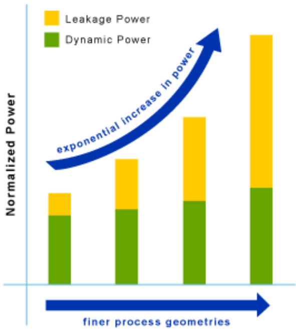
Power Consumption in CMOS

Switching (dynamic) Power

- Due to charge/discharge of load capacitance during switching
- $P_{DYN} \propto V_{DD}^2 . F_{CLK}$

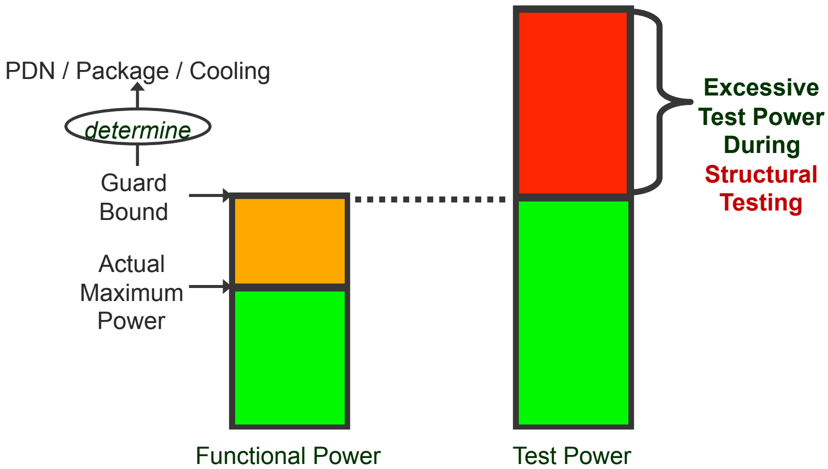
Leakage (static) Power

- Power consumed when the circuit is idle
- Mainly due to sub-threshold leakage
- $I_{SUB} \propto V_{DD} / V_{TH}$



Power During Test …

Much higher than during functional operations



Power During Test …

Much higher than during functional operations

(presented by TI & Siemens AG @ ITC 2003)
ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM

Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%

(Presented by Freescale @ ITC 2008)
Power under test mode up to 3.8X power during functional mode

And many other industrial experiences reported in the literature …

Power During Test …

Main reasons for excessive test power

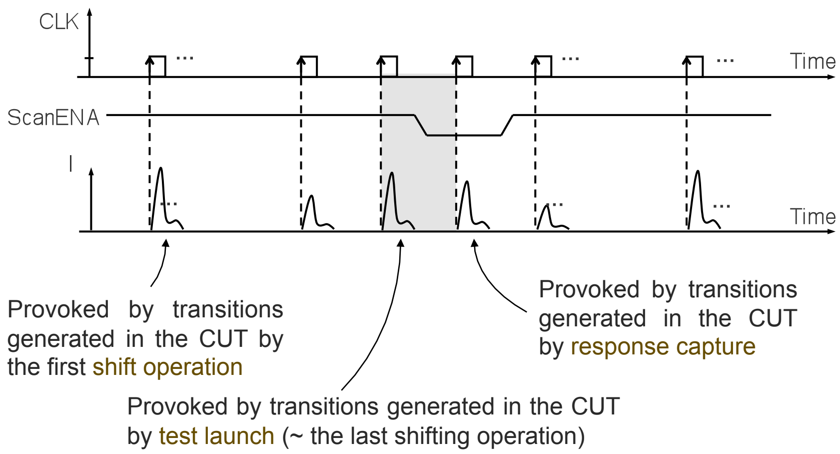
- No correlation between consecutive test vectors
- Test vectors may ignore functional (especially power) constraints
- Non-functional clocking during test
- DFT (e.g. scan) circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction

For conventional (non low-power) designs, dynamic power is the main responsible for excessive test power !!

Leakage power is a real issue during IDDQ test (reduced sensitivity) and during burn-in test (can result in thermal runaway condition and yield loss)

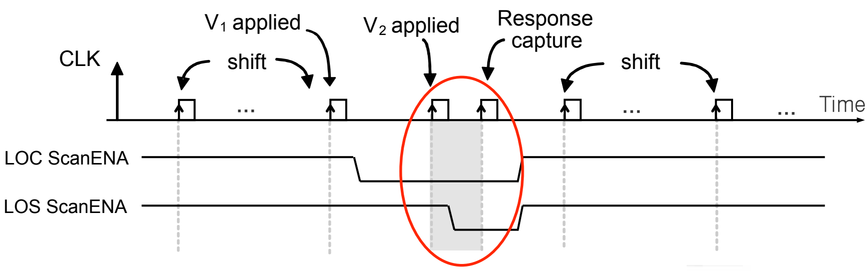
Power During Test …

Conventional (slow-speed) scan testing



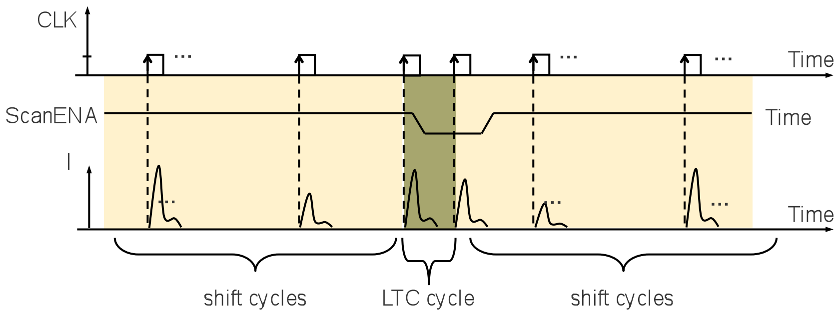
Power During Test …

At-speed scan testing with a LOC/LOS scheme



- Used to test for timing faults often caused by resistive defects
- Need of two-vector test patterns to provoke transitions
- Commonly used in microprocessor test
- **Example**: quad-core AMD Opteron processor (presented @ ITC 2008)

Power During Test …



- The problem of excessive power during scan testing can be split into two sub-problems: excessive power during the shift cycles and excessive power during the Launch-To-Capture (LTC) cycle

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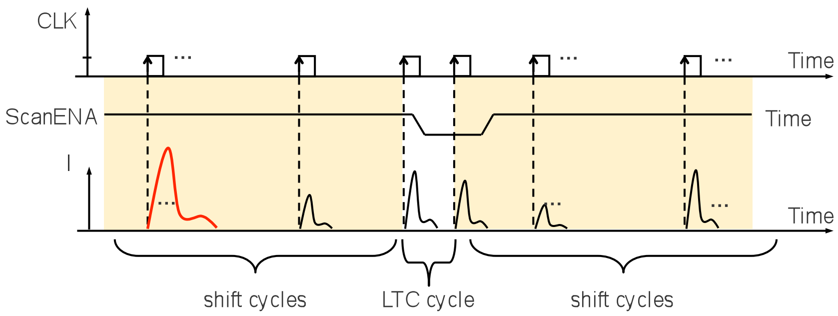
Power During Test …



- Excessive power during the shift cycles:
  - no value has to be captured/stored
  - **one peak is not relevant**

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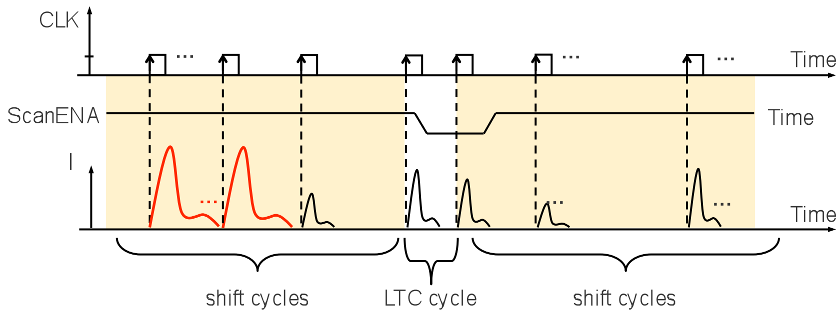
Power During Test …



- Excessive power during the shift cycles:
  - more than one peak → relates to **high average power**
  - **problems may occur**

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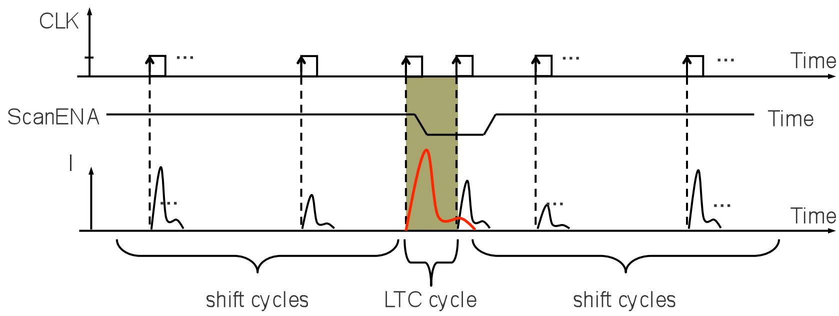
Power During Test …



- Excessive power during the LTC cycle:
  - logic values have to be captured/stored
  - **one peak is highly relevant**

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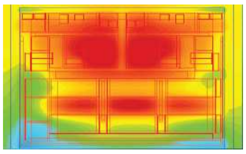
Main Test Power Issues

Elevated Average Power

↓

Temperature Increase $T_{die} = T_{air} + \theta \times P_{Average}$



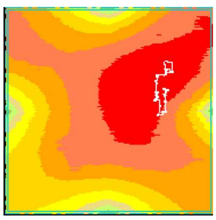
↓

Excessive Heat Dissipation

Structural degradations	Hot-Carrier-Induced Defects Electro-migration Dielectric Breakdown	Temperature variations Timing variations different from functional mode
↓	↓	↓
Chip Damage	**Reduced Reliability**	**Yield Loss**

Main Test Power Issues

- **Thermal hot-spot** results from localized overheating due to non-uniform spatial on-die power distribution
- Thermal hot-spot are likely to increase during package testing since test power dissipation can be high
- Main impact on the carrier's mobility $\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-k_1}$
- Slow down the device in the thermal hot-spot affected region of the chip
- Increase gate delays → yield loss
- Structural degradation → permanent damage !



Main Test Power Issues

Elevated Average Power
(temperature increase, excessive heat dissipation)

↓

Low Allowable Parallelism
(Wafer Testing & Package Testing)

Reduced Test Frequency
(Wafer Testing & Package Testing)

↓

Low Test Throughput
(longer test time)

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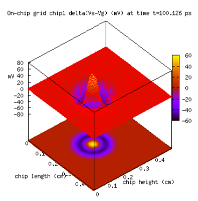
Main Test Power Issues



High Instantaneous Current

↓

Elevated Peak Power

↓

Power Supply Noise (IR-Drop, Ldi/dt)

↓

Significant Delay Increase due to Excessive PSN

↓

Erroneous Behavior Only During Testing (test fail)

↓

Manufacturing Yield Loss
(Over-Kill)

As huge designs can be manufactured today, most power-related test issues (during scan) are due to excessive peak power

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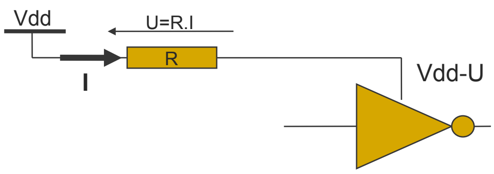
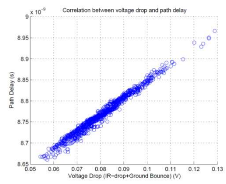
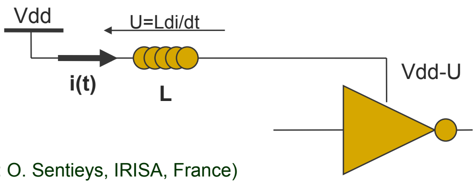
Main Test Power Issues

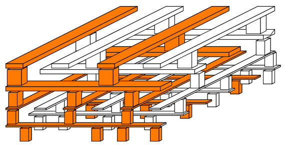
- **IR Drop** refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a resistance between the PDN source and the Vdd (Gnd) node of the gate





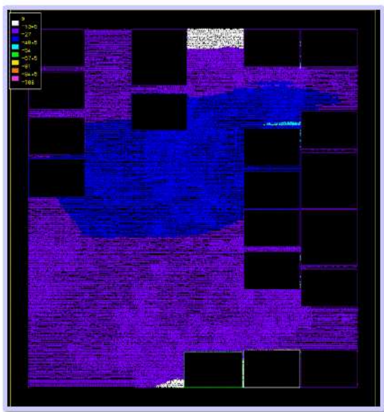
- **L(di/dt)** due to abrupt changes in current in short time (during switching) through inductive connections



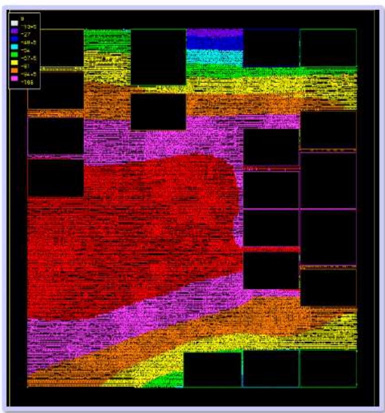


(courtesy: O. Sentieys, IRISA, France) 23

Main Test Power Issues



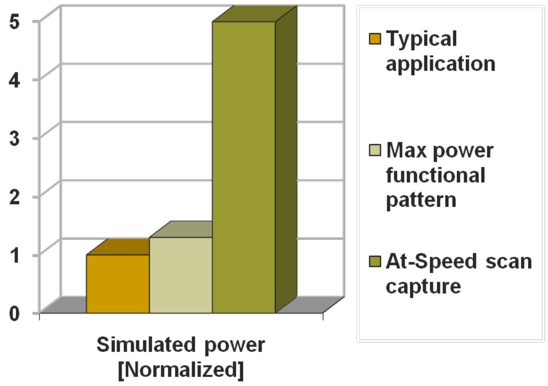
Voltage drop in functional mode



Voltage drop in test mode

(courtesy: A. Domic, Synopsys , USA) 24

Main Test Power Issues

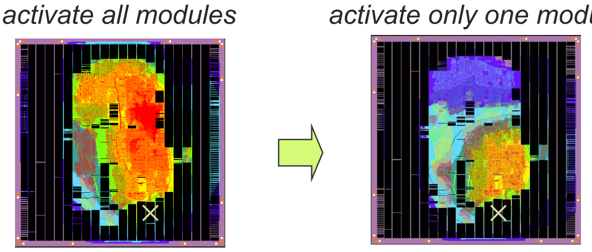


- Voltage drop: the main suspect for increased delay during capture
- Presented by Freescale @ ITC 2008

Main Test Power Issues

- Local IR-drop can be an issue even though total test power is reduced

activate all modules *activate only one module*



peak: 1.2V ® 1.026V (176mV(14.5%) drop)

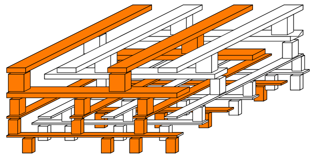
peak: 1.2V ® 1.029V (171mV(14.3%) drop)

(courtesy: K. Hatayama, STARC, Japan)

Reducing Test Power

Straightforward Solutions

- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing power distribution network (PDN)
  - Grid Sizing based on functional power requirements
  - all parts not active at a time
  - Grid Sizing for test purpose too expensive !!



Costly or longer test time

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Reducing Test Power

Main classes of dedicated solutions

- Test Data Manipulation for Power Reduction
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

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Reducing Test Power

Main classes of dedicated solutions

- Test Data Manipulation for Power Reduction
- Design for Test Power Reduction
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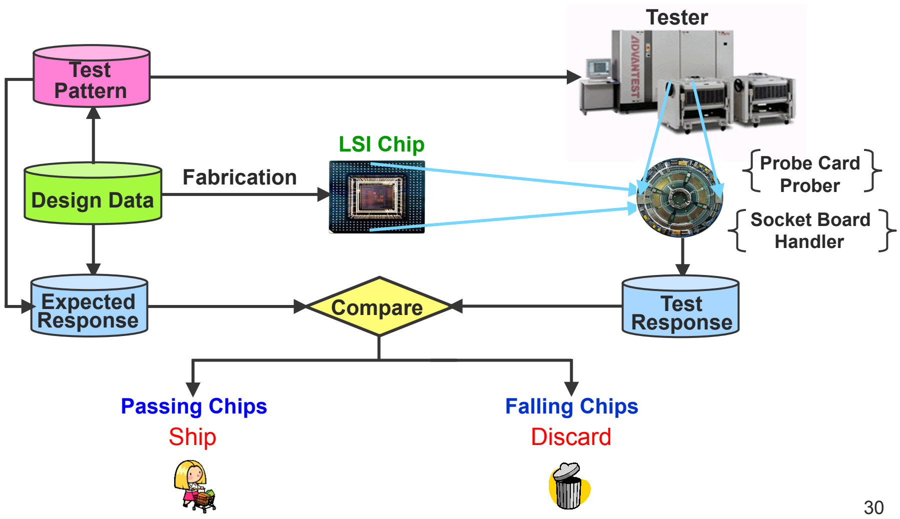
Low-Power Test Pattern Generation

Test Data Preparation in Test Flow



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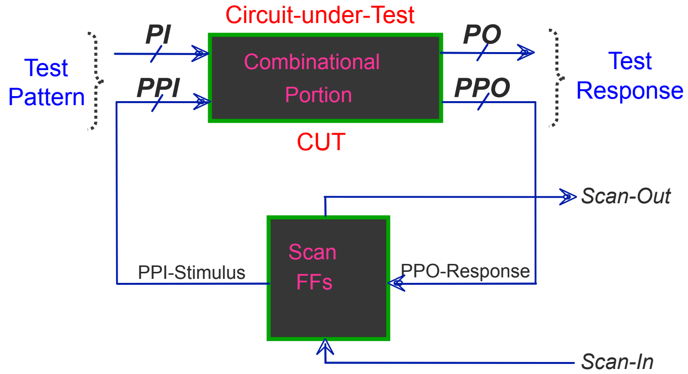
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation



- Basic Idea of Test Pattern Generation: Assume a fault in CUT, and find logic value assignments to some inputs (PI / PPI) so that the faulty (with the fault) and fault-free (without the fault) CUT create different responses on at least one output (PO / PPO).

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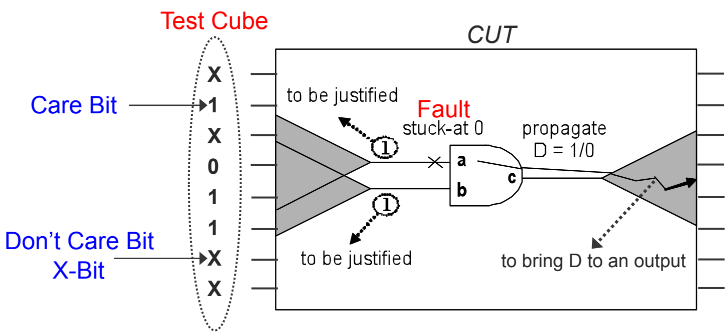
Low-Power Test Pattern Generation

Automatic Test Pattern Generation (ATPG)



- ATPG is based on complex algorithms and is used to generate a sequence of test vectors for a given CUT based on a specific fault model.
- Not all input bits need to be assigned with logic values in order to detect a fault.
- The immediate result of ATPG is a test cube, which contains both specified bits (care bits) and unspecified bits (don't care bits or X-bits).

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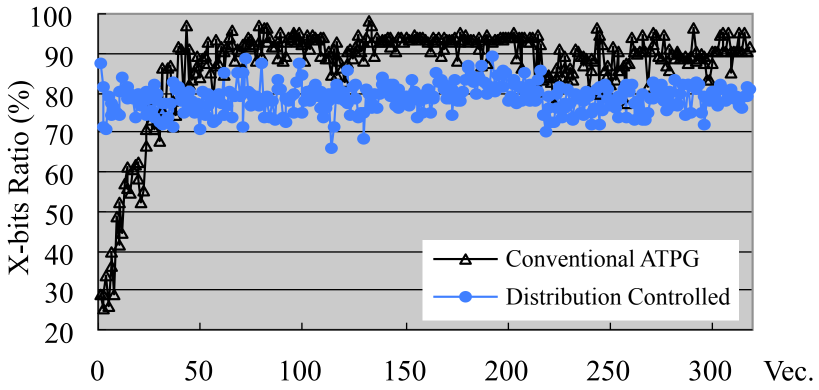
Low-Power Test Pattern Generation

X-Bits in Test Cubes

(Test Chip from STARC: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)



- A large percentage of input bits in a test cube are don't care bits (X-bits).
- Need X-filling (*i.e., assigning logic values to X-bits*) to create complete test patterns.

Low-Power Test Pattern Generation

Conventional X-Filling: Random-Fill

- Conventionally, X-bits in a test cube are filled with random logic values.
- Advantages → *small test pattern count due to "fortuitous detection"*
- Disadvantage → *high test (shift and capture) power*

Low-Power Test Pattern Generation

Various Low-Power X-Filling Techniques

Low-Shift-Power X-Filling ✓		
Shift-In Power Reduction	Shift-Out Power Reduction	Total Shift Power Reduction
0-fill *1-fill* *MT-fill* *adjacent fill / repeat fill*	*output-justification-based X-filling*	*MTR-fill*
Low-LTC-Power X-Filling ✓		
FF-Oriented	Node-Oriented	Critical-Area-Oriented
PMF-fill *LCP-fill* *preferred fill* *JP-fill* *CTX-fill*	*PWT-fill* *state-sensitive X-filling*	*CCT-fill*
Low-Shift-and-LTC-Power X-Filling ✓		
impact-oriented X-filling	*hybrid X-filling*	*bounded adjacent fill*
Low-Power X-Filling for Compressed Scan Testing		
0-fill	*PHS-fill*	*CJP-fill*

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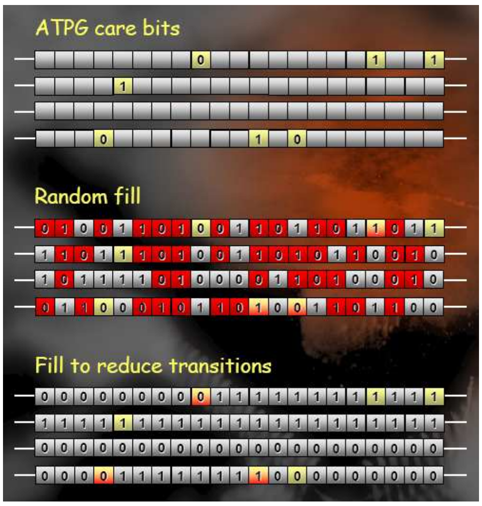
Low-Power Test Pattern Generation

Example 1: Low-Shift-Power X-filling



- From a set of deterministic test cubes, the goal is to assign proper logic values to don't care bits (X-bits) so that the occurrence of transitions in scan chains (and hence also in the combinational logic) is minimized.
- Popular techniques include 0-fill, 1-fill, MT-fill, and adjacent-fill.
- Mostly shift-in power is reduced. Occasionally, shift-out power and capture power are also reduced.
- Presented by TI at International Test Conference 2003.
- No area overhead but may increase test pattern count.

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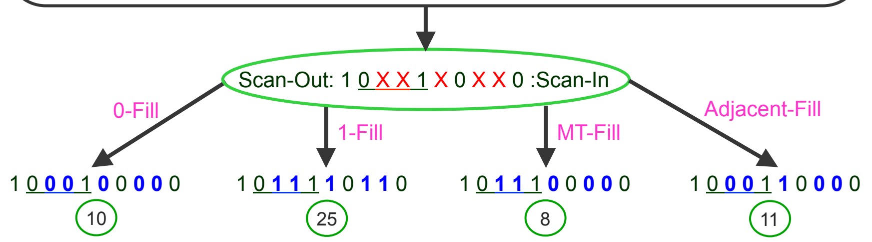
Low-Power Test Pattern Generation

Example 1 (cont'd): Low-Shift-Power X-filling

- 0-Fill → Fill all *X*-strings with 0.
- 1-Fill → Fill all *X*-strings with 1.
- MT-Fill → If the specified bits on both sides of an *X*-string have the same logic value, the *X*-string is filled with that logic value; if the specified bits on the two sides of an *X*-string have opposite logic values, the *X*-string is filled with an arbitrary logic value.
- Adjacent-Fill → Fill an *X*-string with the nearest specified-bit in the shift direction.



- Available from all commercial ATPG tools.

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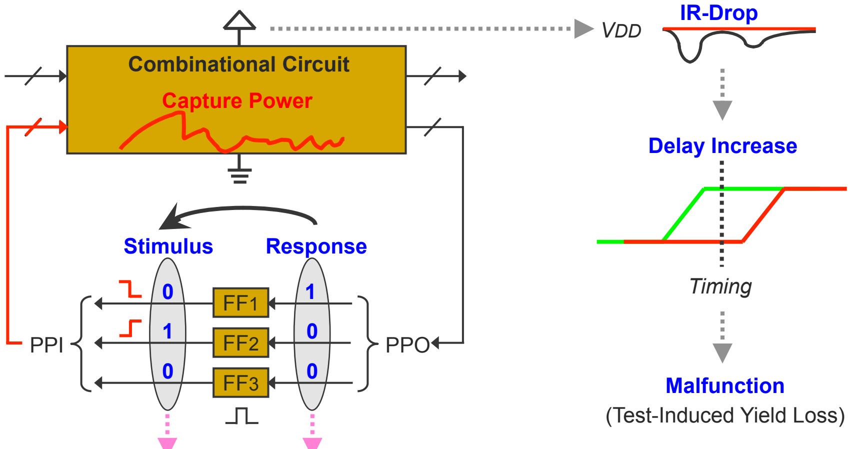
Low-Power Test Pattern Generation

Example 2: Low-LTC-Power X-Filling



To minimize the Hamming distance between PPI and PPO

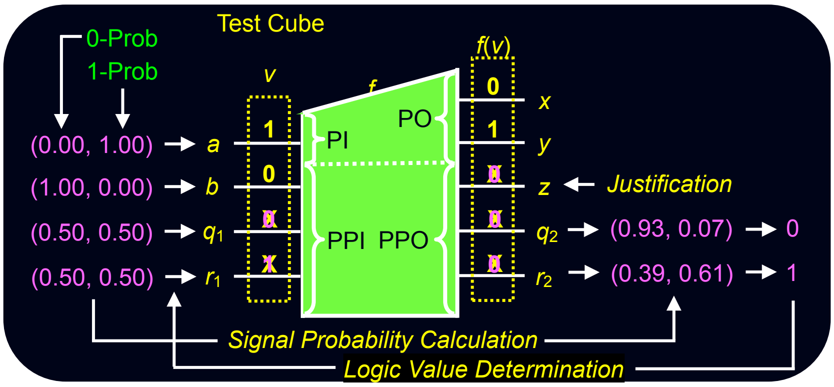
Low-Power Test Pattern Generation

Example 2 (cont'd): Low-LTC-Power X-Filling

	a b c
v_1	1 1 ***X***
v_2	1 ***X*** 1
v_3	***X*** 1 ***X***

JP X-Filling →

	a b c
v_1	1 1 **1**
v_2	1 **1** 1
v_3	**0** 1 **1**



- Implemented in SynTest ATPG tool.

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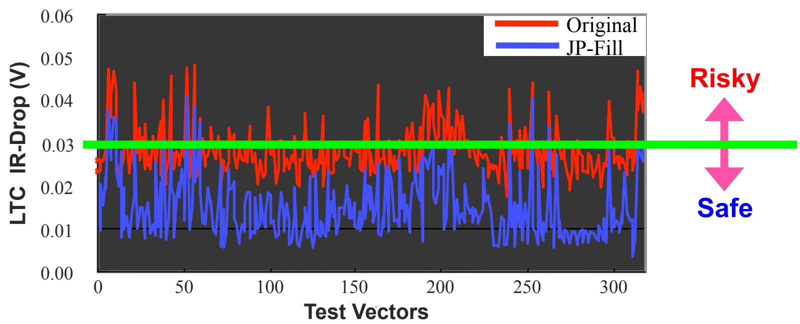
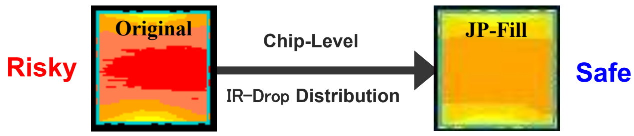
Low-Power Test Pattern Generation

Example 2 (cont'd): Low-LTC-Power X-Filling

(Test Chip from STARC: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)





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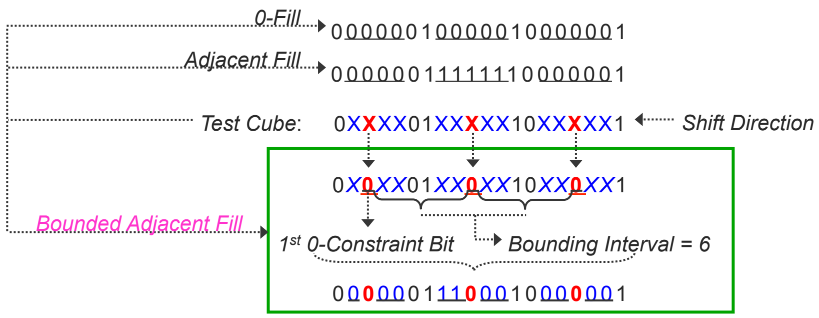
Low-Power Test Pattern Generation

Example 3: Low-Shift-&-LTC-Power X-Filling



- The basic idea is to first set several *X*-bits in a test cube to 0 and then conduct *adjacent fill*.

➔ *The occurrence of 0 in the resulting fully-specified test vector is increased, which helps reduce shift-out and capture power.* → *making use of the benefit of 0-fill*

➔ *At the same time, applying adjacent fill helps reduce shift-in power.*

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Synopsys: (*A. Chandra et. al., Proc. VTS, pp. 131-138, 2008*)

Low-Power Test Pattern Generation

Summary

- A large portion of input bits are X-bits in test cubes even after aggressive test compaction in ATPG.
- X-bits can be used for reducing various test power.
- X-filling-based low-power test generation causes no area overhead and performance degradation.
- Most commercial ATPG tools now support low-power X-filling.
- Test pattern count may increase due to low-power X-filling. This problem can be solved by conducting test power analysis to identify high-test-power test patterns and conducting X-filling only for these patterns.

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Reducing Test Power

Main classes of dedicated solutions

- Test Data Manipulation for Power Reduction
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

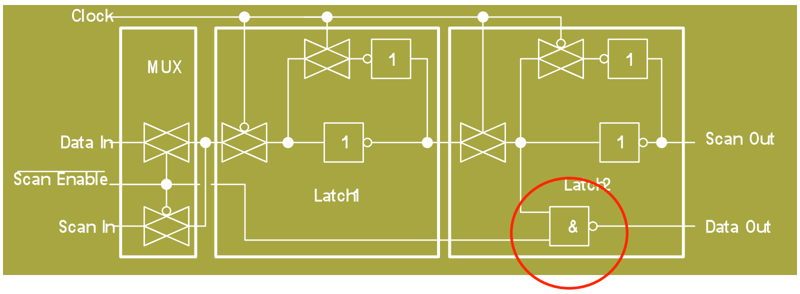
Design for Test Power Reduction

During scan testing (standard or at-speed):

Shift Power Reduction	LTC Power Reduction
• **Shift Impact Blocking** - *blocking gate, special scan cell* - *first-level power supply gating* • **Scan Chain Modification** - *scan cell reordering* - *scan chain segmentation* - *scan chain disable* • **Scan Clock Manipulation** - *splitting, staggering* - *multi-duty clocking*	• **Partial Capture** - *circuit modification* - *scan chain disable* - *one-hot clocking* - *capture-clock staggering*

Design for Test Power Reduction

Example 1 : Low power scan cell



- Master-slave structure of a mux-D flip-flop is modified
- Gate the data output during shift
- Toggle suppression during shift
- But modification of all flip-flops → impact on area and performance

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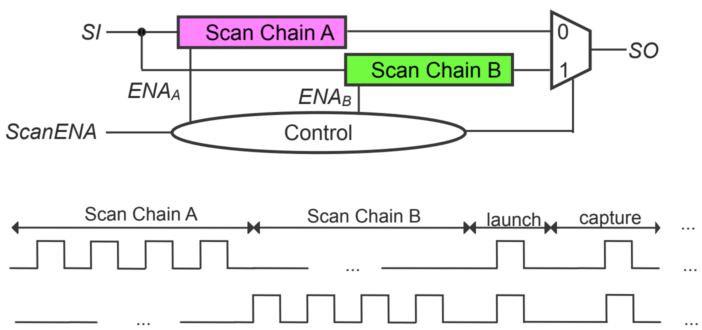
Design for Test Power Reduction

Example 2 : Scan chain segmentation



- Controllable and data-independent effect of shift power reduction
- No change to ATPG and no increase in test application time
- Presented (and used) by TI @ ITC 2000

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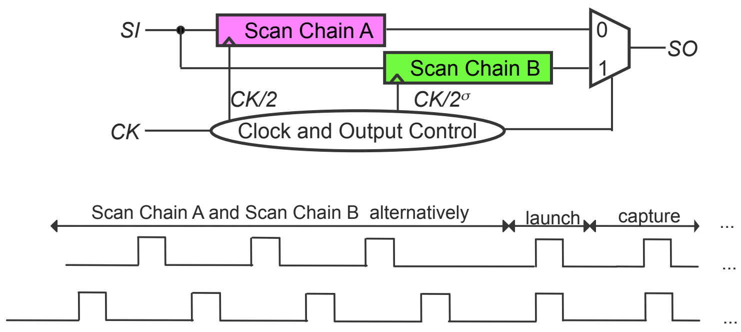
Design for Test Power Reduction

Example 3 : Staggered clocking



- The original scan chain is segmented into two new scan chains
- Each scan chain is driven by a clock whose speed is half of the normal speed
- At each clock cycle, only half of the circuit inputs can switch

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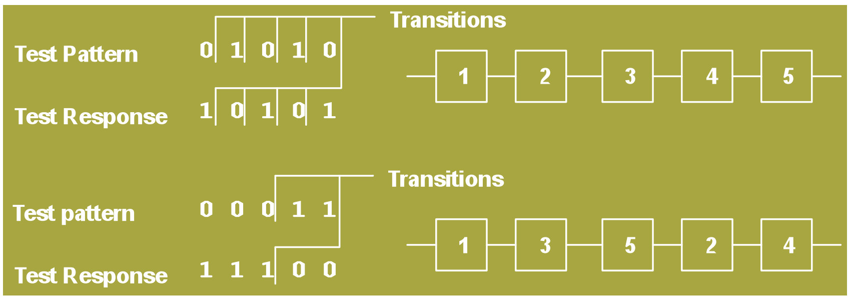
Design for Test Power Reduction

Example 4 : Scan cell reordering



- Scan cell order influences the number of transitions
- Need to change the order of bits in each vector during test application
- No overhead, FC and test time unchanged, low impact on design flow
- May lead to routing congestion problems …

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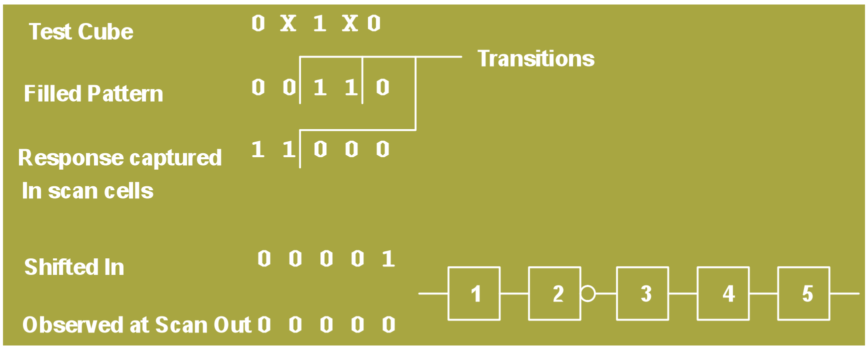
Design for Test Power Reduction

Example 5 : Inserting logic into scan chains



- The goal is to modify the transition count during shift

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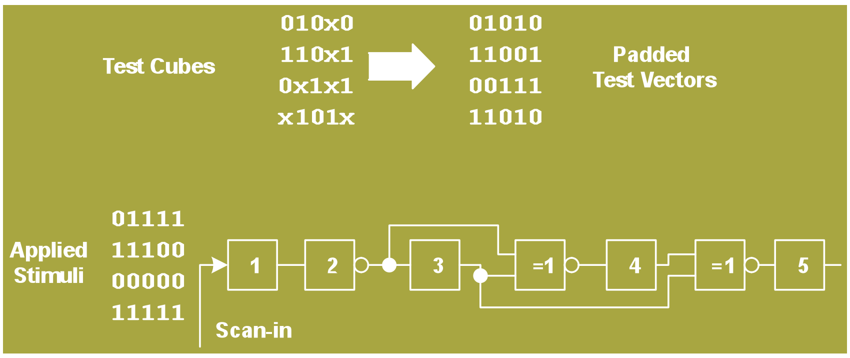
Design for Test Power Reduction

Example 6 : Scan segment inversion



- This is done by embedding a linear function in the scan path
- Reduces the transition count in the scan chain

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Reducing Test Power

Main classes of dedicated solutions

- Test Data Manipulation for Power Reduction
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

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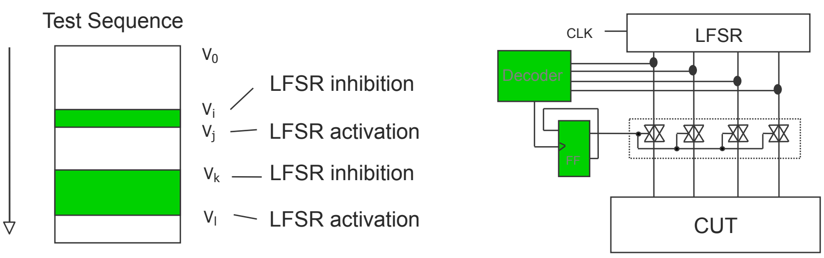
Power-Aware BIST and Compression

Example 1: Masking logic insertion during BIST



Prevent application of non-detecting (but consuming) vectors to the CUT. A decoder is used to store the first and last vectors of each sub-sequence of consecutive non-detecting vectors to be filtered.

Minimizes average power without reducing fault coverage

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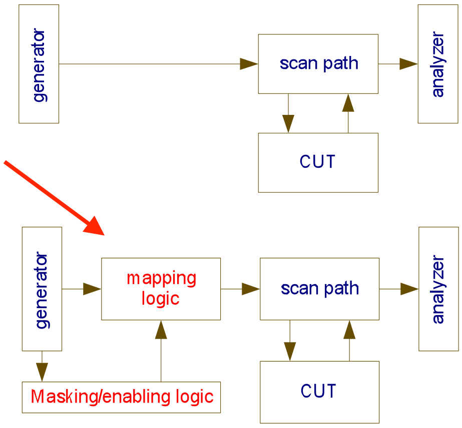
(based on P. Girard et. al., Proc. VTS, pp. 407-412, 1999)

Power-Aware BIST and Compression

Example 2: Adaptation to Scan-Based BIST

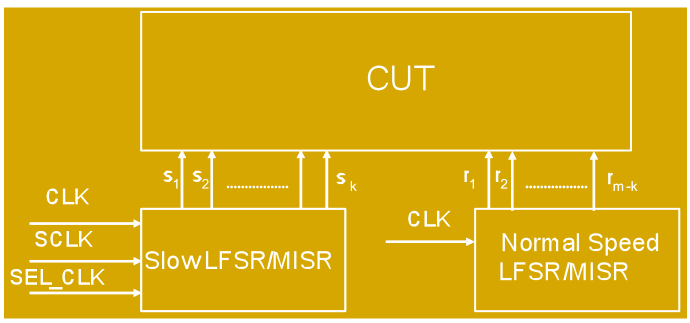
Masking/enabling logic filters the non-essential vectors and mapping logic can improve the correlation of the values on the generator output



(based on F. Corno et. al., Proc. DFT, pp. 219-226, 1999)

Power-Aware BIST and Compression

Example 3: Dual-Speed LFSR



(based on S. Wang and S. Gupta., Proc. ITC, pp. 848-857, 1997)

Power-Aware BIST and Compression

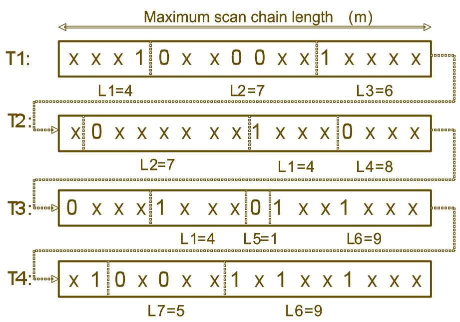
Example 3 (cont'd): Dual-Speed LFSR

	Partitioned → S	N	Reordered → S	N
0001	00	01	01	01
1000	10	00	01	10
0100	01	00	01	11
0010	00	10	01	00
1001	10	01	10	01
1100	11	00	10	10
0110	01	10	10	11
1011	10	11	10	00
0101	01	01	11	01
1010	10	10	11	10
1101	11	01	11	11
1110	11	10	11	00
1111	11	11	00	01
0111	01	11	00	10
0011	00	11	00	11
0000	00	00	00	00

(based on S. Wang and S. Gupta., Proc. ITC, pp. 848-857, 1997)

Power-Aware BIST and Compression

Example 4: Coding for compression and test power



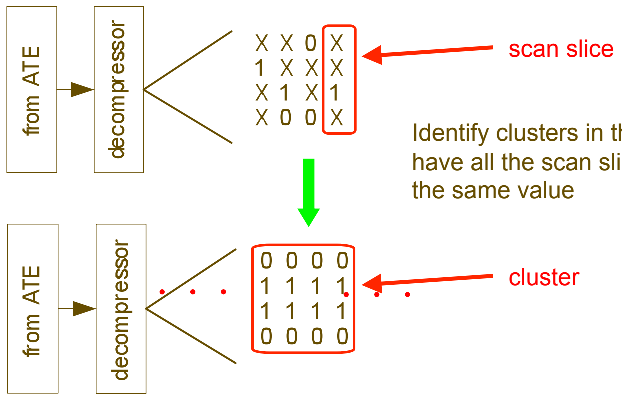
	Characters (Li)	Occurrence Frequency (fi)	Huffman Code (Ci)	Saving (Si)
N_1	4	3	00	+6
	9	2	010	+12
	7	2	011	+8
	5	1	100	+2
	8	1	101	+5
	6	1	110	+3
	1	1	111	-2
				S=+34

(based on K. Chakrabarty and S.K. Goel, Duke Univ)

Power-Aware BIST and Compression

Example 5: Linear Finite State Machines

Conventional EDT does random filling



Identify clusters in the test cube that can have all the scan slices mapped onto the same value

Push the decompressor in self-loop states during encoding for low-power fill

(based on F. Czyusz et. al., Proc. VTS, pp. 75-83, 2007)

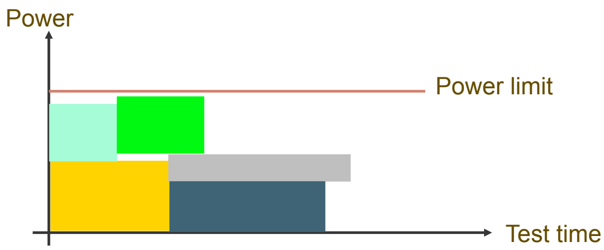
Reducing Test Power

Main classes of dedicated solutions

- Test Data Manipulation for Power Reduction
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

System-Level Power-Aware Scheduling

Improve Test Throughput by Exploiting Design Modularity

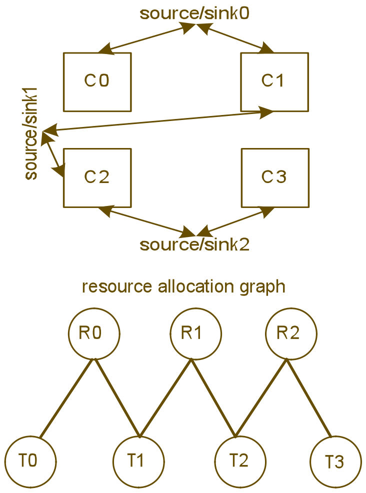


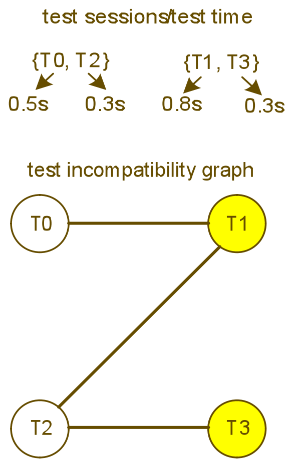
- The goal is to determine the blocks (memory, logic, analog, etc.) of an SOC to be tested in parallel at each stage of a test session in order to keep power dissipation under a specified limit while optimizing test time
- Some of the test resources (pattern generators and response analyzers) must be shared among the various blocks

(based on Y. Zorian, Proc. VTS pp. 4-9, 1993)

System-Level Power-Aware Scheduling

Example 1: Resource Allocation and Incompatibility Graphs

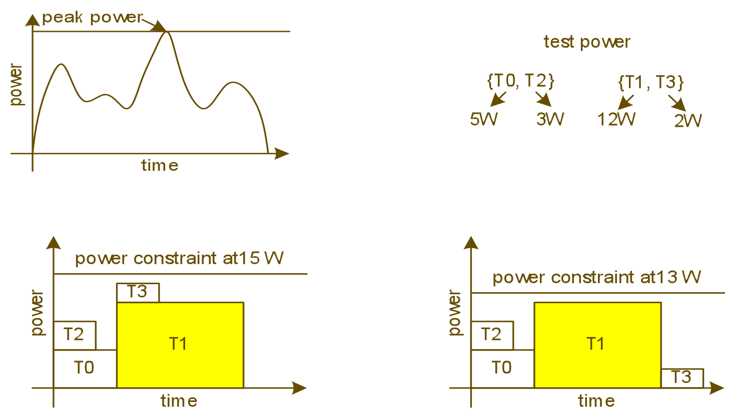




(based on R. Chou et. al, IEEE Trans on VLSI, Vol. 5, No. 2, pp. 175-185 , 1997)

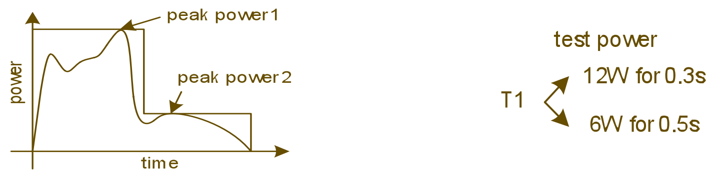
System-Level Power-Aware Scheduling

Example 1 (cont'd): Power Model and Test Schedule

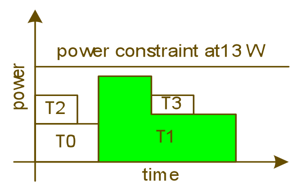


System-Level Power-Aware Scheduling

Example 2: Power Profile Manipulation

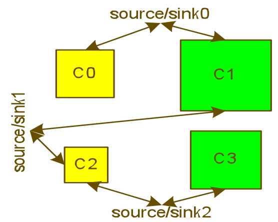


Power profile can be modified by pattern modification and/or test set reordering



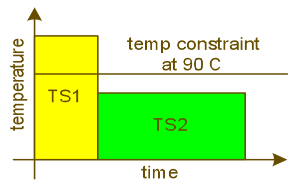
System-Level Power-Aware Scheduling

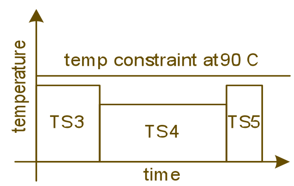
Example 3: Thermal Considerations



temperature dependent test

- TS1 = {T0, T2} → 130 C
- TS2 = {T1, T3} → 70 C
- TS3 = {T0, T3} → 80 C
- TS4 = {T1} → 60 C
- TS5 = {T2} → 80 C





Evaluating …

… Test Power Reduction Strategies

- Power reduction effectiveness — *High*
- Fault coverage impact — *Low*
- ATPG engine impact — *Minimum*
- Test data volume impact — *Low*
- Test time impact — *Low*
- Functional timing impact — *Low*
- Area overhead — *Low*
- Usability with test compression — *High*
- Design effort — *Minimum*
- Design flow change — *Low*

(source: S. Ravi, TI, ITC07)

Test Power Estimation

- Needed for test space exploration (DfT/ATPG) early in the design cycle
- Availability of scan enhanced design and ATPG patterns only at the gate level in today's design flows imposes the usage of gate-level estimators for test power
- Conventional flow adopted to perform estimation is simulation-based
- Estimation is performed at various PVT corners
- Challenges for multi-million gate SoCs
  - Time-consuming !!
  - Dump sizes can be very large !!
- The weighted transition metric (WSA) is quick but approximate

Faster and low cost solutions for test power estimation are needed !

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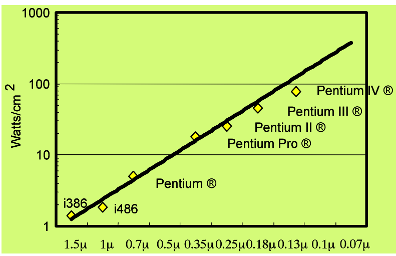
Low Power Design (LPD)

Power Consumption Trends

- Exponential growth in transistor density
  - More functionality
- But linear reduction in supply voltage
  - Not adequate to prevent power density to increase



(Tirimurti et al., DATE, 2004)

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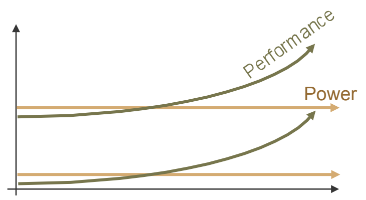
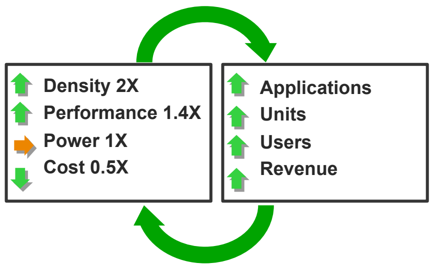
Low Power Design (LPD)

The new power-performance paradigm:

- Low (fixed) power budget to limit power density
- But ever increasing integration and performance …





Adoption of low-power design and power management techniques

(courtesy: M. Hirech, Synopsys , USA)

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Low Power Design (LPD)

System & Architecture	IC Design & Implementation
▪ Voltage / Frequency Scaling ▪ Architecture (parallel, well managed pipeline, etc.) ▪ Others (H/S partitioning, instruction set, algorithms, etc.)	▪ Clock Gating ▪ Multiple Supply Voltage ▪ Multiple Threshold Voltage ▪ Substrate-Bias ▪ Power Gating ▪ Others
Circuit (Logic) Design	**Process Technology**
▪ Low Power Cell Library ▪ Gate sizing (to equalize paths) ▪ Buffer insertion to reduce slew ▪ Logic restructuring to avoid hazards ▪ Memory Bit Cell and Compiler ▪ Others	▪ Reduce Vdd ▪ Threshold Voltage Option ▪ Low Capacitance Dielectric ▪ New Gate Oxide Material ▪ Transistor Sizing ▪ Others

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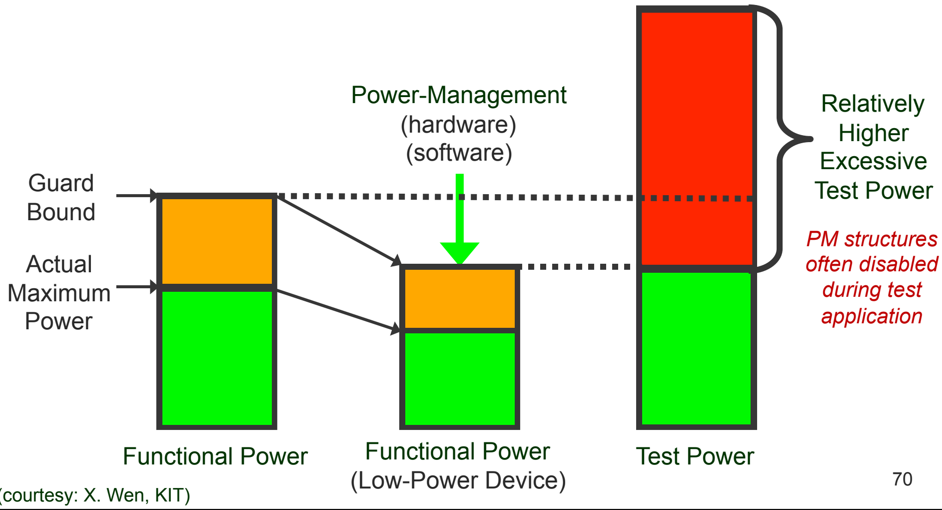
Low Power Design (LPD)

Main LPD techniques	Power reduction	
	Dynamic	Leakage
Clock gating	✓	
Power gating	✓	✓
Multi-Voltage domains	✓	
Multi-Threshold cells		✓

These techniques are often combined together to achieve the maximum power optimization value

Power During Test …

Even more critical for Low-Power Design !!



(courtesy: X. Wen, KIT)

Requirements for Test of LPD

- Reduce (even more) test power by using the power management (PM) infrastructure (and/or applying the previous dedicated solutions)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures

And still target:

High fault coverage, short test application time, small test data volume, low area overhead, etc … while making test power dissipation (dynamic and leakage) comparable to functional power

Reducing Test Power of LPD

Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

Objective (again)

Make test power dissipation comparable to functional power

Reducing Test Power of LPD

Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

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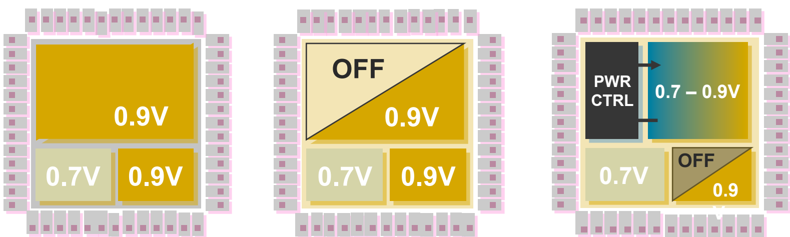
Test for Multi-Voltage Designs

Multi-Voltage Design Styles



Multi-Voltage Multi-supply | **Multi-Voltage with power gating** | **Dynamic Voltage Frequency Scaling (DVFS)**

- Creation of "power islands"
- Vdd scaling results in quadratic power reduction ($P=kV^2f$)
- Level shifters to let signals cross power domain boundaries

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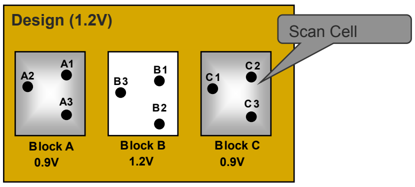
Test for Multi-Voltage Designs

Example 1: Multi-Voltage Aware Scan Cell Ordering

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93%)



Scan chain assembly

Ordering / Position	Logical	Physical	Multi-Voltage
1	A1	A2	A2
2	A2	A1	A1
3	A3	A3	A3
4	B1	B3	C1
5	B2	B1	C2
6	B3	B2	C3
7	C1	C1	B2
8	C2	C2	B3
9	C3	C3	B1

Level shifter

- Presented by Synopsys in JOLPE vol.1 n°1 April 2005 and implemented in Synopsys Galaxy™ Test

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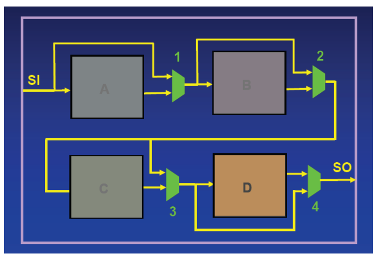
Test for Multi-Voltage Designs

Example 2: Power-Aware Scan Chain Assembly

- Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints
- Bypass multiplexers allow testing of specific power domains in MSMV environment (switched-off power domains are bypassed)
- Preserve test functionality !



- Presented by Cadence @ ITC 2008 and implemented in Cadence *Encounter*™

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Test for Multi-Voltage Designs

Example 3: Voltage scaling in scan mode

- During scan shifting, the combinational logic needs not meet timing
- Goal: re-use the DVS infrastructure in test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
- At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
  - Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan FFs (V_t) = 0.35 V, shift Frequency (F_{shift}) = 125 MHz → V_{shift} = 0.635 V
- Presented by TI @ ITC 2007

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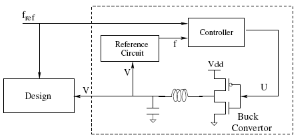
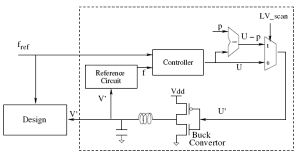
Test for Multi-Voltage Designs

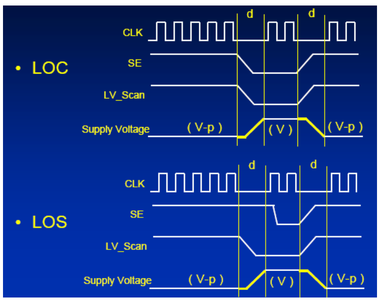
Example 3 (cont'd): Voltage scaling in scan mode



Conventional Voltage Scaling Apparatus



PMScan: Shift Voltage Scaling Apparatus



LV_scan: Control signal from tester for low-voltage scan

- Around 45% reduction of dynamic (average and peak) power and 90% reduction of leakage power, with negligible physical design impact and minimum area overhead

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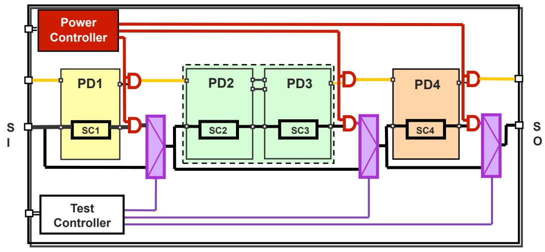
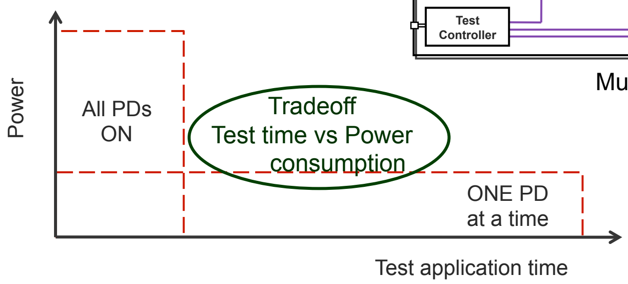
Test for Multi-Voltage Designs

Example 4: Power Domain Test Planning

Objective:
Create distinct test modes (test partitioning) for power domains



Multi-mode DFT architecture



(Source: M. Hirech, Synopsys, DATE 2008)

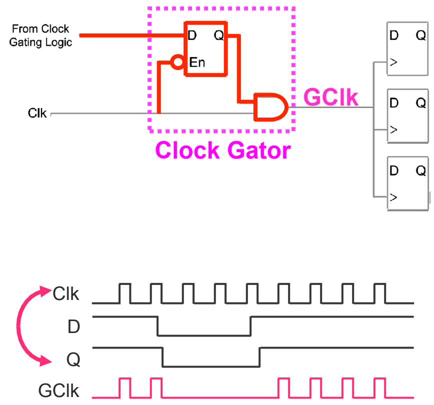
Reducing Test Power of LPD

Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

Test for Gated Clock Designs

Basic Clock Gating Design



- Not all FFs need to be triggered to perform a function (e.g., the camera control logic in a mobile-phone SoC can be inactive during a call).
- Gating-off the clock to functionally-noncontributing FFs reduces dynamic power dissipation, *not only in logic portions but also in clock trees (> 50%).*
- One of the major techniques for reducing functional power.
- Widely adopted and supported by existing EDA tools.

Test for Gated Clock Designs

Impact of Clock Gating on Test

- Clock gating prevents all scan FFs from being active at the same time.
- **Impact on Shift Mode**
  Negative → Scan shift realized through scan chains may become impossible if some FFs are inactive.

  ↓

  Shift Operation Guarantee Needed
  - *DfT for Clock Gating Logic* ✓
- **Impact on Capture Mode**
  Positive → Dynamic power can be reduced.

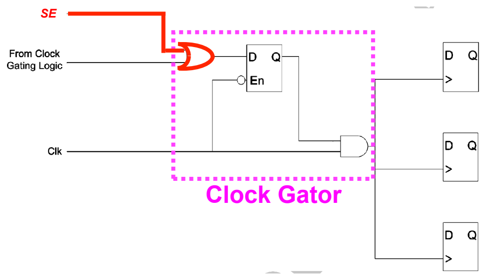
  ↓

  Good for Capture (LTC) Power Reduction
  - *Dynamic In-ATPG Techniques*
  - *Static In-ATPG Techniques* ✓
  - *Static Post-ATPG Techniques*

Test for Gated Clock Designs

Example 1: DfT for Clock Gating Logic

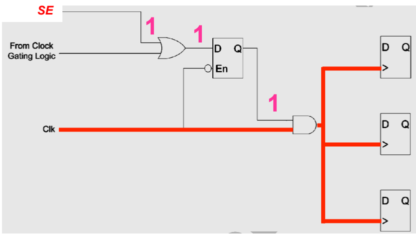
- **Shift Mode** (*SE* = 1): All scan FFs must be active to form one or more scan chains to shift-in test stimulus / shift-out test response. Clock gating logic needs to be overridden (by *SE*) in shift mode.
- **Capture Mode** (*SE* = 0): Scan FFs are allowed to be controlled by clock gating logic. Nothing needs to be done.



- Automatically implemented by Cadence and Synopsys DfT tools.

Test for Gated Clock Designs

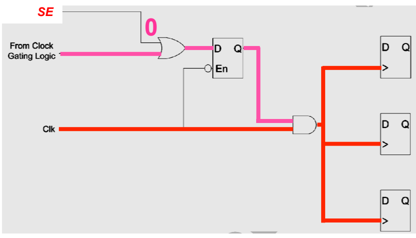
Example 1 (cont'd): DfT for Clock Gating Logic



- Disable clock gating in ***shift mode*** (*SE* = 1): Unconditionally-ON Clock

↓

Shift Register Operation



- Enable clock gating in ***capture mode*** (*SE* = 0): Conditionally-ON Clock

↓

Capture Power Reduction

Test for Gated Clock Designs

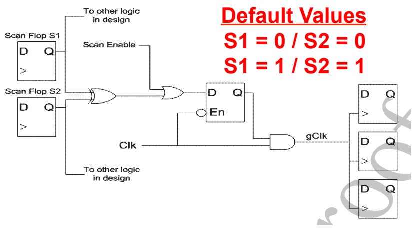
Example 2: Capture Power Reduction by Clock Gating

- A **default value** is a value to be assigned to an input in order to gate-off a clock.
  - ➔ *A preset value to be used to fill an X-bit in a test cube.*
- Flow for obtaining default values for clock gating:
  - ➔ *Identify all clock gators.*
  - ➔ *For each clock gator, calculate a set of input settings that set the clock off.*
  - ➔ *The values in each input setting are default values*
- Flow for using default values for clock gating:
  - ➔ *Generate a test cube for fault detection.*
  - ➔ *Assign default values to the X-bits in the test cube.*
    (*If there are multiple choices of default values, use the one that can turn-off more FFs.*)

Cadence: (*R. Illman et. al., Proc. LPonTR, pp. 45-46, 2008*)

Test for Gated Clock Designs

Example 2 (cont'd): Capture Power Reduction by Clock Gating



Default Values
S1 = 0 / S2 = 0
S1 = 1 / S2 = 1

Test Cubes after ATPG

Test Cubes	Scan flops in design					
	S0	**S1**	**S2**	S3	S4	S5
T1	X	**0**	**X**	1	0	X
T2	0	**1**	**X**	X	X	0
T3	X	**X**	**0**	1	0	X

Test Cubes after Assigning Default Values

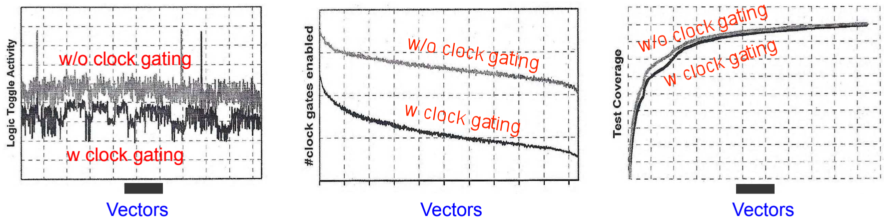
Test Cubes	Scan flops in design						Merge "default values"?
	S0	**S1**	**S2**	S3	S4	S5	
T1	X	**0**	**0**	1	0	X	Yes
T2	0	**1**	**X**	X	X	0	Conflict
T3	X	**0**	**0**	1	0	X	Yes

Cadence: (*R. Illman et. al., Proc. LPonTR, pp. 45-46, 2008*)

Test for Gated Clock Designs

Example 2 (cont'd): Capture Power Reduction by Clock Gating

Circuit Statistics
89K FFs
6 Scan Clocks
2200 Clock Gators



- The number of active clocks are reduced by more than 50%.
- Capture toggle activity is reduced by 35%.
- Fault coverage and test set size remain almost unchanged.

Cadence: (*R. Illman et. al., Proc. LPonTR, pp. 45-46, 2008*)

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Test for Gated Clock Designs

Summary

- Functional clock gating is indispensable in reducing dynamic power.
- Functional clock gating logic needs to be modified in order to guarantee correct operation in *shift mode*.
- Clock gating can be used in *capture mode* to reduce capture power.

➔ Static In-ATPG Techniques

(Assign pre-determined clock-gator disabling values to don't-care bits (X-bits) in a test cube initially generated for fault detection.)

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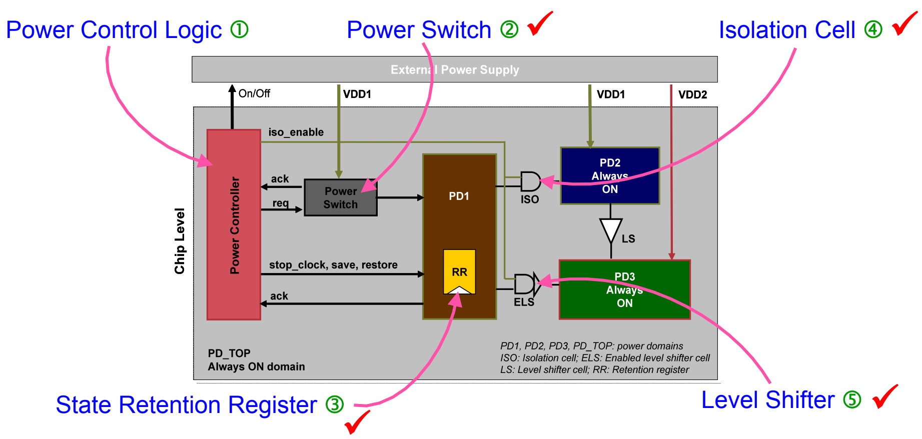
Reducing Test Power of LPD

Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

Test for Power Management Structures

Typical Power Management (PM) Structures

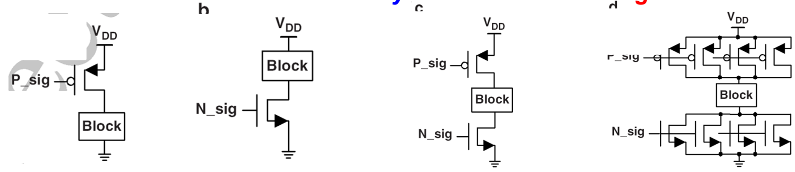


- Conditionally turning on or off the power supply of a logic block (power domain) in order to reduce both dynamic and static power.
- PM structures (①~⑤) require dedicated DfT methods and test patterns.

Test for Power Management Structures

Example 1: Test for Header Switches

Header Switch *Footer Switch* *Symmetric Switch* *Segmented Switch*



Header Switch / Footer Switch / Symmetric Switch

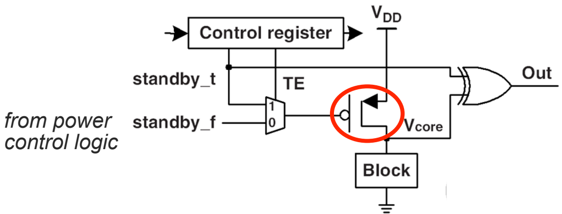
- Also called sleep transistors and used to shut down blocks (power domains) that are not in used (idle mode), hence reducing leakage power and dynamic power.
- Should be large enough to provide sufficient current to the circuit.

Segmented Switch

- Individual transistors can be small.
- Preferable in practice due to concerns about layout, design for manufacturability, and limiting inrush current when switching on a power domain.

Test for Power Management Structures

Example 1 (cont'd): Test for Header Switches

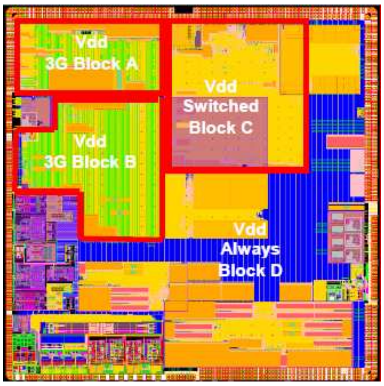


- Pattern 1 (*Test for Short*): *TE* = 1 / *standby_t* = 1
  ➔ Turn-off the power switch. After sufficient discharge, Vcore should be much lower than VDD, and thus *Out* (fault-free) = 1 / *Out* (faulty) = 0
- Pattern 2 (*Test for Open*): *TE* = 1 / *standby_t* = 0
  ➔ Turn-on the power switch. Vcore should be close to VDD, and thus *Out* (fault-free) = 1 / *Out* (faulty) = 0

NXP: (*Goal et. al., Proc. ETS, pp. 145-150, 2006*)

Test for Power Management Structures

Example 2: Parametric Test of Micro Switches



- Presented by ST-Ericson (Sophia) at International Test Conference 2008.
- Single-die 3G mobile phone base band Chip made in 65nm technology
- Includes multimedia features, such as video decoder, MP3 player, camera, games, and designed to be extremely low power.
- Rush current during power up → specific functional mode → test mode has to map functional mode !

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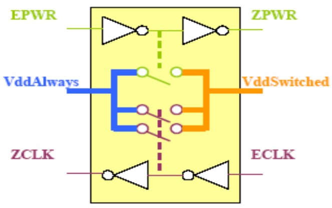
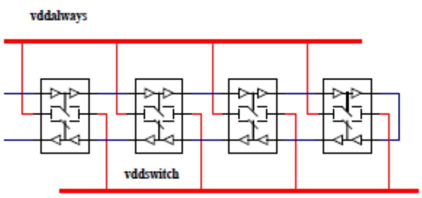
Test for Power Management Structures

Example 2 (cont'd): Parametric Test of Micro Switches





- The micro switches are daisy-chained. First, all the EPWR control signals are propagated in the chain. This gives a progressive ramp-up of the VddSwitched. Then, the ECLK control signal follows, turning 'on' all the transistors of the micro switches.
- Testing micro-switches individually is needed to detect resistive defects in each of them, and testing the micro switches' control chain is important to ensure the chain is not broken.

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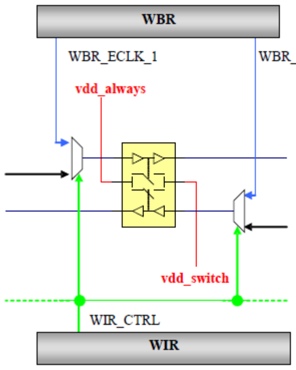
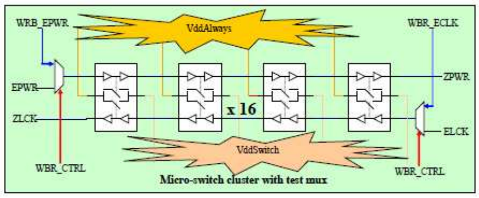
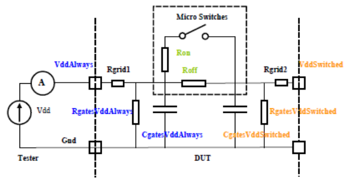
Test for Power Management Structures

Example 2 (cont'd): Parametric Test of Micro Switches



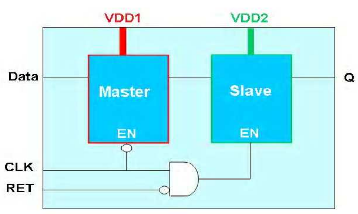




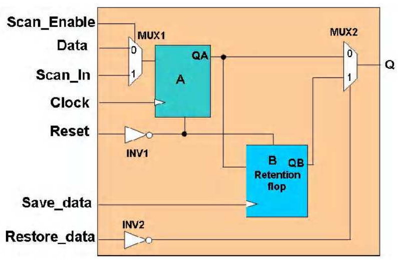
- DfT to add controllability and observability
- Test environment modeling needed to allow R_{off}/R_{on} measurement
- Test time for 150 clusters (each composed of 16 switches): 36 ms

Test for Power Management Structures

Example 3: Test for State Retention Registers (SRR's)



Basic Design

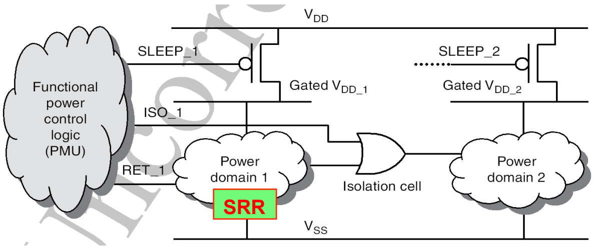


Design with Scan Function

- A SRR cell is for keeping its state when the power supply is turned off.
- Normal Mode: *VDD1* = ON / *VDD2* = ON / *RET* = 0
- Retention Mode: *VDD1* = OFF / *VDD2* = ON / *RET* = 1
- Implemented in Mentor Graphics DfT tools.

Test for Power Management Structures

Example 3 (cont'd): Test for State Retention Registers (SRR's)



Retention Capability Test

(1) Turn-on Power Domain 2 (*SLEEP_2* = 0).
(2) Shift in value *v* to SRR.
(3) Enable retention (*RET_1* = 1).
(4) Enable the isolation cell (*ISO_1* = 1).
(5) Turn-off Power Domain 1 (*SLEEP_1* = 1).
(6) Turn-on Power Domain 1 (*SLEEP_1* = 0).
(7) Disable the isolation cell (*ISO_1* = 0).
(8) Disable retention (*RET_1* = 0).
(9) Shift out the value of SRR and check if it is *v*.

Repeat for V = 0 and V = 1

Other tests, such as test for retention robustness to the state element's clock, asynchronous set/reset, etc., may also need to be applied.

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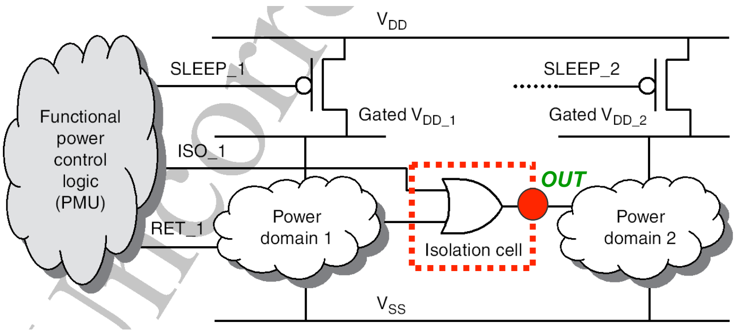
Test for Power Management Structures

Example 4: Test for Isolation Cells



(1) Turn-off Power Domain 1 (*SLEEP_1* = 1).

(2) Turn-on Power Domain 2 (*SLEEP_2* = 0).

(3) Apply a test to detect the stuck-at-0 at the output of the isolation cell.
This is done by setting 1 to *ISO_1* and checking if the isolation cell output (*OUT*) is 1.

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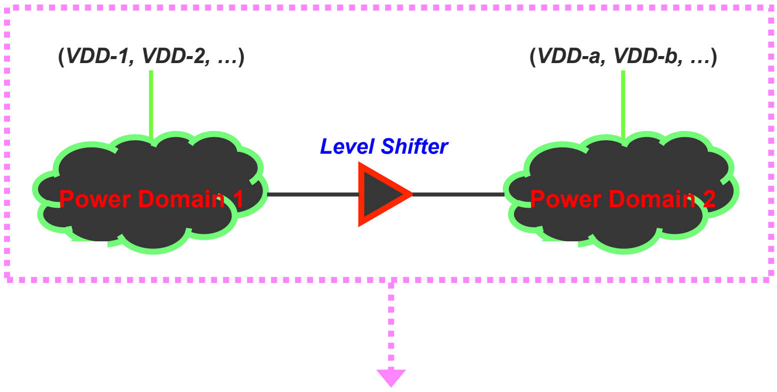
Test for Power Management Structures

Example 5: Test for Level Shifters



Test as a whole under all power supply voltage combinations of Power Domain 1 and Power Domain 2.

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Test for Power Management Structures

Summary

- More and more power management structures are used in various IC designs in order to reduce power (dynamic and static) dissipation.
- Conventional ATPG does not target power management structures, leading to potential quality problems.
- There is a strong need to fully understand the basics of various power management structures and their operation modes.
- Special considerations and even new algorithms are needed to fully test various power management structures.
  - Clock Gating Logic (Clock Gator, Control Logic)
  - Power Gating Logic
    - ➔ PMU (Power Management Unit)
    - ➔ Power Switch
    - ➔ State Retention Register, Isolation Cell, Level Shifter
  - Power Distribution Network

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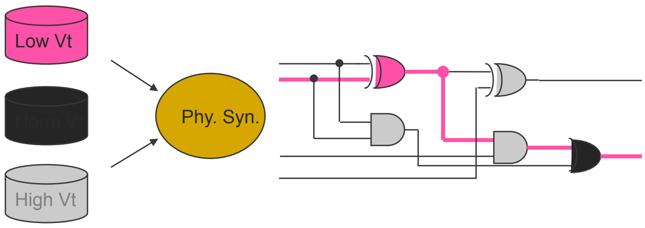
Impact of MTV Design on Test

- Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction → speed cost to decrease leakage !!
- MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)
- Leakage power reduction while meeting timing and no area overhead
- Well established and supported by existing EDA tools



(source: CADENCE, 2007)

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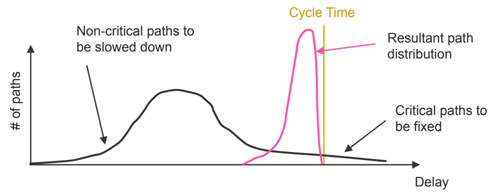
Impact of MTV Design on Test

- By using such power optimization techniques, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations
  - PDF selection more complex
  - More test data are needed
  - Sensitivity to variations



- PSN has a significant impact on the timing behavior
  - Need to integrate PSN effects in delay test pattern generation

Solutions for high quality at-speed fault coverage are needed !

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Power-Aware DFT Tools

- **Synopsys:**
  - Galaxy™ Test is a comprehensive test automation solution
  - DFT Compiler and its low power features (for more details on this tools, see "Power and Design for Test: A Design Automation Perspective", A. De Colle et al, Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, April 2005)
  - DFT MAX and its low power features (for more details on this tools, see "DFT MAX and Power", R. Kapur et al, Journal of Low Power Electronics (JOLPE), Vol. 3, N° 2, August 2007)
  - TetraMAX® and its low-power management capabilities
  - Details at http://www.synopsys.com/products/solutions/galaxy/test/

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Power-Aware DFT Tools

- **Cadence:**
  - Encounter® Test, a key technology in the Cadence® Encounter digital IC design platform
  - To support manufacturing test of low-power devices, Encounter Test uses power intent information to create distinct test modes automatically for power domains and shut-off requirements. It also inserts design-for-test (DFT) structures to enable control of power shut-off during test. The power-aware ATPG engine targets low-power structures, such as level shifters and isolation cells, and generates low-power scan vectors that significantly reduce power consumption during test. Cumulatively, these capabilities minimize power consumption during test while still delivering the highest quality of test for low-power devices
  - Details at http://www.cadence.com/products/digital_ic/encountertest/

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Conclusion

- Power consumption during Test is a real issue !!
- Not only during manufacturing test but also during on-line test
- Not only ATPG and DFT but also BIST, test compression, and test scheduling have been addressed
- No generic solution, but rather a combination of solutions. Example: power-aware DfT for reducing shift power and power-aware ATPG for reducing LTC power
- New test solutions for Low-Power Design that preserve test functionality are needed !!

Thank You !