Power-Aware Testing and Test Strategies for Low Power Devices

Patrick Girard, Nicola Nicolici, Xiaoqing Wen

To cite this version:

Patrick Girard, Nicola Nicolici, Xiaoqing Wen. Power-Aware Testing and Test Strategies for Low Power Devices. 2012. lirmm-00820718

HAL Id: lirmm-00820718

https://hal-lirmm.ccsd.cnrs.fr/lirmm-00820718

Submitted on 6 May 2013

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Tutorial Proposal

Power-Aware Testing and Test Strategies for Low Power Devices

Presenters:

Coordinating Presenter	Full name:	Patrick GIRARD
	Affiliation:	LIRMM / CNRS
	Email:	girard@lirmm.fr
	Tel:	+33 467 418 629
	Fax:	+33 467 418 500
	Address:	161 rue Ada, 34392 Montpellier, France
Co-Presenter 1	Full name:	Nicola NICOLICI
	Affiliation:	McMaster University, Department of ECE
	Email:	nicola@ece.mcmaster.ca
	Tel:	+1 (905) 525-9140
	Fax:	+1 (905) 521-2922
	Address:	1280 Main Street West, Hamilton, Ontario L8S 4K, Canada
Co-Presenter 2	Full name:	Xiaoqing WEN
	Affiliation:	Kyushu Institute of Technology, Department of CSE
	Email:	wen@cse.kyutech.ac.jp
	Tel:	+81-948-29-7891
	Fax:	+81-948-29-7651
	Address:	Kawazu 680-4, Iizuka, Fukuoka 820-8502, Japan

Information about the tutorial:

Tutorial Duration:	Full-day (6-hours) or Half-day (3 hours)
Intended Audience:	VLSI design or test professionals, EDA tool developers, academics who are planning to develop or update their course material on advanced VLSI testing, and students who are entering into the VLSI design, test or EDA fields. The prerequisite knowledge of audience only includes basic understanding of VLSI design and test, although fundamentals of manufacturing test and low-power design will also be covered in this tutorial.
Tutorial Summary:	Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.
Keywords:	Power-aware Testing, Power-Constrained Testing, Low Power Design, Power Management, Test Power Issues, Design-for-Test, Scan Testing, Built-In Self-Test, Test Data Compression, ATPG
Tutorial Program:	1. Fundamentals on VLSI Testing 1.2 Fault Models 1.3 Design for Testability 1.4 Logic Testing 2. Power Issues during Test 2.1 Power and Energy Basics 2.2 Manufacturing Test Flow 2.3 Power Delivery Issues during Test 2.4 Thermal Issues during Test 2.5 Test Throughput Problem 2.6 Manufacturing Yield Loss 2.7 Test Power Metrics and Estimation 3. Low-Power Test Pattern Generation 3.1 Low-Power ATPG 3.2 Low-Power Test Compaction

- 3.3 Low-Power X-Filling
- 3.4 Low-Power Test Ordering

4. Power-Aware Design-for-Test
    - 4.1 Power Consumption in Scan Design
    - 4.2 Low Power Scan Cells
    - 4.3 Scan Path Organization
    - 4.4 Partitioning for Low-Power

5. Power-Aware BIST and Test Data Compression
    - 5.1 Coding-Based Compression Methods
    - 5.2 LFSR-Decompressor-Based Compression Methods
    - 5.3 Broadcast-Scan-Based Compression Methods
    - 5.4 Low-Power BIST Techniques

6. Power-Aware System-Level Test Planning
    - 6.1 Introduction
    - 6.2 Core-Based Test Architecture Design and Test Planning
    - 6.3 Power Constraint Modeling, Estimation and Manipulation
    - 6.4 Power-Constrained Test Planning
    - 6.5 Low-Power Test Planning for Multiple Clock Domains

7. Low-Power Design Techniques and Test Implications
    - 7.1 Low-Power Design Trends
    - 7.2 Power Specification Formats
    - 7.3 Implications to test requirement and test cost

8. Test Strategies for Multi-Voltage Designs
    - 8.1 Test for Multi-Voltage Design: Bridge Defects
    - 8.2 Test for Multi-Voltage Design: Open Defects
    - 8.3 DFT for Multi-Voltage Designs

9. Test Strategies for Gated Clock Designs
    - 9.1 Clock Gating Logic
    - 9.2 DFT for Clock Gating Logic
    - 9.3 Taking Advantage of Clock Gating

10. Test of Power Management Structures
    - 10.1 Power Control logic
    - 10.2 Power Switches
    - 10.3 Low Power Cells

	10.4 Power Distribution Network 11. EDA Solution for Power-Aware Design-for-Test 11.1 Design Flows for Power Management 11.2 Test Automation Objectives 11.3 Integration of Power Management Techniques in Design-for-Test Synthesis Flows 11.4 Test Planning General Conclusion
Report on previous presentations of the tutorial	This tutorial has been given as a half-day tutorial at the IEEE Design Automation and Test in Europe (DATE) conference in Munich, Germany, on March 10th, 2008, at the IEEE Asian Test Symposium (ATS), Taichung, Taiwan, on November 23rd, 2009, at the IEEE Latin American Test Workshop (LATW) in Punta del Este, Uruguay, on March 28th, 2010, at the IEEE International NEWCAS Conference, in Montreal, Canada, on June 20th, 2010, at the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) in Seattle, USA, on August 1st, 2010, at the IEEE International Conference on Microelectronics (ICM), in Cairo, Egypt, on December 19th, 2010, and at the IEEE Design Automation and Test in Europe (DATE) conference in Grenoble, France, on March 14th, 2011. It was also given as a full-day tutorial at the IEEE International Test Conference (ITC) in Austin, USA, on November 2nd, 2009, and will be given at the IEEE International Test Conference (ITC) in Anaheim, USA, on September 18th, 2011. This tutorial is supported by a book on this topic published by Springer in October 2009 and edited by the tutorial presenters. Details are available at: http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4419-0927-5
Comments to the Program Committee:	This tutorial on "Power-Aware Testing and Test Strategies for Low Power Devices" is a tutorial that addresses one of the most important challenges for current and future test technologies: the management of the power consumed during test that requires dedicated test approaches. This is a hot topic with numerous research papers and case studies published every year. Based on our extensive research done in this area, we believe that sharing our knowledge through this tutorial can bring good value to test and DfT practitioners, who are facing the difficult implementation challenges caused by excessive power during test. The tutorial can be presented as a full-day or half day tutorial depending on the conference, symposium or workshop selected.

Biographies of the presenters:

Coordinating Presenter:	Patrick GIRARD received a M.S. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research), and Head of the Microelectronics Department of the LIRMM (Laboratory of Informatics, Robotics and Microelectronics of Montpellier - France). His research interests include all aspects of digital testing and memory testing, with emphasis on critical constraints such as timing and power. From 2006 to 2010, Patrick Girard was Vice-Chair of the European Test Technology Technical Council (ETTTC) of the IEEE Computer Society. He has served on numerous conference committees including ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design Automation and Test in Europe (DATE), IEEE International Test Conference (ITC), IEEE International Conference on Computer Design (ICCD), IEEE VLSI Test Symposium (VTS), IEEE European Test Symposium (ETS), IEEE Asian Test Symposium (ATS), and ACM/IEEE International Symposium on Low Power Electronic Design (ISLPED). Patrick Girard is the founder and Editor-in-Chief of the ASP Journal of Low Power Electronics (JOLPE). He is an Associate Editor of the IEEE Transactions on VLSI Systems and the Journal of Electronic Testing – Theory and Applications (JETTA - Springer). From 2005 to 2009, he was an Associate Editor of the IEEE Transactions on Computers. He is a co-editor of the book "Power-Aware Testing and Test Strategies for Low Power Devices", Springer, 2009, and a co-author of the book "Advanced Test Methods for SRAMs – Effective Solutions for Dynamic Fault Detection in Nanoscale Technologies", Springer, 2009. Patrick Girard has been involved in several European research projects (ESPRIT III ATSEC, EUREKA MEDEA, MEDEA+ ASSOCIATE, IST MARLOW, MEDEA+ NanoTEST, CATRENE TOETS) and has managed industrial research contracts with major companies like Infineon Technologies, Intel, Atmel, ST-Ericsson, STMicroelectronics, etc. He has supervised 26 PhD dissertations and has published 6 books or book chapters, 36 journal papers, and more than 150 conference and symposium papers on these fields. Patrick Girard is a Golden Core Member of the IEEE Computer Society.
Co-Presenter 1	Nicola NICOLICI is an Associate Professor in the Department of Electrical and Computer Engineering at McMaster University, Canada. He received the Dipl. Ing. degree in Computer Engineering from the "Politehnica" University of Timisoara, Romania (1997), and a Ph.D. in Electronics and Computer Science from the University of Southampton, U.K. (2000). His research interests are in the area of computer-aided design and test. He has authored over fifty research papers and one book in this area and received the IEEE TTTC Beausang Award for the Best Student Paper at the International Test Conference (ITC 2000) and the Best Paper Award at the IEEE/ACM Design Automation and Test in Europe Conference (DATE 2004). Currently he is on the technical program committee for the DATE, IEEE/ACM Design Automation Conference (DAC), IEEE European Test Symposium (ETS), IEEE Defect and Fault Tolerance Symposium (DFT), IEEE Asian Test Symposium (ATS), IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS), IEEE Workshop on Silicon Debug and Diagnosis (SDD), and he

	serves as the Program Co-Chair for Diagnostic Services in Network-on-Chips Workshop. He was the guest co-editor for a special issue on Silicon Debug and Diagnosis (to be published by IET Proceedings on Computers and Digital Techniques) and a special issue on Low Power Test (to be published by for the Journal of Electronic Testing – Theory and Applications). He is a member of the ACM SIGDA and the IEEE Computer and Circuits and Systems Societies.
Co-Presenter 2	Xiaoqing WEN received a B.E. degree from Tsinghua University, Beijing China, in 1986, a M.E. degree from Hiroshima University, Hiroshima, Japan, in 1990, and a Ph.D degree from Osaka University, Osaka, Japan, in 1993. From 1993 to 1997, he was a Lecturer at Akita University, Akita, Japan. He was a Visiting Researcher at University of Wisconsin, Madison, U.S.A., from October 1995 to March 1996. He joined SynTest Technologies, Inc., U.S.A., in 1998, and served as its CTO until 2003. In January 2004, he joined the Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor. He was the Program Committee Co-Chair of the Sixteenth IEEE Asian Test Symposium and the Eighth IEEE Workshop on RTL and High Level Testing. Currently, he is on numerous program committees, including IEEE/ACM Design Automation Conference (DAC), IEEE International Test Conf. (ITC), Design, Automation, and Test in Europe (DATE), IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS), European Test Symposium (ETS), and Asian Test Symposium (ATS). He is the Associate Editor for Journal of Computer Science and Technology) and the Information Processing Society Transactions on System LSI Design Methodology. He co-authored and co-edited two books: VLSI Test Principles and Architectures: Design for Testability (San Francisco, CA: Morgan Kaufmann, 2006) and Power-Aware Testing and Test Strategies for Low Power Devices (New York, NY: Springer, 2009). His research interests include design, test, and diagnosis of integrated circuits. He currently holds 23 U.S. Patents and 5 Japan Patents in logic built-in self-test (BIST), test compression, and low-power test generation. He received the 2008 IEICE-ISS Best Paper Award. He is a member of the IEICE, the IPSJ, and the REAJ.