Tutorial intitulé ”Power-Aware Testing and Test Strategies for Low Power Devices”
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Power-Aware Testing and Test Strategies for Low Power Devices

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ITC 2012 – Anaheim, USA

Power-Aware Testing and Test Strategies for Low Power Devices

P. Girard; N. Nicolici; X. Wen (Eds.)
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Springer web site:
Motivation and Objectives

- Power constraints have severe impact on test
- Implications for test engineers / test tool developers:
  - Reduce power consumption in test mode becomes mandatory
  - Dedicated test strategies for low-power devices are needed

- Objectives of this tutorial:
  - Learning more about the impact of power during test
  - How to alleviate test power issues
  - How low-power devices and power management structures can be tested safely

Outline

1. Basics on Test
2. Relevance of power during test
3. Main test power issues
4. Reducing test power by dedicated techniques
5. Low power design and its implications on test
6. Reducing test power of low power circuits
7. Conclusion
Context

- Manufacturing test
- Digital circuits and systems
- Test stimuli are logic values (0,1)
- Test is an experiment!
  - If responses meet expectations, chip may be good … or stimuli are not sufficient (test escape)
  - If responses fail, chip may be faulty … or measurement may be erroneous (yield loss)
- Test costs can now amount to 40% of overall product cost

(courtesy: Bernardi et al., ETS, 2009)

Basics on Test - DfT

- Functional test is used … but structural test is dominant!
- Use of fault models … and DfT (Design-for-Test)
Basics on Test - DfT

![Diagram of a circuit under test with primary inputs, primary outputs, clock (CLK), scan in, scan enable (ScanENA), scan chain, stimuli, and responses.]

- **Primary Inputs**
- **Primary Outputs**
- **CLK**
- **Scan In**
- **Scan Enable (ScanENA)**
- **Scan Chain**
- **Capture**
- **Shift**
- **Shift & Launch**

Circuit Under Test

**Scan Chain**

**Responses**

**Stimuli**

**Shift & Launch**

**Capture**

**Time**

FF1 FF2 FF3 FF4

0 1 0 1

1 X X X X
0 1 X X
1 0 1 X
0 1 0 1

0 0 0 0

1 1 1 1
0 1 1 1
0 0 1 1
0 0 0 1
0 0 0 0

Basics on Test - DfT
Example (presented @ ITC 2008):

- 16 core CMT microprocessor from Sun Microsystems
- 410 millions of transistors, 250W @ 2.3GHz, 1.2V
- 1.35 millions of flip-flops, all are scannable !!

Power Consumption in CMOS

**Switching (dynamic) Power**

- Due to charge/discharge of load capacitance during switching
- \( P_{\text{DYN}} \propto V_{\text{DD}}^2 \cdot F_{\text{CLK}} \)

**Leakage (static) Power**

- Power consumed when the circuit is idle
- Mainly due to sub-threshold leakage
- \( I_{\text{SUB}} \propto \frac{V_{\text{DD}}}{V_{\text{TH}}} \)

*Short-circuit (dynamic) power due to direct current path from VDD to GND during output switching is considered as negligible*
Power During Test …

Much higher than during functional operations

PDN / Package / Cooling

Guard Bound

Actual Maximum Power

Functional Power

Test Power

Excessive Test Power During Structural Testing

determine

( presented by TI & Siemens AG @ ITC 2003 )

ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM

Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%

( Presented by Freescale @ ITC 2008 )

Power under test mode up to 3.8X power during functional mode

And many other industrial experiences reported in the literature …
Main reasons for excessive test power

- Conflict of objectives between test and functional mode
- No correlation between consecutive test vectors
- Non-functional clocking during test (e.g. LOC or LOS)
- DFT (e.g. scan) circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction

For conventional (non low-power) designs, dynamic power is the main responsible for excessive test power!!

Leakage power is a real issue during IDDQ test (reduced sensitivity) and during burn-in test (can result in thermal runaway condition and yield loss)

Power availability and quality may be limited

- During wafer sort test, all power pins may not be connected to the Tester Power Supply (TPS), resulting in reduced power availability

- Current limiters placed on TPS to prevent burn-out due to short-circuit current may affect power availability and quality

Wafer sort test targets gross defect (stuck-at fault) coverage

(Kundu et al. 2004)
Conventional (slow-speed) scan testing

Provoked by transitions generated in the CUT by the first shift operation

Provoked by transitions generated in the CUT by test launch (~ the last shifting operation)

At-speed scan testing with a LOC/LOS scheme

• Used to test for timing faults often caused by resistive defects
• Need of two-vector test patterns to provoke transitions
• Commonly used in microprocessor test
• Example: quad-core AMD Opteron processor (presented @ ITC 2008)
The problem of excessive power during scan testing can be split into two sub-problems: excessive power during the shift cycles and excessive power during the Launch-To-Capture (LTC) cycle.

- Excessive power during the shift cycles:
  - no value has to be captured/stored
  - one peak is not relevant
Power During Test …

**Excessive power during the shift cycles:**
- more than one peak → relates to **high average power**
- problems may occur

**Excessive power during the LTC cycle:**
- logic values have to be captured/stored
- one peak is highly relevant
Main Test Power Issues

**Elevated Average Power**

- Temperature Increase
  \[ T_{\text{die}} = T_{\text{air}} + \theta \times P_{\text{Average}} \]
- Excessive Heat Dissipation

- Structural degradations
- Hot-Carrier-Induced Defects
- Electro-migration
- Dielectric Breakdown
- Temperature variations
- Timing variations different from functional mode

- Chip Damage
- Reduced Reliability
- Yield Loss

---

**Main Test Power Issues**

- **Thermal hot-spot** results from localized overheating due to non-uniform spatial on-die power distribution
- Thermal hot-spot are likely to increase during package testing since test power dissipation can be high
- Main impact on the carrier’s mobility
  \[ \mu(T) = \mu(T_0) \left( \frac{T}{T_0} \right)^k \]
- Slow down the device in the thermal hot-spot affected region of the chip
- Increase gate delays → yield loss
- Structural degradation → permanent damage!
Main Test Power Issues

Elevated Average Power
(temperature increase, excessive heat dissipation)

Low Allowable Parallelism
(Wafer Testing & Package Testing)
Reduced Test Frequency
(Wafer Testing & Package Testing)

Low Test Throughput
(longer test time)

Main Test Power Issues

High Instantaneous Current

Elevated Peak Power

Power Supply Noise (IR-Drop, Ldi/dt)

Significant Delay Increase due to Excessive PSN
Erroneous Behavior Only During Testing (test fail)

Manufacturing Yield Loss
(Over-Kill)

As huge designs can be manufactured today, most power-related test issues (during scan) are due to excessive peak power
Main Test Power Issues

- **IR Drop** refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a resistance between the PDN source and the Vdd (Gnd) node of the gate

\[ U = R \cdot I \]

- **L(di/dt)** due to abrupt changes in current in short time (during switching) through inductive connections

\[ U = L \frac{di}{dt} \]
Main Test Power Issues

• Voltage drop: the main suspect for increased delay during capture
• Presented by Freescale @ ITC 2008

Main Test Power Issues

• Local IR-drop can be an issue even though total test power is reduced

activate all modules
activate only one module

peak: 1.2V @ 1.026V
(176mV(14.5%) drop)

peak: 1.2V @ 1.029V
(171mV(14.3%) drop)

(courtesy: K. Hatayama, STARC, Japan)
Reducing Test Power

**Straightforward Solutions**

- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing power distribution network (PDN)
  - Grid Sizing based on functional power requirements
  - all parts not active at a time
  - Grid Sizing for test purpose too expensive !!

*Costly or longer test time*

---

**Reducing Test Power**

**Main classes of dedicated solutions**

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

**Objective**

*Make test power dissipation comparable to functional power*

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …
Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Low-Power Test Pattern Generation

The Role of Test Data in Test Flow

Test Data

Test Patterns
Design Data
Expected Responses

Fabrication
LSI Chip
Comparison
Actual Responses

Passing Chips
Ship
Falling Chips
Discard

Tester

Probe Card
Prober
Socket Board
Handler
Low-Power Test Pattern Generation

The Importance of Test Patterns

- Judgment
  - Passing Chips
  - Failing Chips

  If defective chips pass ...
  High-Defect-Coverage Test → Low Quality

  Avoid

  If test pattern count is too large ...
  High Cost

  Reduce

  Test Compression

  If defect-free chips fail ...
  Low Yield ← Low-Power Test

Test Patterns

Low-Power Test Pattern Generation

Concept of Scan Test Generation

- Hard-to-Test
  Original Design

- Easy-to-Test
  Scan Design

- Logical Faults
  in Circuit Model

- Physical Defects
  in VLSI Chip

- Test Data
  Patterns & Responses

- Test Application
  by ATE
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (1)

Combinational Portion

Fault

Hard to detect

Pls (Primary Inputs)

PPIs (Pseudo Primary Inputs)

POs (Primary Outputs)

PPOs (Pseudo Primary Outputs)

CK

Target of Scan Test Pattern Generation - (2)

Combinational Portion

PIs

PPIs

SO (Scan Output)

SI (Scan Input)

Scan Chain

Scan FF

D

SI (Scan Input)

CK

SE (Scan Enable)
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (3)

Combinational Portion

Pls \rightarrow PPOs

PPIs

SO (Scan Output)

SI (Scan Input) Internal Test Stimulus

SE CK

SE = 1 (Shift Mode)

Target of Scan Test Pattern Generation - (4)

Combinational Portion

Pls \rightarrow PPOs

PPIs

PPOs Internal Test Response

SE CK

SE = 0 (Capture Mode)
**Low-Power Test Pattern Generation**

**Target of Scan Test Pattern Generation - (5)**

![Diagram showing test stimulus and capture with shift clock pulses](image)

- **Shift Clock Pulses**
  - Test Stimulus Load Started
  - Test Stimulus Load Completed

- **Capture**
  - Response Capture

- **Easy to get test stimuli in.**
- **Easy to get test responses out.**

**Target of Scan Test Pattern Generation - (6)**

![Diagram showing circuit-under-test and scan chain](image)

- **Test Pattern**
- **Combinational Portion**
- **CUT**
- **Scan FFs**
- **Scan Chain**

- **Scan Test Pattern Generation**: Assume a target fault in CUT, and find logic value assignments to some inputs (PI / PPI) so that the faulty (with the fault) and fault-free (without the fault) CUT create different responses on at least one output (PO / PPO).
Low-Power Test Pattern Generation

Stuck-At Fault and Its Test Generation - (1)

Fault-Free

Faulty Circuit

Stuck-at-0 Fault (Logic Value Fixed at 0)

Test Pattern

Fault Detected

Low-Power Test Pattern Generation

Stuck-At Fault and Its Test Generation - (2)

Shift

Test Pattern Load Started

Test Pattern Load Completed

Capture

Response Capture

Shift Clock Pulses

Average Shift Power

SE

CK

S_1  S_2  S_i

C
Low-Power Test Pattern Generation

Transition Delay Fault and Its Test Generation - (1)

Test Vector Pair

<table>
<thead>
<tr>
<th>V1</th>
<th>V2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Transition Delay Fault (Slow Value Change)

Test Cycle = Functional Cycle

At-Speed Testing

Low-Power Test Pattern Generation

Transition Delay Fault and Its Test Generation - (2)

Shift

Shift Clock Pulses

Capture

Func. Cycle

Average Shift Power

Peak Capture Power

Test Pattern Load Started

Test Pattern Load completed

Transition Launch

Response Capture
Automatic Test Pattern Generation (ATPG)

- ATPG is based on complex algorithms and is used to determine logic values for input bits in order to detect a fault in the given CUT.
- Not all input bits need to be assigned with logic values in order to detect a fault.
- The immediate result of ATPG is a test cube, which contains both specified bits (care bits) and unspecified bits (don’t care bits or X-bits).

Low-Power Test Pattern Generation

X-Bits in Test Cubes

- A large percentage of input bits in a test cube are don’t care bits (X-bits).
- Need X-filling (i.e., assigning logic values to X-bits) to create a complete test pattern.
Low-Power Test Pattern Generation

X-Filling in Test Pattern Generation

START

Initial Fault List Generation

Primary Fault Selection

Input Value Determination for Detecting Primary Fault

Dynamic Compaction

Partially-Specified Test Cube

X-Filling (e.g., Random-Fill)

Fully-Specified Test Vector

Fault Simulation to Update Fault List

Termination Condition Met?

N

Y

END

Low-Power Test Pattern Generation

Conventional X-Filling Technique: Random-Fill

- Conventionally, X-bits in a test cube are filled with random logic values.
- Advantages → Small test pattern count due to "fortuitous detection"
- Disadvantage → High test (shift and LTC) power

• Conventionally, X-bits in a test cube are filled with random logic values.
• Advantages → Small test pattern count due to "fortuitous detection"
• Disadvantage → High test (shift and LTC) power
## Various Low-Power X-Filling Techniques

<table>
<thead>
<tr>
<th>Low-Shift-Power X-Filling</th>
<th>Shift-In Power Reduction</th>
<th>Shift-Out Power Reduction</th>
<th>Total Shift Power Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MT-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>adjacent fill / repeat fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>output-justification-based X-filling</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MTR-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Low-LTC-Power X-Filling</th>
<th>FF-Oriented</th>
<th>Node-Oriented</th>
<th>Critical-Area-Oriented</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMF-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCP-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>preferred fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JP-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTX-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWT-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>state-sensitive X-filling</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCT-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAT-fill</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Low-Shift-and-LTC-Power X-Filling</th>
<th>impact-oriented X-filling</th>
<th>hybrid X-filling</th>
<th>bounded adjacent fill</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-fill</td>
<td>PHS-fill</td>
<td>CJP-fill</td>
<td></td>
</tr>
</tbody>
</table>


## Analysis of Test Power Impact

### Excessive Heat + Excessive Delay along Sensitized Paths

- **Heat Analysis**
- **IR-Drop Analysis**
- **Delay Analysis**
- **Sensitization Analysis**

Ideal but costly in terms of CPU time and data volume.

### Improvement

- Architecture-Level
- RTL
- Gate-Level

### Simplification

- Transition Count
  - Target: Cycle / Vector / Test Set
  - What: Total / Average / Peak
  - Where: FFs / Nodes (FFs + Gates) / Region
  - Level: Netlist / Layout + Power Supply Network
  - Sensitization: Not Considered / Considered

Trade-Off in Accuracy and Computational Costs
Typical Metric for Shift Power Analysis

Weighted Transition

\[ \text{Weighted}_\text{Transitions} = \sum (\text{Scan}\_\text{Chain}\_\text{Length} - \text{Transition}\_\text{Position}) \]

- Transitions closer to SI in a test vector cause more transitions in a scan chain.
- This metric has a good correlation with the total switching activity in a circuit.


Low-Power Test Pattern Generation

Example 1: Low-Shift-Power X-filling

- **Goal**: To assign proper logic values to don't care bits (X-bits) in a test cube so as to reduce transitions in scan chains (and thus also in the combinational logic).
- Popular techniques include 0-fill, 1-fill, MT-fill, and adjacent-fill.
- Mostly shift-in power is reduced. Occasionally, shift-out power and LTC power are also reduced, especially by 0-fill.
- Reported by TI at ITC 2003.
- No area overhead but may increase test pattern count.
Example 1 (cont’d): Low-Shift-Power X-filling

- **0-Fill**: Fill all X-strings with 0.
- **1-Fill**: Fill all X-strings with 1.
- **MT-Fill**: If the specified bits on both sides of an X-string have the same logic value, the X-string is filled with that logic value; otherwise, the X-string is filled with an arbitrary logic value.
- **Adjacent-Fill**: Fill an X-string with the specified-bit on the shift-out side.

MT-Fill

<table>
<thead>
<tr>
<th>0-Fill</th>
<th>1-Fill</th>
<th>MT-Fill</th>
<th>Adjacent-Fill</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 1 1 0 1 1 0 1 0 1 1 0 0 0 0 1 0 1 1 0 0 0 0 0 1 0 0 1 1 0 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>25</td>
<td>8</td>
<td>11</td>
</tr>
</tbody>
</table>

* Available from most commercial ATPG tools.

Low-Power Test Pattern Generation

Typical Metric for LTC Power Analysis - (1)
Weighted Switching Activity

**WSA**
(for a target area of elements (FFs, gates) 1, 2, ..., N)

\[ WSA = \sum (t_i \times w_i) \]

- \( t_i = 1 \) if the output of element \( i \) has a transition; otherwise, \( t_i = 0 \).
- \( w_i = (\text{the number of fanout lines from element } i) + \alpha \) (usually 1)

\[ \text{Weight} = 2 + 1 \]

Low-Power Test Pattern Generation

Typical Metric for LTC Power Analysis - (2)
Regional Weighted Switching Activity

Impact Area of Path $P$
On-Path Gate $G$
Aggressor Region of Gate $G$
Long Sensitized Path (LSP) $P$
($\geq 70\%$ Longest Structural Path)

Path $P$ is RISKY if the WSA in its impact area
$> 30\%$ of Maximum WSA in the impact area.

Example 2: Low-LTC-Power X-Filling

Combinational Circuit
Launch-to-Capture (LTC) Power

Stimulus
Response

PPI
1
FF1
0
FF2
1
FF3
0
PPO

IR-Drop
Delay Increase
Timing
Malfunction
(Test-Induced Yield Loss)

To minimize the Hamming distance between PPI and PPO
Low-Power Test Pattern Generation

Example 2 (cont’d): Low-LTC-Power X-Filling

JP-Fill

Test Cube

Test Response

0-Prob
1-Prob

(1.00, 0.00)  Assign
(0.00, 1.00)
(1.00, 0.00)
(0.00, 1.00)
(0.50, 0.50)
(0.50, 0.50)

f =

PI PO PPI PPO

0 1 0 1
0 1
0 0

Signal Probability Calculation
Logic Value Determination
Justify
Next Pass
No Decision

too close to call

(0.63, 0.57)

(0.17, 0.83)

0


Low-Power Test Pattern Generation

Example 2 (cont’d): Low-LTC-Power X-Filling

(Block in an Industry Chip: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)

LTC IR-Drop (V)

Test Vectors

0 50 100 150 200 250 300

Risky

Safe

Risky Safe

Original JP-Fill

Original JP-Fill

Chip-Level IR-Drop Distribution

Safe
Low-Power Test Pattern Generation

Example 3: Low-Shift-&-LTC-Power X-Filling

The basic idea is to first set several X-bits in a test cube to 0 and then conduct adjacent fill.

- The occurrence of 0 in the resulting fully-specified test vector is increased, which helps reduce shift-out and LTC power.
- Making use of the benefit of 0-fill.
- At the same time, applying adjacent fill helps reduce shift-in power.


Low-Power Test Pattern Generation

Extension to Test Compression Environments - (1)

Non-Test-Compression Environment

All X-bits are used for test power reduction. Easy to achieve significant reduction effect.
Low-Power Test Pattern Generation

Extension to Test Compression Environments - (2)

Test Compression Environment

- Compressed Test Pattern
- Decompressor
- Internal Test Cube
- Compactor

X-bits are also needed for test compression.
Remaining X-bits may be insufficient for test power reduction.

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (3)

- Shift Power Reduction
  - Use additional circuitry to force constant values to scan chains.
    - (0-Fill / 1-Fill: use one AND / OR gate for each scan chain)
    - (MT-Fill / Adjacent-Fill: use a shadow register for each scan chain)

Forced 0-Fill

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (4)

- **LTC Power Reduction**
  - *Combinational-Decompressor-Based Test Compression*
    - Disable clock gators in test generation.
    - Expand the combinational decompressor and apply low-LTC-power X-filling.
    - Conduct pinpoint LTC power reduction.
  - *Sequential-Decompressor-Based Test Compression*
    - Disable clock gators in test generation.
    - Apply low-LTC-power X-filling to independent or free X-bits.
    - Conduct pinpoint LTC power reduction.

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (5)

*Low-LTC-Power X-Filling based on Combinational Decompressor Expansion*

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (6)
Disabling Clock Gators in Test Generation

Fault Detection and Low LTC Power


Low-Power Test Pattern Generation

Extension to Test Compression Environments - (7)
X-Filling Using Independent / free X-Bits

- **X-classification** for separating implied X-bits from free X-bits.
- **CFBS identification** for identifying a set of free X-bits that can be filled with any logic values simultaneously without affecting compressibility.

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (8)

Pinpoint LTC Power Reduction

Do not reduce transitions around Dead Areas.
Hot Areas must be removed by reducing local switching and/or masking.
Cold Areas may be made "warm" by increasing local switching.


Low-Power Test Pattern Generation

Summary - (1)

- A large portion of input bits in test cubes are don't care bits (X-bits) even after aggressive test compaction in ATPG.
- X-bits can be used for reducing various shift and/or LTC power. Especially, 0-fill can reduce shift-in, shift-out, and LTC power to some extent.
- X-filling-based low-power test generation causes neither area overhead nor performance degradation.
- Most commercial ATPG tools now support low-power X-filling.
- Test pattern count may increase due to low-power X-filling. This problem can be solved by
  (1: Vector-Pinpoint) identifying high-test-power test patterns and conducting X-filing only for those patterns, or
  (2: Area-Pinpoint) identifying high-test-power areas and conducting X-filing only to reduce test power in those areas.
Low-Power Test Pattern Generation

Summary - (2)

---

**Current Low-Power Test Generation**

```
2012

Coarse-Grained

Unfocused (Global) Reduction
Over-Reduction Risk
Under-Reduction Risk
Test Quality Degradation Risk
Severe Test Data Increase
No Power Safety Guarantee
```

**Future Power-Safe Test Generation**

```
20??

Fine-Grained

Focused (Regional) Reduction
No Over-Reduction
Under-Reduction Countermeasure
Minimum Test Quality Impact
Minimum Test Data Increase
Power Safety Guarantee
```

(source: X. Wen, ETS, Invited Talk, 2012)

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Reducing Test Power

**Main classes of dedicated solutions**

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

**Objective**

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …
Design for Test Power Reduction

During scan testing (standard or at-speed):

<table>
<thead>
<tr>
<th>Shift Power Reduction</th>
<th>LTC Power Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Shift Impact Blocking</td>
<td>• Partial Capture</td>
</tr>
<tr>
<td>- blocking gate, special scan cell</td>
<td>- circuit modification</td>
</tr>
<tr>
<td>- first-level power supply gating</td>
<td>- scan chain disable</td>
</tr>
<tr>
<td>• Scan Chain Modification</td>
<td>- one-hot clocking</td>
</tr>
<tr>
<td>- scan cell reordering</td>
<td>- capture-clock staggering</td>
</tr>
<tr>
<td>- scan chain segmentation</td>
<td></td>
</tr>
<tr>
<td>- scan chain disable</td>
<td></td>
</tr>
<tr>
<td>• Scan Clock Manipulation</td>
<td></td>
</tr>
<tr>
<td>- splitting, staggering</td>
<td></td>
</tr>
<tr>
<td>- multi-duty clocking</td>
<td></td>
</tr>
</tbody>
</table>

An implementation of toggle suppression during shift using a latch at the output of the mux-D flip-flop with scan

Example 1 (cont’d): Low power scan cell

- Master-slave structure of a mux-D flip-flop is modified
- Gate the data output during shift
- Toggle suppression during shift
- But modification of all flip-flops \(\rightarrow\) impact on area and performance


Example 2: Scan cell reordering

- Scan cell order influences the number of transitions
- Need to change the order of bits in each vector during test application
- No overhead, FC and test time unchanged, low impact on design flow
- May lead to routing congestion problems ...

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)
Example 3: Inserting logic into scan chains

- The goal is to modify the transition count during shift.

Example 4: Scan segment inversion

- This is done by embedding a linear function in the scan path
- Reduces the transition count in the scan chain
Example 5: Scan chain segmentation

- Controllable and data-independent effect of shift power reduction
- No change to ATPG and no increase in test application time
- Presented (and used) by TI @ ITC 2000

Example 5 (cont’d): Scan chain segmentation

- The original scan chain is segmented into two scan chains
- Each scan chain is driven by a clock whose speed is half of the normal speed
- At each clock cycle, only half of the circuit inputs can switch
Example 6: Scan clock disabling

Design for Test Power Reduction

- Partial scan
- Disable clocks on non-scan flip-flops or latches

(example: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

Example 6 (cont’d): Scan clock disabling

Design for Test Power Reduction

- Partial scan
- Disable clocks on non-scan flip-flops or latches

Different scan chains can be activated based on multiple sensitizations of the same fault.

Example 7: Scan partitioning

Isolating multiple blocks of logic using boundary registers.

Example 8: Circuit partitioning
Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Power-Aware BIST and Compression

Example 1: Dual-speed LFSR for BIST

Dual-speed LFSR - concept

Power-Aware BIST and Compression

Example 1 (cont’d): Dual-speed LFSR for BIST


Example 2: Pattern suppression

![Pattern Suppression Diagram](source: S. Manich et al., JETTA, Vol. 16, Issue 3, 2000)
Useless patterns do not detect any faults
Deactivate scan clocks when no fault coverage improvement

Example 2 (cont’d): Pattern suppression

Useless patterns do not detect any faults
Deactivate scan clocks when no fault coverage improvement

Example 3: Pattern suppression in Scan BIST

• Decoder used for pattern suppression
  • Fault simulation
  • Logic minimization


(source: S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999)
Power-Aware BIST and Compression

Example 3 (cont’d): Pattern suppression in Scan BIST

<table>
<thead>
<tr>
<th>Index</th>
<th>Binary</th>
<th># Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>17</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>0</td>
</tr>
</tbody>
</table>

\{0000, 0001, 0010, 0100, 0101, 0110, 1000, 1011, 1100\} \quad \text{on-set}

\{0011, 0111, 1001, 1010\} \quad \text{offset}

\{1101, 1110, 1111\} \quad \text{do-set}

Implementing the pattern decoder

(source: S. Gerstendorfer and H.-J. Wunderlich, Proc. FIC, pp. 77-84, 1999)

---

Power-Aware BIST and Compression

Example 4: Application of Run-Length Coding

<table>
<thead>
<tr>
<th>Group</th>
<th>Run-Length</th>
<th>Group Prefix</th>
<th>Tail</th>
<th>Codeword</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_1</td>
<td>0</td>
<td>0</td>
<td>00</td>
<td>000</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>01</td>
<td>01</td>
<td>001</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>10</td>
<td>10</td>
<td>010</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>11</td>
<td>11</td>
<td>011</td>
</tr>
<tr>
<td>A_2</td>
<td>4</td>
<td>00</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>01</td>
<td>1001</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>10</td>
<td>1010</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>11</td>
<td>1011</td>
<td></td>
</tr>
<tr>
<td>A_3</td>
<td>8</td>
<td>00</td>
<td>1100</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>01</td>
<td>11001</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>10</td>
<td>11010</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>11</td>
<td>11011</td>
<td></td>
</tr>
</tbody>
</table>

Golomb code

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)
Example 5: Application of Huffman Coding

Power-Aware BIST and Compression

Example 5 (cont'd): Application of Huffman Coding

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)
Example 6: Application of selective encoding

Selective encoding - concept

Example 6 (cont'd): Application of selective encoding

<table>
<thead>
<tr>
<th>Slice</th>
<th>Slice code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XX00 010X</td>
<td>00 0101</td>
<td>Start a new slice, map X to 0, set bit 5 to 1</td>
</tr>
<tr>
<td>1110 0001</td>
<td>00 0111</td>
<td>Start a new slice, map X to 0, set bit 7 to 1</td>
</tr>
<tr>
<td></td>
<td>11 0000</td>
<td>Enter group-copy-mode, starting from bit 0 (i.e., group 0)</td>
</tr>
<tr>
<td></td>
<td>11 1110</td>
<td>The data is 1110</td>
</tr>
<tr>
<td>XXXX XX11</td>
<td>01 1000</td>
<td>Start a new slice, map X to 1, no bits are set to 0</td>
</tr>
</tbody>
</table>

Selective encoding - example
Example 7: Linear Finite State Machines

Conventional EDT does random filling

Identify clusters in the test cube that can have all the scan slices mapped onto the same value.

Push the decompressor in self-loop states during encoding for low-power fill.

Example 8: Centralized vs distributed BIST

- Circuit partitioning for low-power BIST
- Centralized BIST and controller
- Distributed approach where BIST sessions are power-conscious
Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

System-Level Power-Aware Scheduling

Improve Test Throughput by Exploiting Design Modularity

- The goal is to determine the blocks (memory, logic, analog, etc.) of an SOC to be tested in parallel at each stage of a test session in order to keep power dissipation under a specified limit while optimizing test time
- Some of the test resources (pattern generators and response analyzers) must be shared among the various blocks

(source: Y. Zorian, Proc. VTS, pp. 4-9, 1993)
System-Level Power-Aware Scheduling

Example 1: Resource Allocation and Incompatibility Graphs


Example 2: Power Model and Test Schedule
System-Level Power-Aware Scheduling

Example 3: Power Profile Manipulation

Power profile can be modified by pattern modification and/or test set reordering.

Example 4: Thermal Considerations

Temperature dependent test:
- $TS_1 = (T_0, T_2)$: 130°C
- $TS_2 = (T_1, T_3)$: 70°C
- $TS_3 = (T_0, T_3)$: 80°C
- $TS_4 = (T_1)$: 60°C
- $TS_5 = (T_2)$: 80°C

Temperature constraint at 90°C
Evaluating ...

... Test Power Reduction Strategies

- Power reduction effectiveness: High
- Fault coverage impact: Low
- ATPG engine impact: Minimum
- Test data volume impact: Low
- Test time impact: Low
- Functional timing impact: Low
- Area overhead: Low
- Usability with test compression: High
- Design effort: Minimum
- Design flow change: Low

(source: S. Ravi, TI, ITC07)

Test Power Estimation

- Needed for test space exploration (DfT/ATPG) early in the design cycle
- Availability of scan enhanced design and ATPG patterns only at the gate level in today’s design flows imposes the usage of gate-level estimators for test power
- Conventional flow adopted to perform estimation is simulation-based
- Estimation is performed at various PVT corners
- Challenges for multi-million gate SoCs
  - Time-consuming !!
  - Dump sizes can be very large !!
- The weighted transition metric (WSA) is quick but approximate

Faster and low cost solutions for test power estimation are needed!
Low Power Design (LPD)

Power Consumption Trends

- Exponential growth in transistor density
  - More functionality
- But linear reduction in supply voltage
  - Not adequate to prevent power density to increase

(source: Tirumurti et al., DATE, 2004)

The new power-performance paradigm:

- Low (fixed) power budget to limit power density
- But ever increasing integration and performance …

Adoption of low-power design and power management techniques

(courtesy: M. Hirech, Synopsys, USA)
Low Power Design (LPD)

System & Architecture
- Voltage / Frequency Scaling
- Architecture (parallel, well managed pipeline, etc.)
- Others (H/S partitioning, instruction set, algorithms, etc.)

IC Design & Implementation
- Clock Gating
- Multiple Supply Voltage
- Multiple Threshold Voltage
- Substrate-Bias
- Power Gating
- Others

Circuit (Logic) Design
- Low Power Cell Library
- Gate sizing (to equalize paths)
- Buffer insertion to reduce slew
- Logic restructuring to avoid hazards
- Memory Bit Cell and Compiler
- Others

Process Technology
- Reduce Vdd
- Threshold Voltage Option
- Low Capacitance Dielectric
- New Gate Oxide Material
- Transistor Sizing
- Others

Low Power Design (LPD)

<table>
<thead>
<tr>
<th>Main LPD techniques</th>
<th>Power reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dynamic</td>
</tr>
<tr>
<td>Clock gating</td>
<td>✔️</td>
</tr>
<tr>
<td>Power gating</td>
<td>✔️</td>
</tr>
<tr>
<td>Multi-Voltage domains</td>
<td>✔️</td>
</tr>
<tr>
<td>Multi-Threshold cells</td>
<td></td>
</tr>
</tbody>
</table>

These techniques are often combined together to achieve the maximum power optimization value
**Power Management Infrastructure**

<table>
<thead>
<tr>
<th>PM Structure</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gated Clocks</td>
<td>Gates clock going to a sequential block</td>
</tr>
<tr>
<td>Power Switches</td>
<td>(SLEEP=1) cuts off VDD from going to core</td>
</tr>
<tr>
<td>Isolation Cells</td>
<td>(Enable=1) sets output of domain to 0 when power is shut down</td>
</tr>
<tr>
<td>State Retention FF</td>
<td>(Save=1) ensures that data is saved when power domain is OFF.</td>
</tr>
<tr>
<td></td>
<td>(Restore=1) Restores the saved data when power domain wakes up</td>
</tr>
</tbody>
</table>

(courtesy: S. Ravi, TI)

**Power Specification Formats**

- Need of specifying properties of a circuit block w.r.t. power dissipation during design, verification and implementation
- Interpreted by designers and design automation tools
- To achieve a unified and efficient design flow, various EDA tools need to use a common format
  - Common Power Format (CPF) created by Cadence
  - Unified Power Format (UPF) supported Synopsys, Mentor and Magma and standardized by IEEE (P1801 std. working group)
- 90% same concepts, but different syntaxes
- Both formats are based on the Tool Control Language (TCL) embedded in most EDA tools
Power Specification Formats

- Used to describe the following specifications:
  - Voltage domains, Power domains, Isolation logic, Retention registers, Always-on cells, Power switches
  - The various power modes also need to be specified
  - Operating environment details (process, temperature, operating voltage data, and leakage calculation) are not part of UPF
  - UPF-based low power design flow →
- Example: creation of power domains

```cpp
create_power_domain pdTOP
create_power_domain pd1 -elements U1
create_power_domain pd2 -elements U2
create_power_domain pd3 -elements U3
```

Power During Test …

Even more critical for Low-Power Design !!

Guard Bound

Actual Maximum Power

Functional Power

Functional Power (Low-Power Device)

Test Power

Power-Management (hardware) (software)

Relatively Higher Excessive Test Power

PM structures often disabled during test application

(courtesy: X. Wen, KIT)
Requirements for Test of LPD

- Reduce (even more) test power by using the power management (PM) infrastructure (and/or applying the previous dedicated solutions)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures

And still target:
High fault coverage, short test application time, small test data volume, low area overhead, etc ... while making test power dissipation (dynamic and leakage) comparable to functional power

Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

Objective (again)
Make test power dissipation comparable to functional power
Reduction Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

Test for Multi-Voltage Designs

Multi-Voltage Design Styles

- Creation of “power islands”
- $V_{dd}$ scaling results in quadratic power reduction ($P = kCV^2f$)
- Level shifters to let signals cross power domain boundaries
Test for Multi-Voltage Designs

DVFS Design Style

- When high performance is not required, V and F can be scaled down
- Design flow is similar to MSV flow, but more complex control mechanism and more complicated timing analysis

Example 1: Multi-Voltage Aware Scan Cell Ordering

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93%)

<table>
<thead>
<tr>
<th>Ordering Position</th>
<th>Logical</th>
<th>Physical</th>
<th>Multi-Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A1</td>
<td>A2</td>
<td>A2</td>
</tr>
<tr>
<td>2</td>
<td>A2</td>
<td>A1</td>
<td>A1</td>
</tr>
<tr>
<td>3</td>
<td>A3</td>
<td>A3</td>
<td>A3</td>
</tr>
<tr>
<td>4</td>
<td>B1</td>
<td>B3</td>
<td>C1</td>
</tr>
<tr>
<td>5</td>
<td>B2</td>
<td>B1</td>
<td>C2</td>
</tr>
<tr>
<td>6</td>
<td>B3</td>
<td>B2</td>
<td>C3</td>
</tr>
<tr>
<td>7</td>
<td>C1</td>
<td>C1</td>
<td>B2</td>
</tr>
<tr>
<td>8</td>
<td>C2</td>
<td>C2</td>
<td>B3</td>
</tr>
<tr>
<td>9</td>
<td>C3</td>
<td>C3</td>
<td>B1</td>
</tr>
</tbody>
</table>

- Presented by Synopsys in JOLPE vol.1 n° 1 April 2005 and implemented in Synopsys Galaxy™ Test
Test for Multi-Voltage Designs

Example 2: Power-Aware Scan Chain Assembly

• Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints
• Bypass multiplexers allow testing of specific power domains in MSMV environment (switched-off power domains are bypassed)
• Preserve test functionality!

• Presented by Cadence @ ITC 2008
and implemented in Cadence Encounter™

Example 3: Voltage scaling in scan mode

• During scan shifting, the combinational logic needs not meet timing
• Goal: re-use the DVS infrastructure in test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
• At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
  • Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan FFs (V_t) = 0.35 V
  • If shift frequency (F_{shift}) = 125 MHz → V_{shift} = 0.635 V is enough!
• Presented by TI @ ITC 2007
Example 3 (cont’d): Voltage scaling in scan mode

Conventional Voltage Scaling Apparatus

PMScan: Shift Voltage Scaling Apparatus

LV_scan: Control signal from tester for low-voltage scan

Around 45% reduction of dynamic (average and peak) power and 90% reduction of leakage power, with negligible physical design impact and minimum area overhead.

Example 4: Power Domain Test Planning

Objective:
Create distinct test modes (test partitioning) for power domains

Multi-mode DFT architecture

Test application time

Test for Multi-Voltage Designs
Example 5: Test for MV Design – Bridge Defects

- **Bridge defects**
  - Most of them are resistive
  - Hard-shorts ~ stuck-at faults → detection is independent of Vdd

- **Resistive bridge defects**
  - A finite number of discrete intervals can be used to deal with all bridge $R_{sh}$ values

![Diagram of resistive bridge defects]

- Resistive bridge behavior at MV settings
  - Voltage $V_o$ does not scale linearly with the input threshold voltage of S1, S2 and S3 when changing Vdd
  - Resistance intervals differ from one voltage setting to another
  - Example: a bridge with $R_{sh} = R_{3B}$ will cause a logic fault at $V_{ddB}$ but not at $V_{ddA}$
  - A test pattern targeting a particular logic fault will detect different ranges of defects at different MV settings
Example 5: Test for MV Design – Bridge Defects

• **Goal of test generation for MV settings**
  - Generate test patterns for MV settings to maximize coverage of Resistive Bridging Faults (RBF) while minimizing test sequence length
  - Identification of Vdd specific test patterns for a given fault f
  - Example*: for a given circuit, 621 test patterns are needed at three Vdd settings with a commercial tool (207 at each Vdd), while only 391 test patterns applied at two Vdd settings (0.8V and 1.2V) are needed with the proposed technique (to achieve 100% fault coverage)

(source: U. Invelhon et al., ATS, 2007)

Example 6: Test for MV Design – Open Defects

• **Open defects**
  - Due to unconnected nodes
  - Full opens → logic failures tested using static faults

• **Transmission gate opens**

• **Interconnect resistive opens**
  - Resistive opens → time-dependent → tested using delay tests
  - Better detectability at elevated Vdd settings *

(* B. Kruseman et al., DATE, 2006)
Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

Test for Gated Clock Designs

Basic Clock Gating Design

- Not all FFs need to be triggered to perform a function (e.g., the camera control logic in a mobile-phone SoC can be inactive during a call).
- Gating-off the clock to functionally noncontributing FFs reduces dynamic power dissipation, not only in logic portions but also in clock trees (> 50%).
- One of the major techniques for reducing functional power.
- Widely adopted and supported by existing EDA tools.
Higher flexibility in power control due to the availability of both fine-level and coarse-level clock gating.

Test for Gated Clock Designs

Impact of Clock Gating on Test

- Clock gating prevents all scan FFs from being active at the same time.

- **Impact on Shift Mode**
  
  *Negative* → Scan shift realized through shift registers may become impossible if some FFs are inactive.

  \[\text{Shift Operation Guarantee Needed}\]

  \[\text{DFT for Clock Gating Logic} \checkmark\]

- **Impact on Capture Mode**
  
  *Positive* → Dynamic power can be reduced.

  \[\text{Good for LTC Power Reduction}\]

  \[-\text{Dynamic In-ATPG Techniques}\]
  \[-\text{Static In-ATPG Techniques} \checkmark\]
  \[-\text{Post-ATPG X-Filling Techniques} \checkmark\]
Example 1: DfT for Clock Gating Logic

- **Shift Mode** \((SE = 1)\): All scan FFs must be active to form one or more shift registers to shift-in test stimuli / shift-out test responses. Clock gating logic needs to be overridden (by \(SE\)) in shift mode.

- **Capture Mode** \((SE = 0)\): Scan FFs are allowed to be controlled by clock gating logic. Nothing needs to be done.

Automatically implemented by commercial DfT tools.

Example 1 (cont’d): DfT for Clock Gating Logic

- Disable clock gating in **shift mode** \((SE = 1)\): Unconditionally-ON Clock

  *Shift Register Operation*

- Enable clock gating in **capture mode** \((SE = 0)\): Conditionally-ON Clock

  *LTC Power Reduction*
Example 2: LTC Power Reduction by Clock Gating

- A default value is a value to be assigned to an input in order to gate-off a clock.
  - A preset value is to be used to fill an X-bit in a test cube.

- Flow for obtaining default values for clock gating:
  - Identify all clock gators.
  - For each clock gator, calculate a set of input settings that set the clock off.
  - The values in each input setting are default values.

- Flow for using default values for clock gating:
  - Generate a test cube for fault detection.
  - Assign default values to the X-bits in the test cube.
    (If there are multiple choices of default values, use the one that can turn-off more FFs.)

Test Cubes after ATPG

<table>
<thead>
<tr>
<th>Test Cases</th>
<th>G1</th>
<th>G2</th>
<th>G3</th>
<th>G4</th>
<th>G5</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>T2</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>T3</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
</tbody>
</table>

Test Cubes after Assigning Default Values

<table>
<thead>
<tr>
<th>Test Cases</th>
<th>G1</th>
<th>G2</th>
<th>G3</th>
<th>G4</th>
<th>G5</th>
<th>Merge &quot;default values&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td></td>
<td>X</td>
<td>Yes</td>
</tr>
<tr>
<td>T2</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td></td>
<td>0</td>
<td>Conflict</td>
</tr>
<tr>
<td>T3</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Example 2 (cont’d): LTC Power Reduction by Clock Gating

Static In-ATPG Technique 1

Test for Gated Clock Designs

Circuit Statistics
89K FFs
6 Scan Clocks
2200 Clock Gators

- The number of active clocks are reduced by more than 50%.
- LTC toggle activity is reduced by 35%.
- Fault coverage and test set size remain almost unchanged.


Example 3: LTC Power Reduction by Clock Gating

Static In-ATPG Technique 2

Before Test Generation
- Conduct structural analysis to identify all clock gators for each clock.
- Obtain clock control cubes (CCCs).
  ➔ A CCC is a combination of 0s, 1s, and Xs that disables one or more clock gators.
- Order CCCs by the decreasing number of FFs that a CCC turns off.

During Test Generation
- Generate a test cube for detecting one or more faults.
- Merge the test cube with all compatible CCCs in the determined order.

**Test for Gated Clock Designs**

**Example 4: LTC Power Reduction by Clock Gating**

*Post-ATPG X-Filling Technique*

Calculate logic values for X-bits so as to bring 0 to as many clock gator control lines as possible.


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**Summary**

- Functional clock gating is indispensable in reducing dynamic power.
- Functional clock gating logic needs to be modified in order to guarantee correct operation in *shift mode*.
- Clock gating can be used in *capture mode* to reduce LTC power.

- **Static In-ATPG Techniques**
  - (Assign pre-determined clock-gator disabling values to don’t-care bits (X-bits) in a test cube initially generated for fault detection.)

- **Post-ATPG X-Filling Techniques**
  - (Find and assign proper logic values to don’t-care (X-bits) in a test cube so as to disable as many clock gators as possible.)
Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

Test for Power Management Structures

Typical Power Management (PM) Structures

- Conditionally turning on or off power domains) to reduce dynamic and static power.
- Can be described in UPE (Unified Power Format) or CPF (Common Power Format).
- PM structures (①~⑤) require dedicated DfT methods and test patterns.
Example 1: Test for Power Switches

**Header Switch / Footer Switch / Symmetric Switch**

- Also called sleep transistors and used to shut down blocks (power domains) that are not in use (idle mode), hence reducing leakage power and dynamic power.
- Should be large enough to provide sufficient current to the circuit.

**Segmented Switch**

- Individual switch transistors can be small.
- Preferable in practice due to concerns about layout, design for manufacturability, and limiting inrush current when switching on a power domain.

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Example 1 (cont’d): Test for Power Switches

- **Pattern 1** *(Test for Short)*: \( TE = 1 / \text{standby}_t = 1 \)
  - Turn-off the power switch. After sufficient discharge, \( V_{core} \) should be much lower than \( V_{DD} \), and thus \( \text{Out (fault-free)} = 1 / \text{Out (faulty)} = 0 \)

- **Pattern 2** *(Test for Open)*: \( TE = 1 / \text{standby}_t = 0 \)
  - Turn-on the power switch. \( V_{core} \) should be close to \( V_{DD} \), and thus \( \text{Out (fault-free)} = 1 / \text{Out (faulty)} = 0 \)

*(source: Goal et al., Proc. ETS, pp. 145-150, 2006)*
Example 2: Parametric Test of Micro Switches

- Presented by ST-Ericson (Sophia) at International Test Conference 2008.
- Single-die 3G mobile phone base band Chip fabricated in 65nm technology.
- Includes multimedia features, such as video decoder, MP3 player, camera, games, and designed to be extremely low power.
- Rush current during power up $\rightarrow$ specific functional mode $\rightarrow$ test mode has to map functional mode!

Example 2 (cont’d): Parametric Test of Micro Switches

- The micro switches are daisy-chained. First, all the EPWR control signals are propagated in the chain. This gives a progressive ramp-up of the VddSwitched. Then, the ECLK control signal follows, turning ‘on’ all the transistors of the micro switches.
- Testing micro-switches individually is needed to detect resistive defects in each of them, and testing the micro switches’ control chain is important to ensure the chain is not broken.
Example 2 (cont’d): Parametric Test of Micro Switches

- DfT to add controllability and observability
- Test environment modeling needed to allow $R_{off}/R_{on}$ measurement
- Test time for 150 clusters (each composed of 16 switches): 36 ms

Example 3: Test for State Retention Registers (SRR’s)

- A SRR cell is for keeping its state when the power supply is turned off.
- Scan function can be designed into a SRR cell.
Example 3 (cont’d): Test for State Retention Registers (SRR’s)

Retention Capability Test
(1) Shift-in value \( V \) to SRR.
(2) Enable retention by setting Save to 1.
(3) Enable the isolation cell.
(4) Turn-off Power Domain 1.
(5) Turn-on Power Domain 1 after a few cycles.
(6) Disable the isolation cell.
(7) Disable retention by setting Restore to 1.
(8) Shift out the value of SRR and check if it is \( V \).

Repeat for \( V = 0 \) and \( V = 1 \)

Other tests, such as test for retention robustness to the state element’s clock, asynchronous set/reset, etc., may also need to be applied.

Example 4: Test for Isolation Cells - (1)

(1) Turn-off Power Domain 1 (\( SLEEP_1 = 1 \)).
(2) Turn-on Power Domain 2 (\( SLEEP_2 = 0 \)).
(3) Set 1 to \( ISO_1 \) and check if the isolation cell output (\( OUT \)) is 1.
Example 4: Test for Isolation Cells - (2)

Check for 1

OR

Power Domain ON

Power Domain OFF

Check for 0

AND

Power Domain ON

Power Domain OFF

Check for 0 and 1

FF

Power Domain ON

Power Domain OFF

Example 5: Test for Level Shifters

Test as a whole under all power supply voltage combinations of Power Domain 1 and Power Domain 2.
Example 6: Test for Power Mode Control Logic in SRAMs

- Study performed on Intel MC products in 2011
- Impact of resistive-open defects on the PMC logic
- Definition of appropriate fault models (FFM)
- Proposal of a new March test (LZ) solution

Test for Power Management Structures

Summary

- More and more power management structures are used in various IC designs in order to reduce power (dynamic and static) dissipation.
- Conventional ATPG does not target power management structures, leading to potential quality problems.
- There is a strong need to fully understand the basics of various power management structures and their operation modes.
- Special considerations and even new algorithms are needed to fully test various power management structures.

- Clock Gating Logic (Clock Gator, Control Logic)
- Power Gating Logic
  - PMU (Power Management Unit)
  - Power Switch
  - State Retention Register, Isolation Cell, Level Shifter
- Power Distribution Network
Impact of MTV Design on Test

• Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction \(\rightarrow\) speed cost to decrease leakage !!

• MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)

• Leakage power reduction while meeting timing and no area overhead

• Well established and supported by existing EDA tools

Impact of MTV Design on Test

• By using such power optimization techniques, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations

  ➢ PDF selection more complex
  ➢ More test data are needed
  ➢ Sensitivity to variations

• PSN has a significant impact on the timing behavior

  ➢ Need to integrate PSN effects in delay test pattern generation

Solutions for high quality at-speed fault coverage are needed !
Power-Aware DFT Tools

• Synopsys:
  • Galaxy™ Test is a comprehensive test automation solution.
  • DFT Compiler and its low power features (for more details on this tools, see “Power and Design for Test: A Design Automation Perspective”, A. De Colle et al, Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, April 2005)
  • DFT MAX and its low power features (for more details on this tools, see “DFT MAX and Power”, R. Kapur et al, Journal of Low Power Electronics (JOLPE), Vol. 3, N° 2, August 2007)
  • TetraMAX® - power-aware test patterns for defect detection
  • Details
    http://www.synopsys.com/Tools/Implementation/RTLSynthesis/Test/Pages/default.aspx

Power-Aware DFT Tools

• Mentor:
  • Tessent™ FastScan™ and Tessent™ TestKompress™ provide comprehensive low-power and power-aware test solutions.
  • Details at http://www.mentor.com/products/silicon-yield/logic_test/

• Cadence:
  • Encounter® Test, a key technology in the Cadence® Encounter digital IC design platform
  • To support manufacturing test of low-power devices, Encounter Test uses power intent information to create distinct test modes automatically for power domains and shut-off requirements.
  • Details
Conclusion

• Power consumption during Test is a real issue!!
• Not only during manufacturing test but also during on-line test
• Not only ATPG and DFT but also BIST, test compression, and test scheduling have been addressed
• No generic solution, but rather a combination of solutions. Example: power-aware DfT for reducing shift power and power-aware ATPG for reducing LTC power
• New test solutions for Low-Power Design that preserve test functionality are needed!!

Thank You!