Tutorial intitulé "Power-Aware Testing and Test Strategies for Low Power Devices"

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Power-Aware Testing and Test Strategies for Low Power Devices

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Power-Aware Testing and Test Strategies for Low Power Devices

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Motivation and Objectives

- Power constraints have severe impact on test
- Implications for test engineers / test tool developers:
  - Reduce power consumption in test mode becomes mandatory
  - Dedicated test strategies for low-power devices are needed
- **Objectives of this tutorial:**
  - Learning more about the impact of power during test
  - How to alleviate test power issues
  - How low-power devices and power management structures can be tested safely

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Outline

1. Basics on Test
2. Relevance of power during test
3. Main test power issues
4. Reducing test power by dedicated techniques
5. Low power design and its implications on test
6. Reducing test power of low power circuits
7. Conclusion

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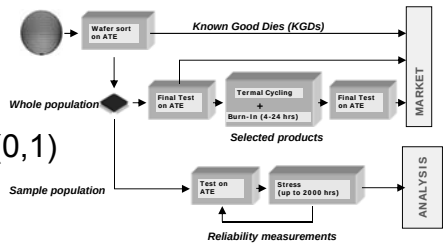
Context

- Manufacturing test
- Digital circuits and systems
- Test stimuli are logic values (0,1)
- Test is an experiment !



✓If responses meet expectations, chip may be good … or stimuli are not sufficient (test escape)

✓If responses fail, chip may be faulty … or measurement may be erroneous (yield loss)

- Test costs can now amount to 40% of overall product cost

(courtesy: Bernardi et al., ETS, 2009)

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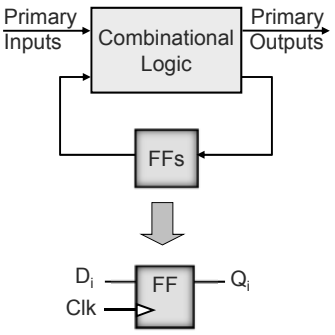
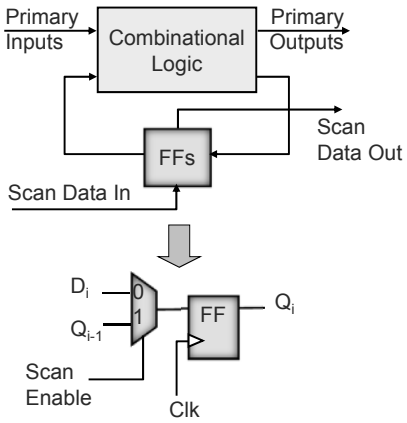
Basics on Test - DfT

- Functional test is used … but structural test is dominant !
- Use of fault models … and DfT (Design-for-Test)





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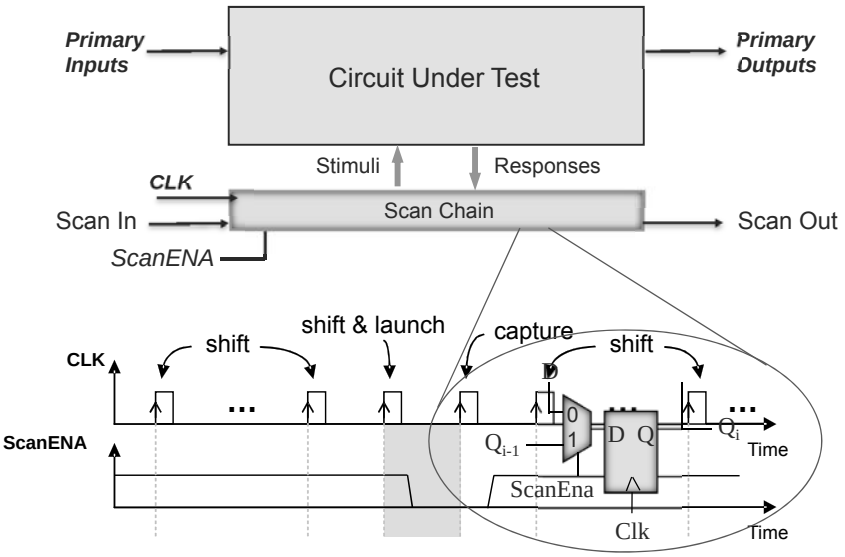
Basics on Test - DfT



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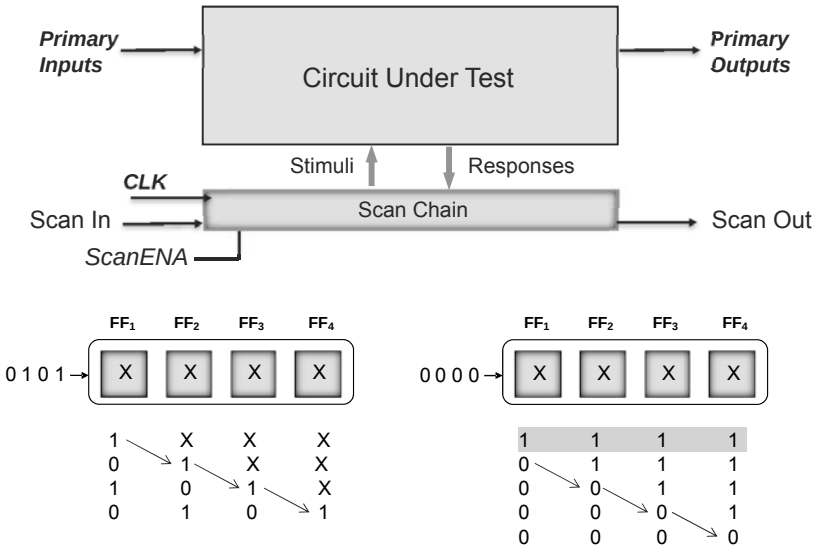
Basics on Test - DfT



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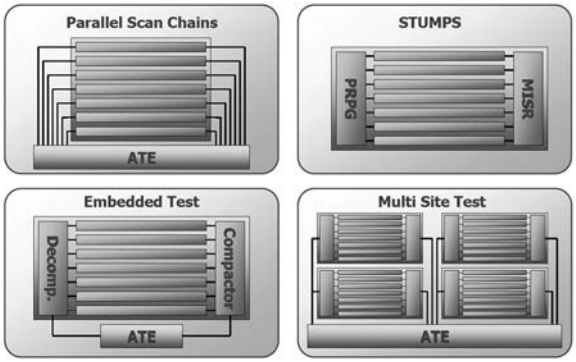
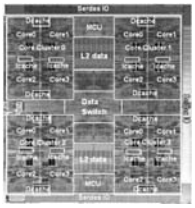
Basics on Test - DfT





Example (presented @ ITC 2008):

- 16 core CMT microprocessor from Sun Microsystems
- 410 millions of transistors, 250W @ 2.3GHz, 1.2V
- **1.35 millions of flip-flops, all are scannable !!**

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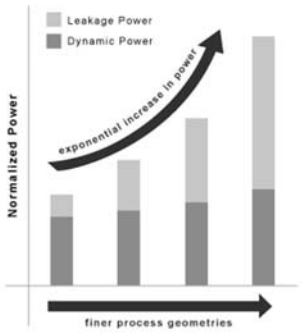
Power Consumption in CMOS

Switching (dynamic) Power

- Due to charge/discharge of load capacitance during switching
- $P_{DYN} \propto V_{DD}^2 . F_{CLK}$

Leakage (static) Power

- Power consumed when the circuit is idle
- Mainly due to sub-threshold leakage
- $I_{SUB} \propto V_{DD} / V_{TH}$



Short-circuit (dynamic) power due to direct current path from VDD to GND during output switching is considered as negligible

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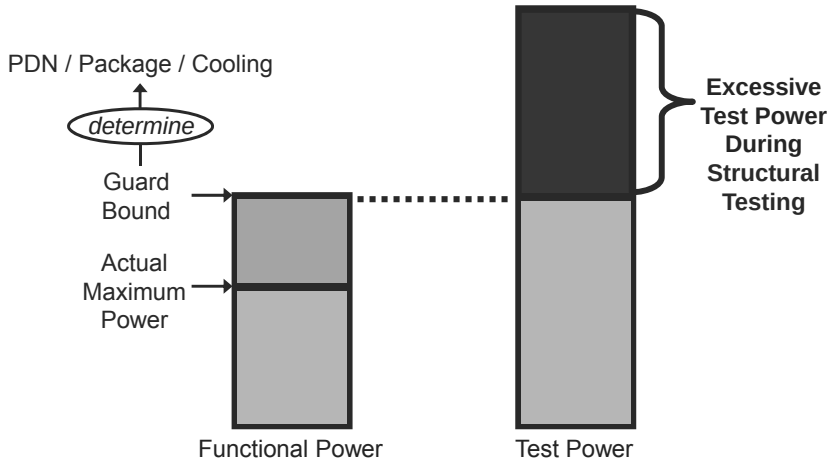
Power During Test …

Much higher than during functional operations



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Power During Test …

Much higher than during functional operations

(presented by TI & Siemens AG @ ITC 2003)
ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM

Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%

(Presented by Freescale @ ITC 2008)
Power under test mode up to 3.8X power during functional mode

And many other industrial experiences reported in the literature …

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Power During Test …

Main reasons for excessive test power

- Conflict of objectives between test and functional mode
- No correlation between consecutive test vectors
- Non-functional clocking during test (e.g. LOC or LOS)
- DFT (e.g. scan) circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction

For conventional (non low-power) designs, dynamic power is the main responsible for excessive test power !!

Leakage power is a real issue during IDDQ test (reduced sensitivity) and during burn-in test (can result in thermal runaway condition and yield loss)

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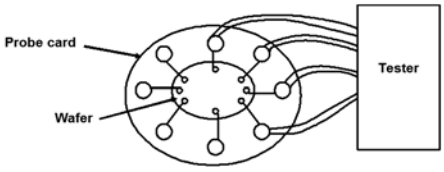
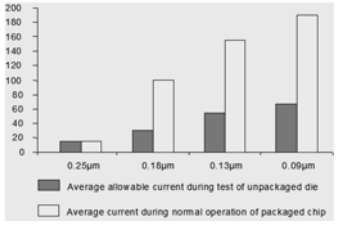
Power During Test …

Power availability and quality may be limited

- During wafer sort test, all power pins may not be connected to the Tester Power Supply (TPS), resulting in reduced power availability





(Kundu et al. 2004)

- Current limiters placed on TPS to prevent burn-out due to short-circuit current may affect power availability and quality

Wafer sort test targets gross defect (stuck-at fault) coverage

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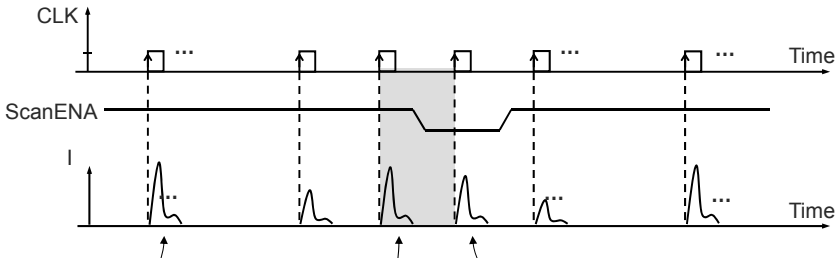
Power During Test …

Conventional (slow-speed) scan testing



Provoked by transitions generated in the CUT by the first shift operation

Provoked by transitions generated in the CUT by response capture

Provoked by transitions generated in the CUT by test launch (~ the last shifting operation)

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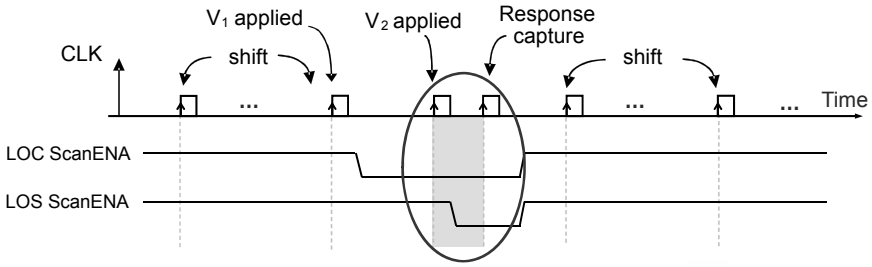
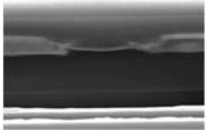
Power During Test …

At-speed scan testing with a LOC/LOS scheme





- Used to test for timing faults often caused by resistive defects
- Need of two-vector test patterns to provoke transitions
- Commonly used in microprocessor test
- **Example**: quad-core AMD Opteron processor (presented @ ITC 2008)

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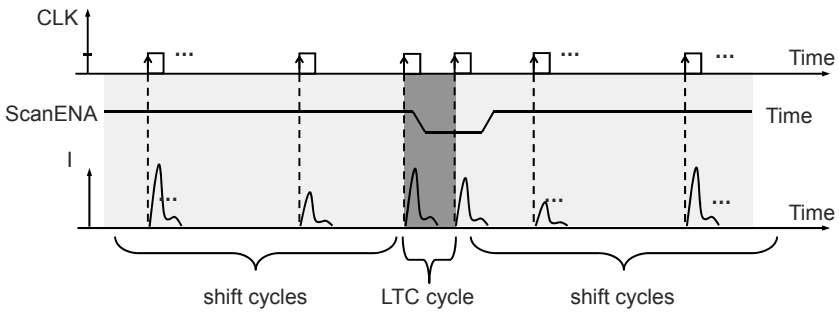
Power During Test …



- The problem of excessive power during scan testing can be split into two sub-problems: excessive power during the shift cycles and excessive power during the Launch-To-Capture (LTC) cycle

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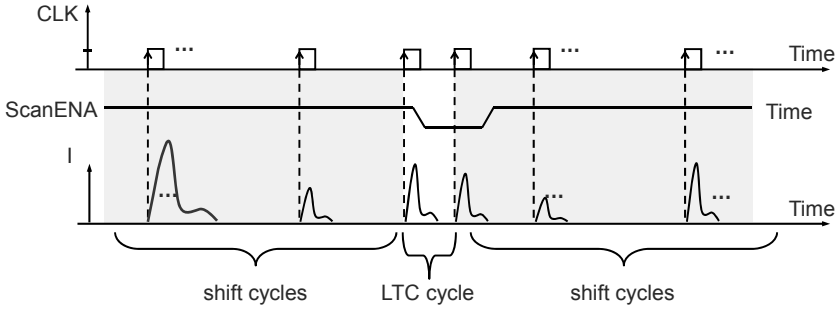
Power During Test …



- Excessive power during the shift cycles:
  - no value has to be captured/stored
  - **one peak is not relevant**

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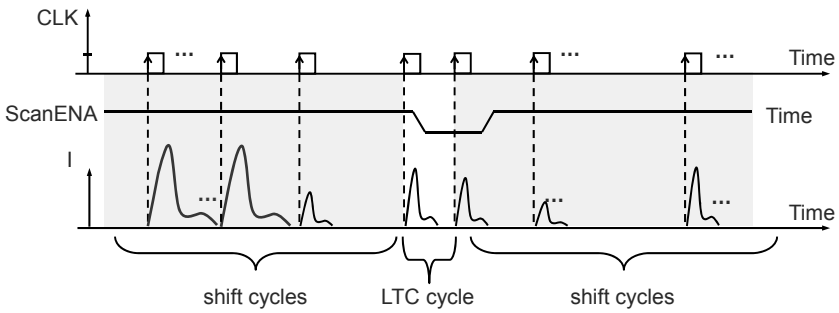
Power During Test …



- Excessive power during the shift cycles:
  - more than one peak → relates to **high average power**
  - **problems may occur**

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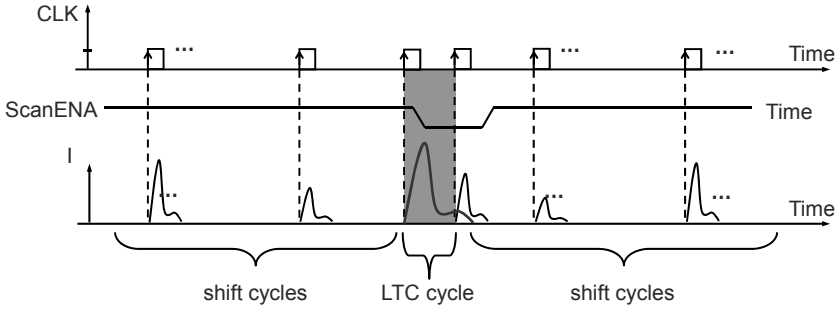
Power During Test …



- Excessive power during the LTC cycle:
  - logic values have to be captured/stored
  - **one peak is highly relevant**

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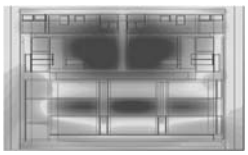
Main Test Power Issues



Elevated Average Power

Temperature Increase

$T_{die} = T_{air} + \theta \times P_{Average}$

Excessive Heat Dissipation

Structural degradations	Hot-Carrier-Induced Defects Electro-migration Dielectric Breakdown	Temperature variations Timing variations different from functional mode
Chip Damage	**Reduced Reliability**	**Yield Loss**

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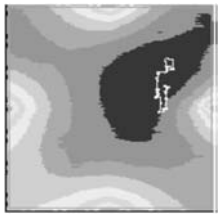
Main Test Power Issues

- **Thermal hot-spot** results from localized overheating due to non-uniform spatial on-die power distribution
- Thermal hot-spot are likely to increase during package testing since test power dissipation can be high
- Main impact on the carrier's mobility $\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-k_1}$
- Slow down the device in the thermal hot-spot affected region of the chip
- Increase gate delays → yield loss
- Structural degradation → permanent damage !



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Main Test Power Issues

Elevated Average Power
(temperature increase, excessive heat dissipation)

Low Allowable Parallelism
(Wafer Testing & Package Testing)

Reduced Test Frequency
(Wafer Testing & Package Testing)

Low Test Throughput
(longer test time)

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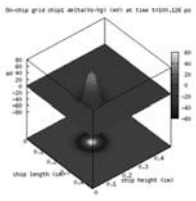
Main Test Power Issues



High Instantaneous Current

Elevated Peak Power

Power Supply Noise (IR-Drop, Ldi/dt)

Significant Delay Increase due to Excessive PSN

Erroneous Behavior Only During Testing (test fail)

Manufacturing Yield Loss
(Over-Kill)

As huge designs can be manufactured today, most power-related test issues (during scan) are due to excessive peak power

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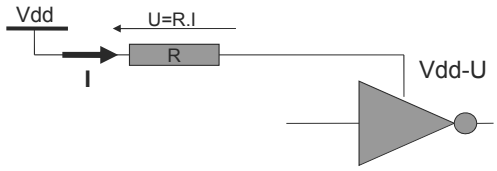
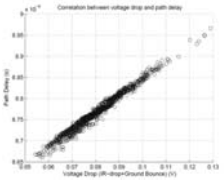
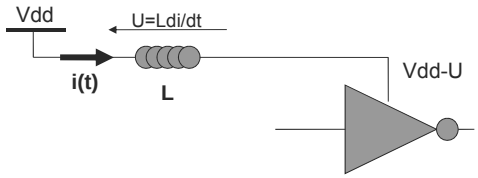
Main Test Power Issues

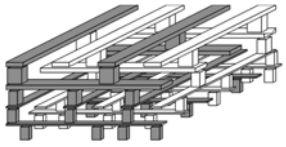
- **IR Drop** refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a resistance between the PDN source and the Vdd (Gnd) node of the gate





- **L(di/dt)** due to abrupt changes in current in short time (during switching) through inductive connections





(courtesy: O. Sentieys, IRISA, France)

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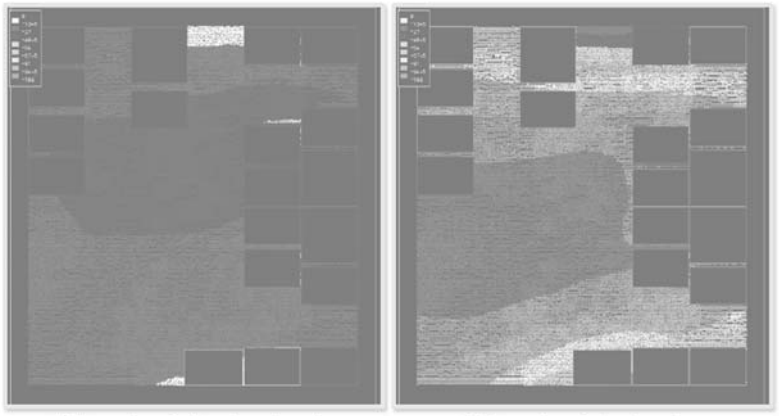
Main Test Power Issues



Voltage drop in functional mode | Voltage drop in test mode

(courtesy: A. Domic, Synopsys, USA)

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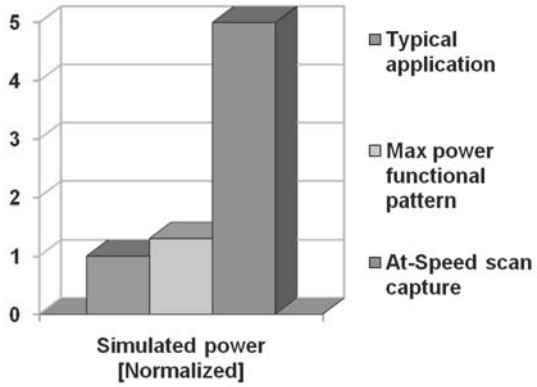
Main Test Power Issues



- Voltage drop: the main suspect for increased delay during capture
- Presented by Freescale @ ITC 2008

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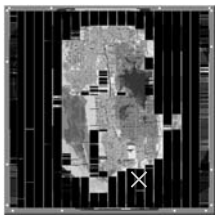
Main Test Power Issues

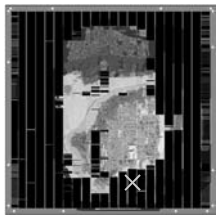
- Local IR-drop can be an issue even though total test power is reduced

activate all modules



peak: 1.2V ® 1.026V
(176mV(14.5%) drop)

activate only one module



peak: 1.2V ® 1.029V
(171mV(14.3%) drop)

(courtesy: K. Hatayama, STARC, Japan)

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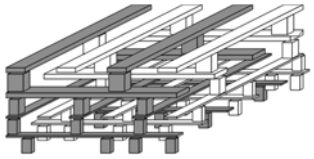
Reducing Test Power

Straightforward Solutions

- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing power distribution network (PDN)
  - Grid Sizing based on functional power requirements - all parts not active at a time
  - Grid Sizing for test purpose too expensive !!



Costly or longer test time

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Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

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Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

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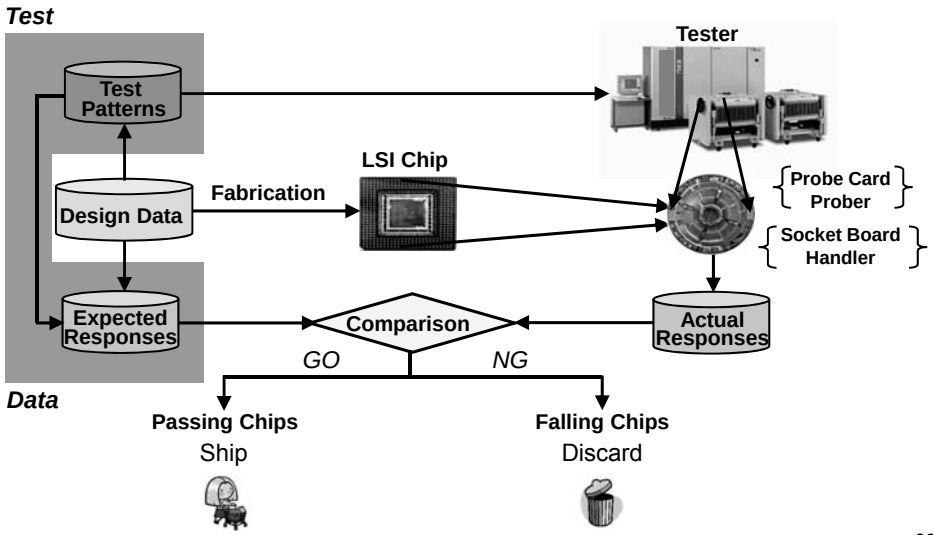
Low-Power Test Pattern Generation

The Role of Test Data in Test Flow



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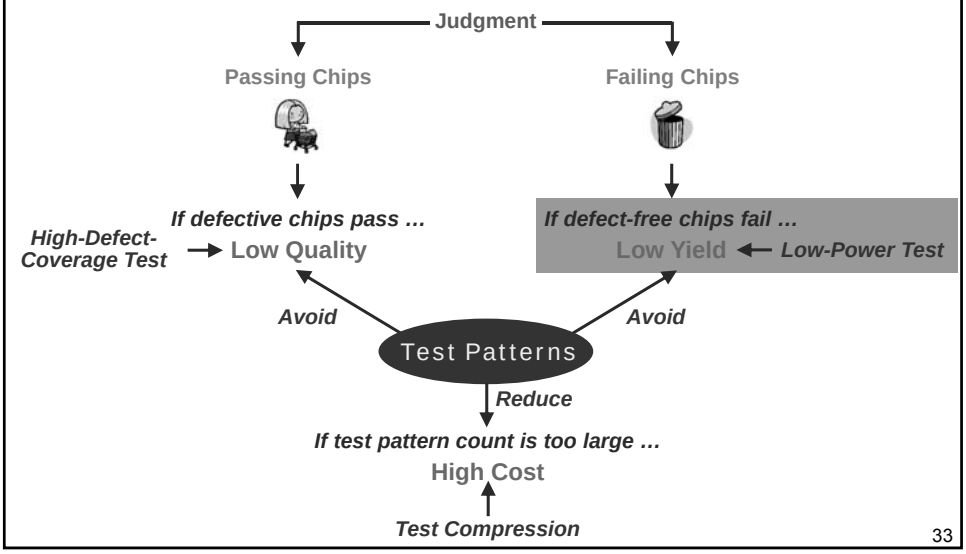
Low-Power Test Pattern Generation

The Importance of Test Patterns



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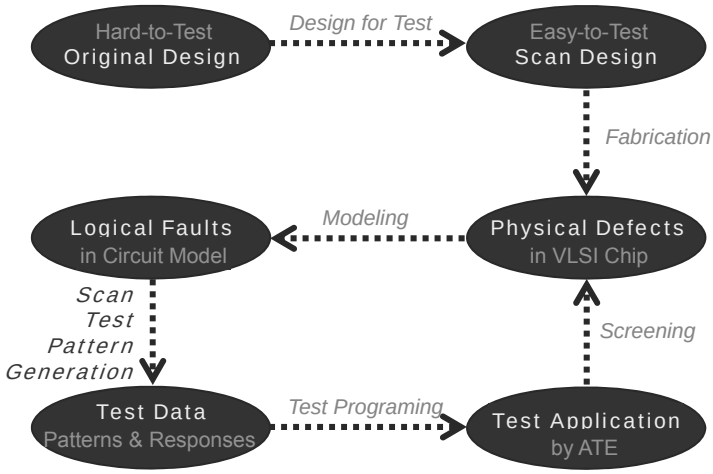
Low-Power Test Pattern Generation

Concept of Scan Test Generation



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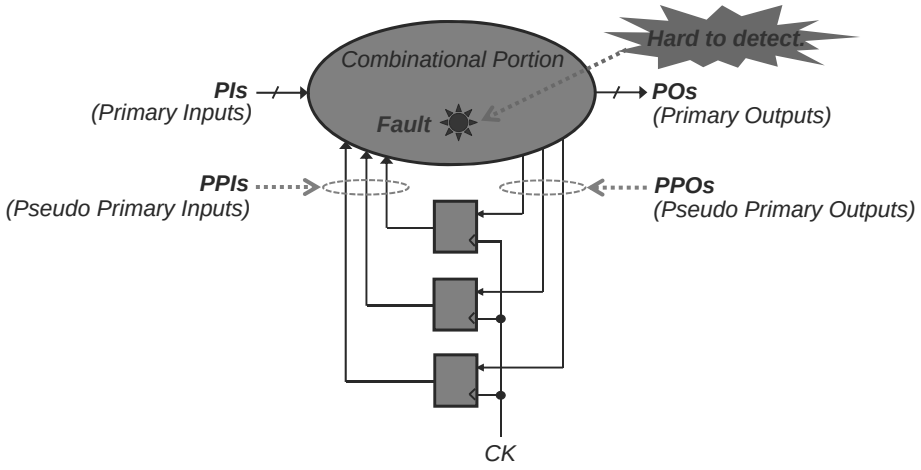
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (1)



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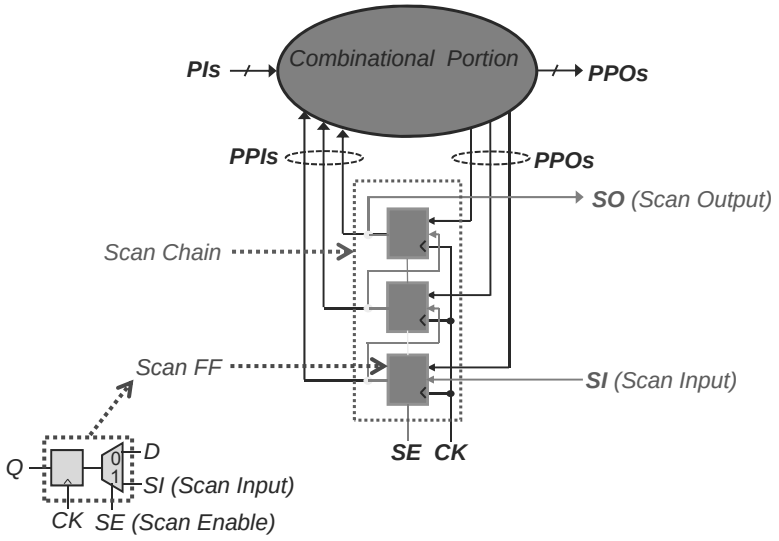
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (2)



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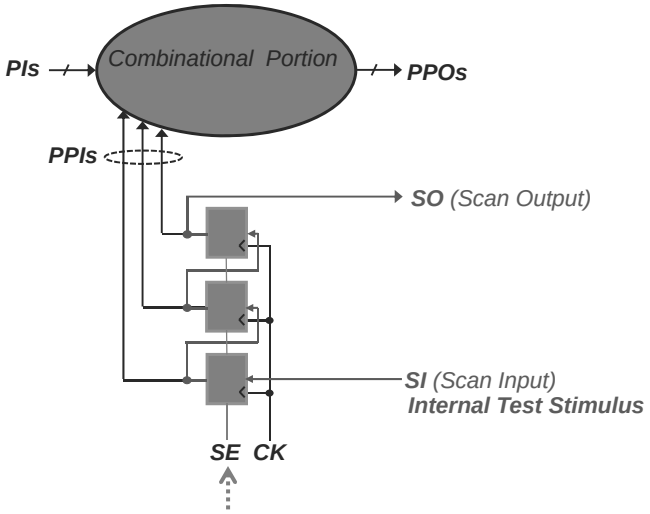
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (3)



SE = 1 (*Shift Mode*)

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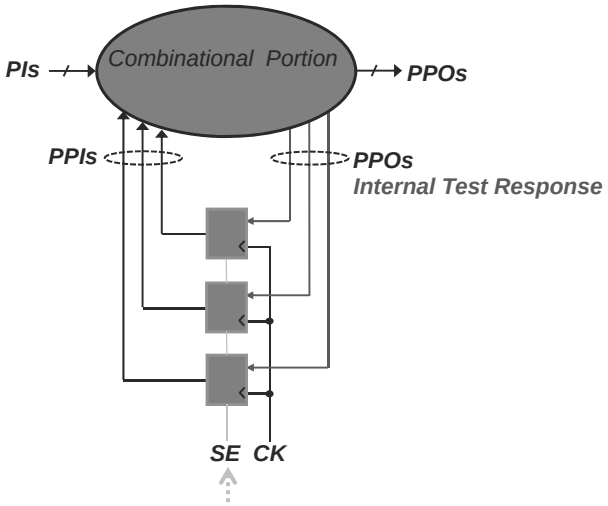
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (4)



SE = 0 (*Capture Mode*)

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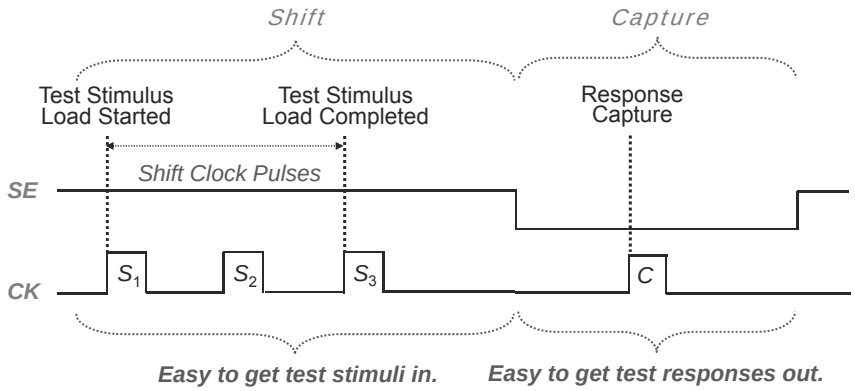
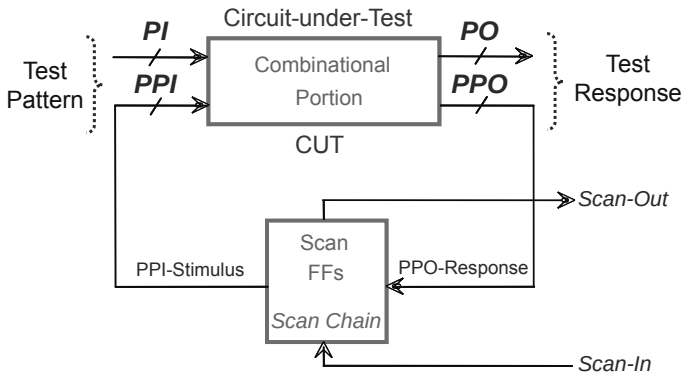
Low-Power Test Pattern Generation

Target of Scan Test Pattern Generation - (5)



Low-Power Test Pattern Generation

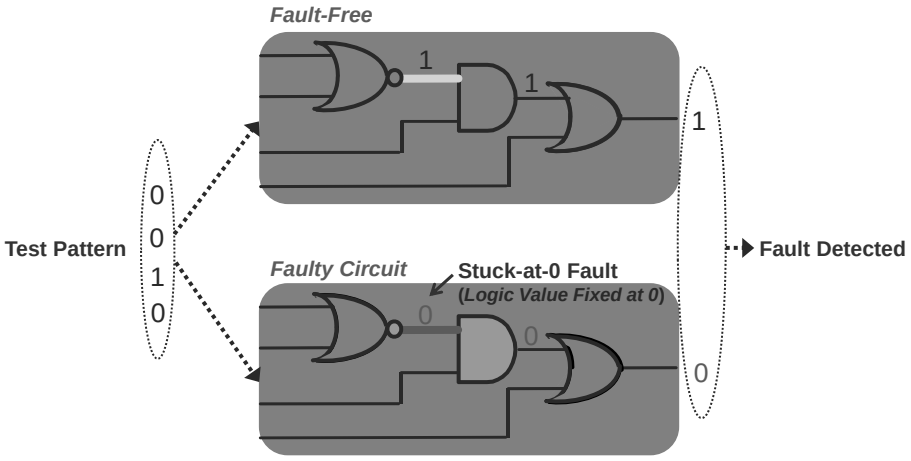
Target of Scan Test Pattern Generation - (6)



- Scan Test Pattern Generation: Assume a target fault in CUT, and find logic value assignments to some inputs (PI / PPI) so that the faulty (with the fault) and fault-free (without the fault) CUT create different responses on at least one output (PO / PPO).

Low-Power Test Pattern Generation

Stuck-At Fault and Its Test Generation - (1)



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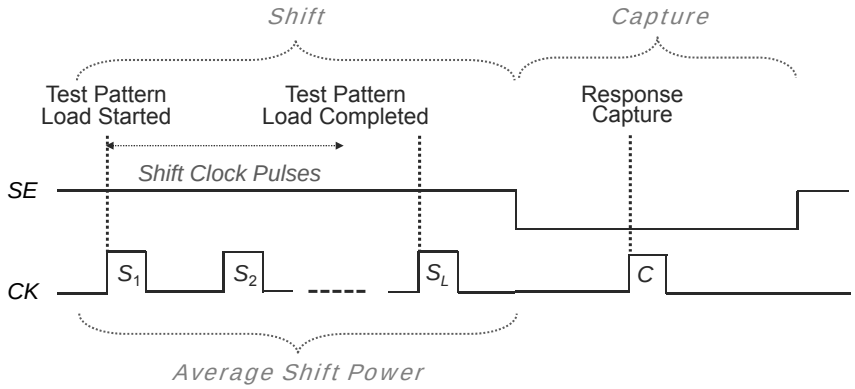
Low-Power Test Pattern Generation

Stuck-At Fault and Its Test Generation - (2)



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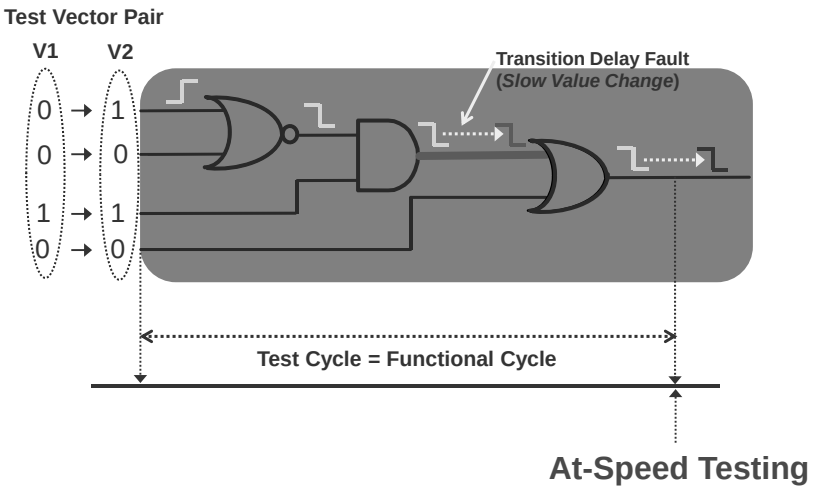
Low-Power Test Pattern Generation

Transition Delay Fault and Its Test Generation - (1)



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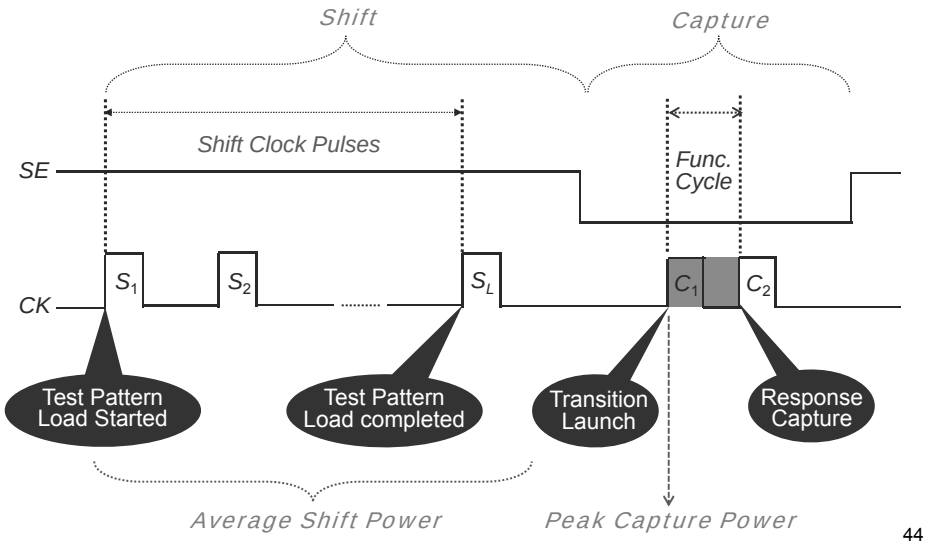
Low-Power Test Pattern Generation

Transition Delay Fault and Its Test Generation - (2)



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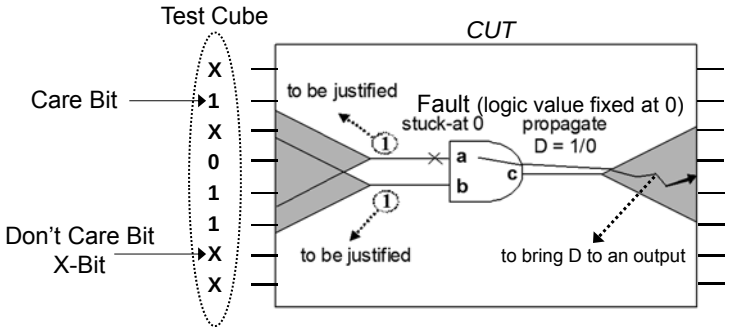
Low-Power Test Pattern Generation

Automatic Test Pattern Generation (ATPG)



- ATPG is based on complex algorithms and is used to determine logic values for input bits in order to detect a fault in the given CUT.
- Not all input bits need to be assigned with logic values in order to detect a fault.
- The immediate result of ATPG is a test cube, which contains both specified bits (care bits) and unspecified bits (don't care bits or X-bits).

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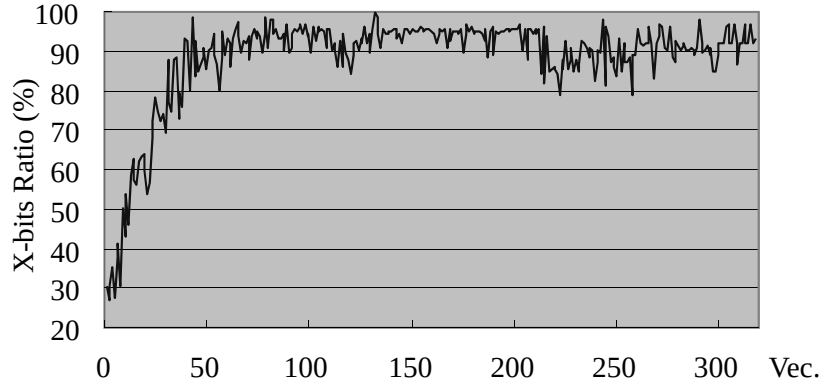
Low-Power Test Pattern Generation

X-Bits in Test Cubes

(Block in an Industry Chip: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)



- A large percentage of input bits in a test cube are don't care bits (X-bits).
- Need X-filling (*i.e., assigning logic values to X-bits*) to create a complete test pattern.

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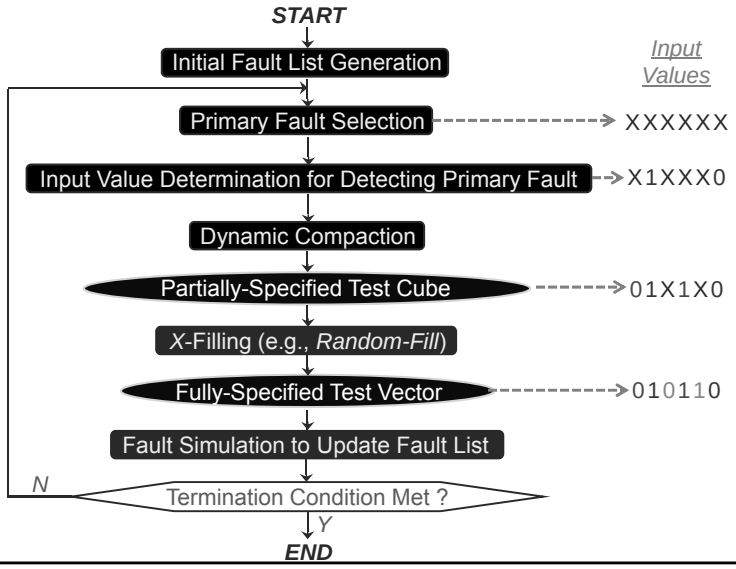
Low-Power Test Pattern Generation

X-Filling in Test Pattern Generation



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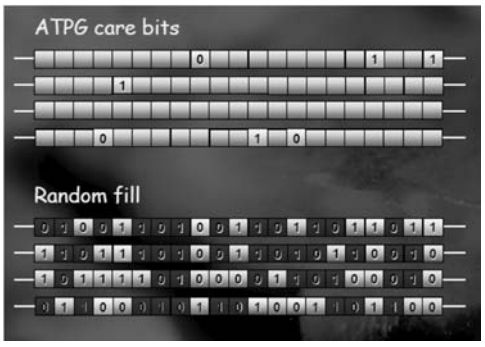
Low-Power Test Pattern Generation

Conventional X-Filling Technique: *Random-Fill*



- Conventionally, X-bits in a test cube are filled with random logic values.
- Advantages → *Small test pattern count due to "fortuitous detection"*
- Disadvantage → *High test (shift and LTC) power*

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Low-Power Test Pattern Generation

Various Low-Power X-Filling Techniques

Low-Shift-Power X-Filling ✓		
Shift-In Power Reduction	Shift-Out Power Reduction	Total Shift Power Reduction
0-fill *1-fill* *MT-fill* *adjacent fill / repeat fill*	*output-justification-based X-filling*	*MTR-fill*
Low-LTC-Power X-Filling ✓		
FF-Oriented	Node-Oriented	Critical-Area-Oriented
PMF-fill *LCP-fill* *preferred fill* *JP-fill* *CTX-fill*	*PWT-fill* *state-sensitive X-filling*	*CCT-fill* *CAT-fill*
Low-Shift-and-LTC-Power X-Filling ✓		
impact-oriented X-filling	*hybrid X-filling*	*bounded adjacent fill*
Low-Power *X*-Filling for Compressed Scan Testing		
0-fill	*PHS-fill*	*CJP-fill*

(*source: X. Wen and S. Wang, Low-Power Test Generation, Chapter 3 in Power-Aware Testing and Test Strategies for Low Power Devices, edited by P. Girard, N. Nicolici & X. Wen, Springer, 2009*)

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Low-Power Test Pattern Generation

Analysis of Test Power Impact

Excessive Heat + Excessive Delay along Sensitized Paths

Heat Analysis

IR-Drop Analysis **Delay Analysis**

Sensitization Analysis

Ideal but costly in terms of CPU time and data volume.

Improvement

- Architecture-Level
- RTL
- Gate-Level
- Vectorless
- Vector-Based

Simplification

Transition Count

- @ *Target: Cycle / Vector / Test Set*
- @ *What: Total / Average / Peak*
- @ *Where: FFs / Nodes (FFs + Gates) / Region*
- @ *Level: Netlist / Layout + Power Supply Network*
- @ *Sensitization: Not Considered / Considered*

Trade-Off in Accuracy and Computational Costs

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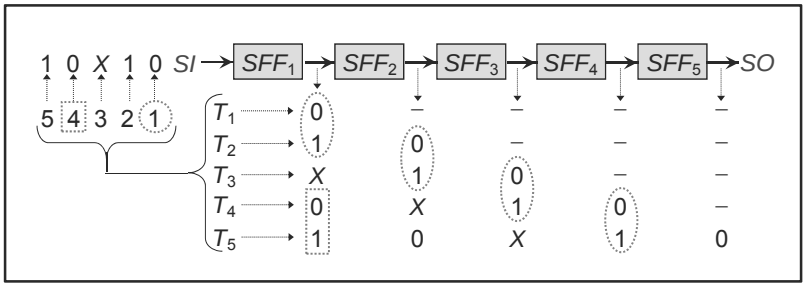
Low-Power Test Pattern Generation

Typical Metric for Shift Power Analysis

Weighted Transition



Weighted_Transitions = Σ (*Scan_Chain_Length* − *Transition_Position*)

- Transitions closer to *SI* in a test vector cause more transitions in a scan chain.
- This metric has a good correlation with the total switching activity in a circuit.

(source: R. Sankaralingam et al., Proc. VTS, pp. 35-40, 2000)

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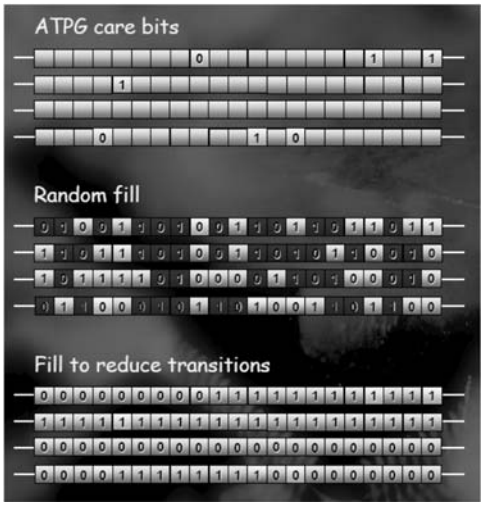
Low-Power Test Pattern Generation

Example 1: Low-Shift-Power X-filling

- **Goal**: To assign proper logic values to don't care bits (X-bits) in a test cube so as to reduce transitions in scan chains (and thus also in the combinational logic).
- Popular techniques include ***0-fill***, ***1-fill***, ***MT-fill***, and ***adjacent-fill***.
- Mostly shift-in power is reduced. Occasionally, shift-out power and LTC power are also reduced, especially by ***0-fill***.
- Reported by TI at ITC 2003.
- No area overhead but may increase test pattern count.



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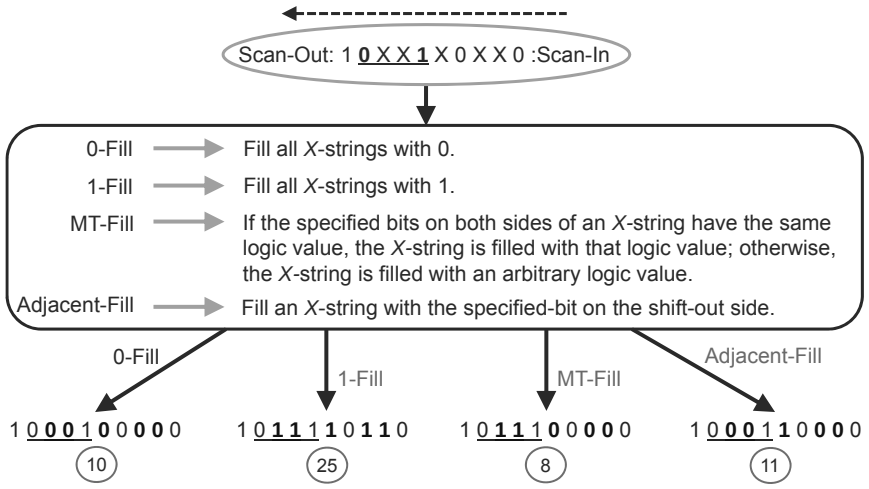
Low-Power Test Pattern Generation

Example 1 (cont'd): Low-Shift-Power X-filling



- Available from most commercial ATPG tools.

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Low-Power Test Pattern Generation

Typical Metric for LTC Power Analysis - (1)

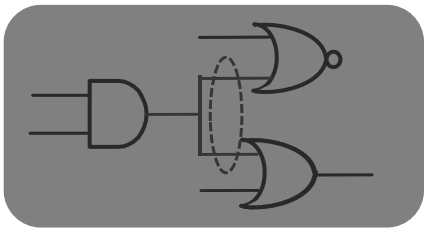
Weighted Switching Activity

WSA

(for a target area of elements (FFs, gates) 1, 2, …, N)

$= \Sigma (t_i \times w_i)$

- $t_i = 1$ if the output of element i has a transition; otherwise, $t_i = 0$.
- W_i = (the number of fanout lines from element i) + α (usually 1)



Weight = 2 + 1

(source: S. Wang et al., Proc. ITC, pp. 250-258, 1994)

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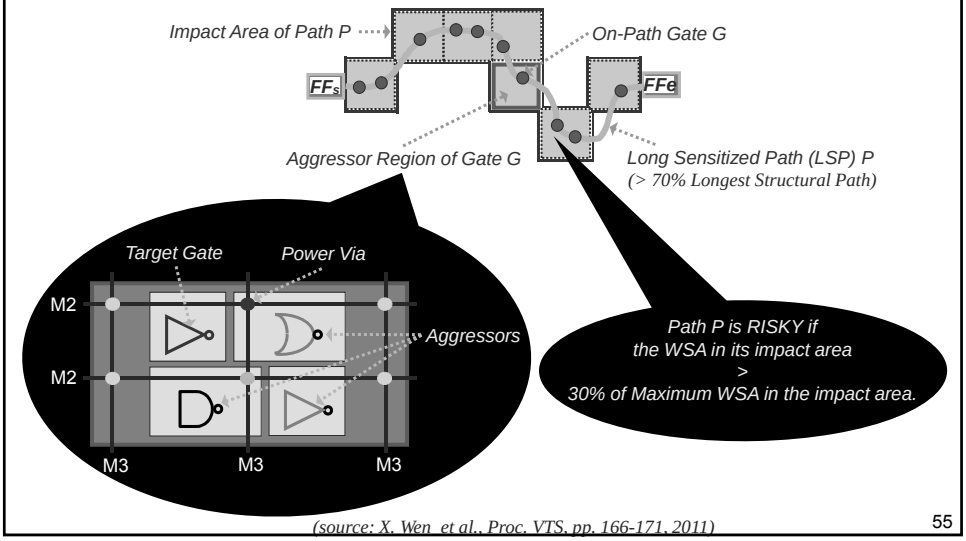
Low-Power Test Pattern Generation

Typical Metric for LTC Power Analysis - (2)

Regional Weighted Switching Activity



(source: X. Wen et al., Proc. VTS, pp. 166-171, 2011)

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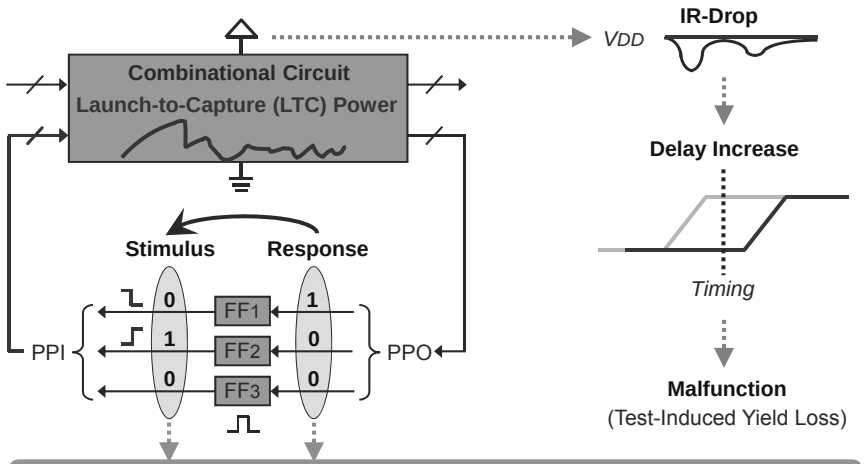
Low-Power Test Pattern Generation

Example 2: Low-LTC-Power X-Filling



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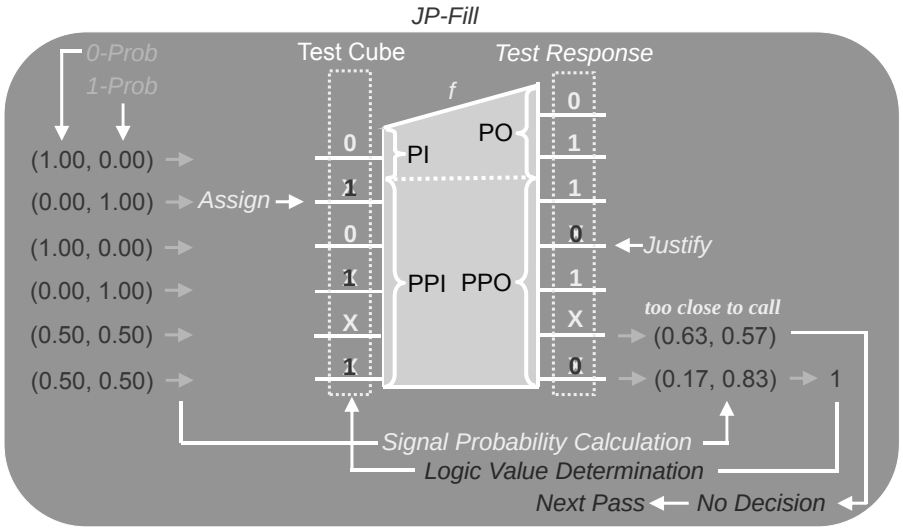
Low-Power Test Pattern Generation

Example 2 (cont'd): Low-LTC-Power X-Filling

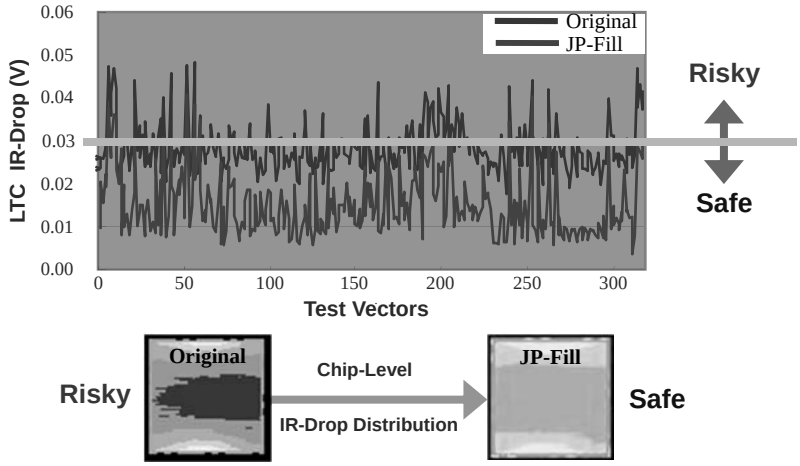


(source: X. Wen et al., Proc. ITC, Paper 25.1, 2007)

Low-Power Test Pattern Generation

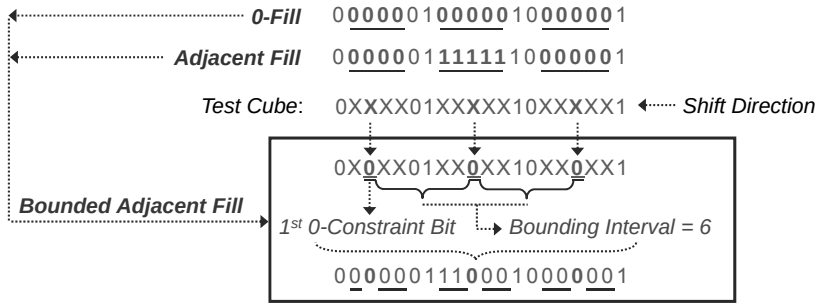
Example 2 (cont'd): Low-LTC-Power X-Filling

(Block in an Industry Chip: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)



Low-Power Test Pattern Generation

Example 3: Low-Shift-&-LTC-Power X-Filling



- The basic idea is to first set several *X*-bits in a test cube to 0 and then conduct *adjacent fill*.

➔ *The occurrence of 0 in the resulting fully-specified test vector is increased, which helps reduce shift-out and LTC power. → making use of the benefit of 0-fill*

➔ *At the same time, applying adjacent fill helps reduce shift-in power.*

(source: A. Chandra et al., Proc. VTS, pp. 131-138, 2008)

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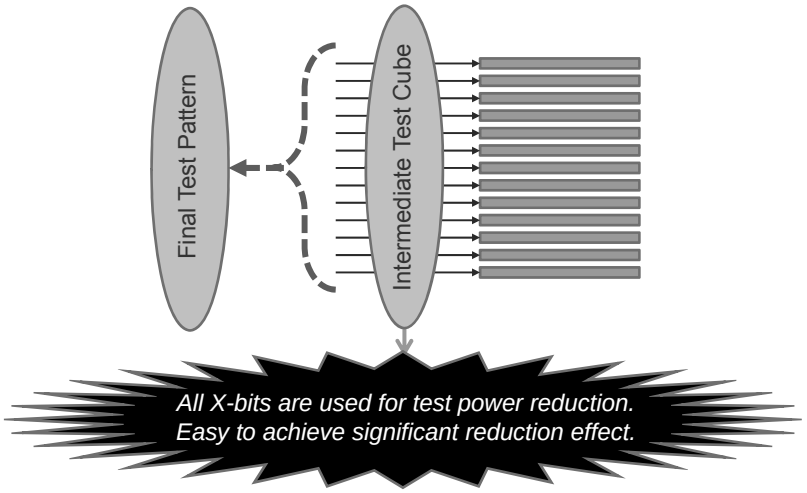
Low-Power Test Pattern Generation

Extension to Test Compression Environments - (1)

Non-Test-Compression Environment



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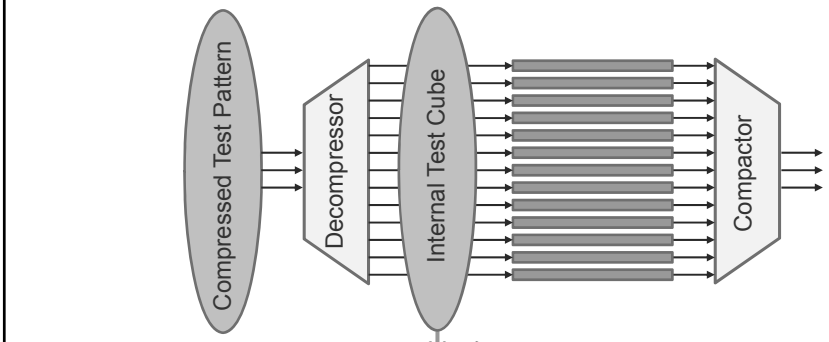
Low-Power Test Pattern Generation

Extension to Test Compression Environments - (2)

Test Compression Environment



X-bits are also needed for test compression.
Remaining X-bits may be insufficient for test power reduction.

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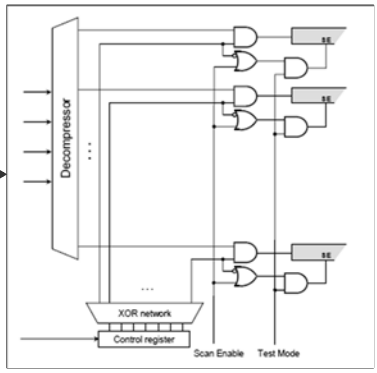
Low-Power Test Pattern Generation

Extension to Test Compression Environments - (3)

- **Shift Power Reduction**

  → Use additional circuitry to force constant values to scan chains.
  (0-Fill / 1-Fill: use one AND / OR gate for each scan chain)
  (MT-Fill / Adjacent-Fill: use a shadow register for each scan chain)

Forced 0-Fill →



(source: D. Czysz et al., Proc. ITC, Paper 13.2, 2008)

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Low-Power Test Pattern Generation

Extension to Test Compression Environments - (4)

- **LTC Power Reduction**
  - ***Combinational-Decompressor-Based Test Compression***
    - → Disable clock gators in test generation.
    - → Expand the combinational decompressor and apply low-LTC-power X-filling.
    - → Conduct pinpoint LTC power reduction.
  - ***Sequential-Decompressor-Based Test Compression***
    - → Disable clock gators in test generation.
    - → Apply low-LTC-power X-filling to independent or free X-bits.
    - → Conduct pinpoint LTC power reduction.

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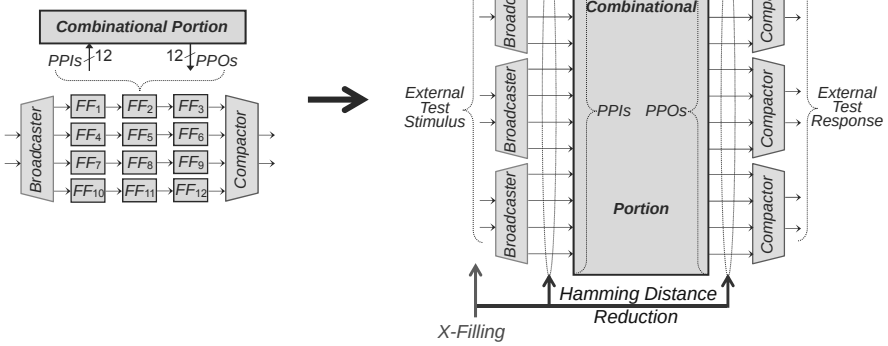
Low-Power Test Pattern Generation

Extension to Test Compression Environments - (5)

Low-LTC-Power X-Filling based on Combinational Decompressor Expansion



(source: K. Miyase, et al., Proc. ICCAD, pp. 97-104, 2009)

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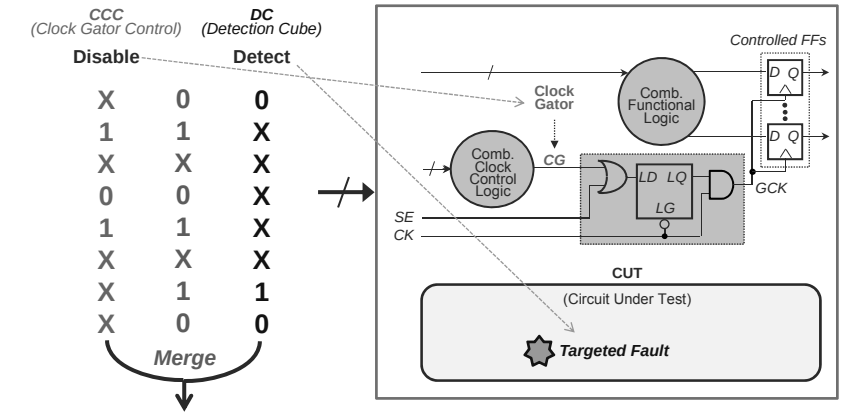
Low-Power Test Pattern Generation

Extension to Test Compression Environments - (6)

Disabling Clock Gators in Test Generation



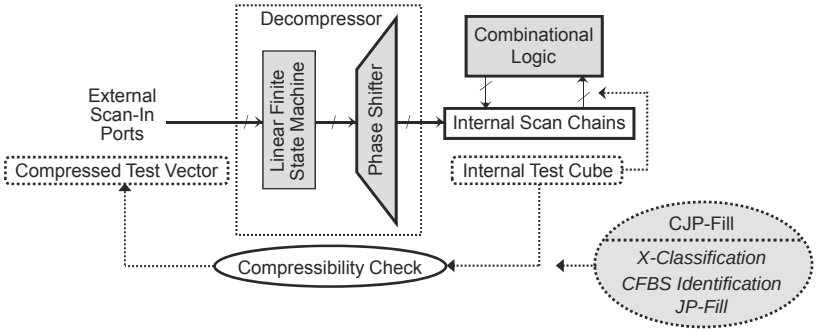
Fault Detection and Low LTC Power

(source: D. Czysz et al., Proc. ITC, Paper 13.2, 2008)

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (7)

X-Filling Using Independent / free X-Bits



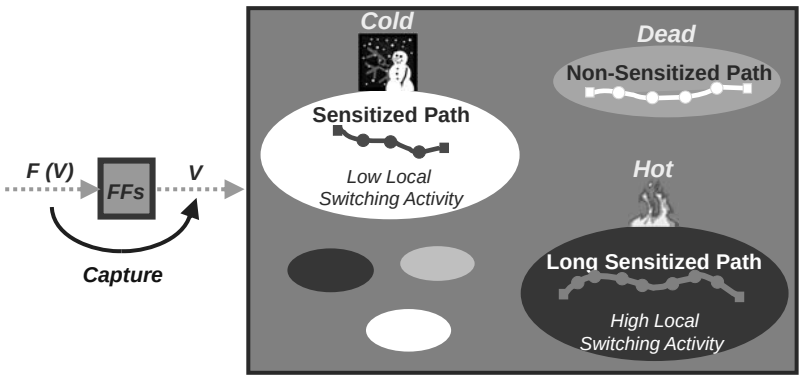
- ***X-classification*** for separating implied *X*-bits from free *X*-bits.
- ***CFBS identification*** for identifying a set of free *X*-bits that can be filled with any logic values simultaneously without affecting compressibility.

(source: M.-F. Wu et al., Proc. ITC, Paper 13.1, 2008)

Low-Power Test Pattern Generation

Extension to Test Compression Environments - (8)

Pinpoint LTC Power Reduction



Pinpoint

- Do not reduce transitions around ***Dead Areas***.
- ***Hot Areas*** must be removed by reducing local switching and/or masking.
- ***Cold Areas*** may be made "*warm*" by increasing local switching.

(source: X. Wen et al., Proc. VTS, pp. 166-171, 2011)

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Low-Power Test Pattern Generation

Summary - (1)

- A large portion of input bits in test cubes are don't care bits (X-bits) even after aggressive test compaction in ATPG.
- X-bits can be used for reducing various shift and/or LTC power. Especially, 0-fill can reduce shift-in, shift-out, and LTC power to some extent.
- X-filling-based low-power test generation causes neither area overhead nor performance degradation.
- Most commercial ATPG tools now support low-power X-filling.
- Test pattern count may increase due to low-power X-filling. This problem can be solved by
  (1: *Vector-Pinpoint*) identifying high-test-power test patterns and conducting X-filling only for those patterns, or
  (2: *Area-Pinpoint*) identifying high-test-power areas and conducting X-filing only to reduce test power in those areas.

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Low-Power Test Pattern Generation

Summary - (2)

Unfocused (***Global***) Reduction	Focused (***Regional***) Reduction
Over-Reduction Risk	No Over-Reduction
Under-Reduction Risk	Under-Reduction Countermeasure
Test Quality Degradation Risk	Minimum Test Quality Impact
Severe Test Data Increase	Minimum Test Data Increase
No Power Safety Guarantee	Power Safety Guarantee

(source: X. Wen, ETS, Invited Talk, 2012)

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Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

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Design for Test Power Reduction

During scan testing (standard or at-speed):

Shift Power Reduction	LTC Power Reduction
• Shift Impact Blocking *- blocking gate, special scan cell* *- first-level power supply gating* • Scan Chain Modification *- scan cell reordering* *- scan chain segmentation* *- scan chain disable* • Scan Clock Manipulation *- splitting, staggering* *- multi-duty clocking*	• Partial Capture *- circuit modification* *- scan chain disable* *- one-hot clocking* *- capture-clock staggering*

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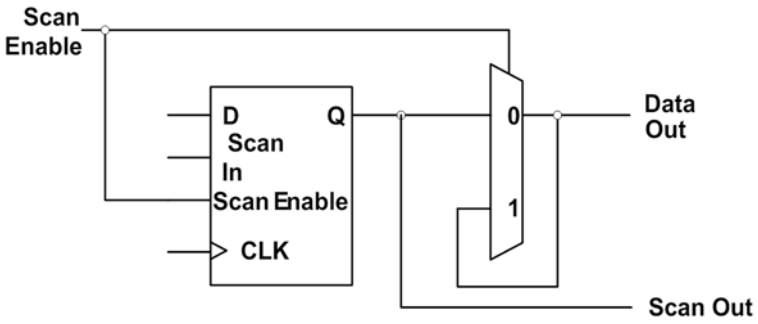
Design for Test Power Reduction

Example 1: Low power scan cell



An implementation of toggle suppression during shift using a latch at the output of the mux-D flip-flop with scan

(source: X. Zhang and K. Roy, Proc. IOLTW, pp. 133-138, 2000)

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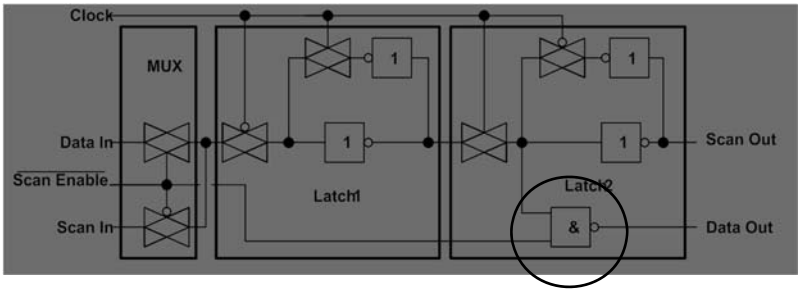
Design for Test Power Reduction

Example 1 (cont'd): Low power scan cell



- Master-slave structure of a mux-D flip-flop is modified
- Gate the data output during shift
- Toggle suppression during shift
- But modification of all flip-flops → impact on area and performance

(source: A. Hertwig and H.-J. Wunderlich, Proc. ETW, pp. 49-53, 1998)

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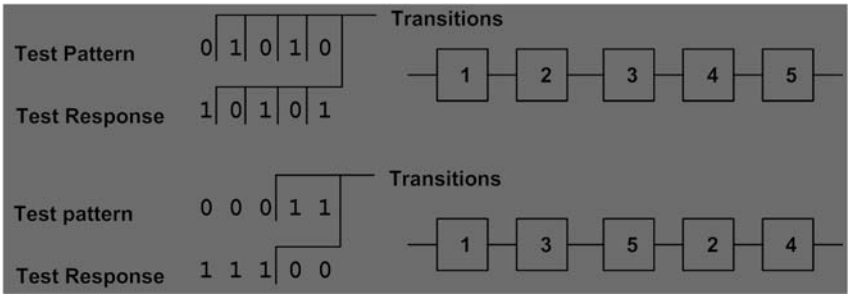
Design for Test Power Reduction

Example 2 : Scan cell reordering



- Scan cell order influences the number of transitions
- Need to change the order of bits in each vector during test application
- No overhead, FC and test time unchanged, low impact on design flow
- May lead to routing congestion problems …

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

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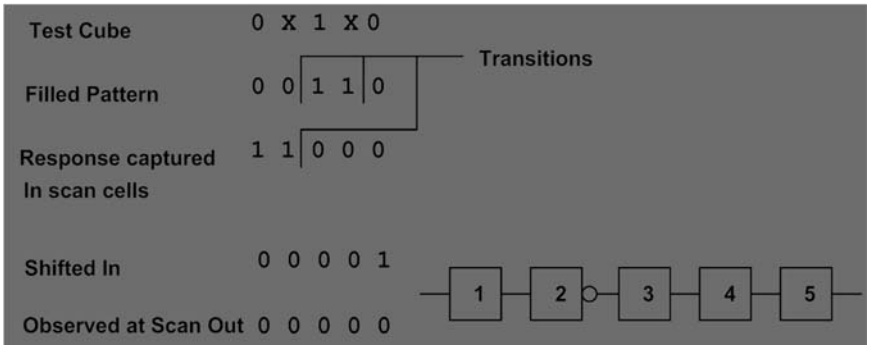
Design for Test Power Reduction

Example 3: Inserting logic into scan chains

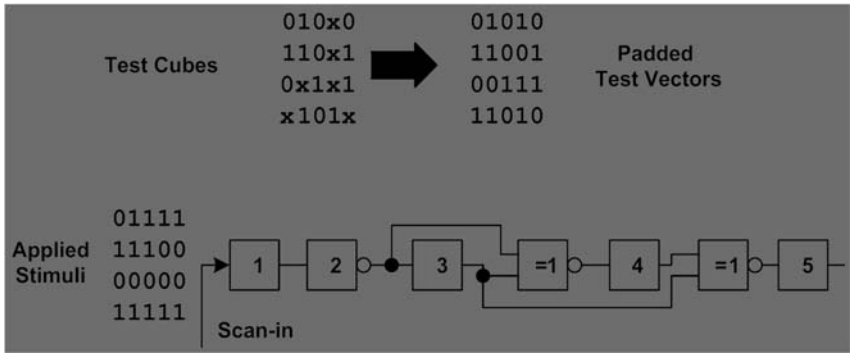


- The goal is to modify the transition count during shift.

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

Design for Test Power Reduction

Example 4: Scan segment inversion

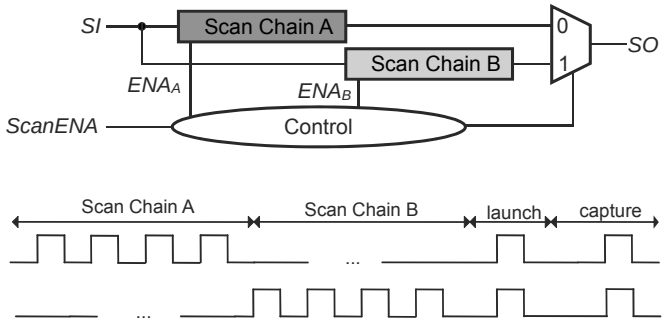


- This is done by embedding a linear function in the scan path
- Reduces the transition count in the scan chain

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

Design for Test Power Reduction

Example 5: Scan chain segmentation



- Controllable and data-independent effect of shift power reduction
- No change to ATPG and no increase in test application time
- Presented (and used) by TI @ ITC 2000

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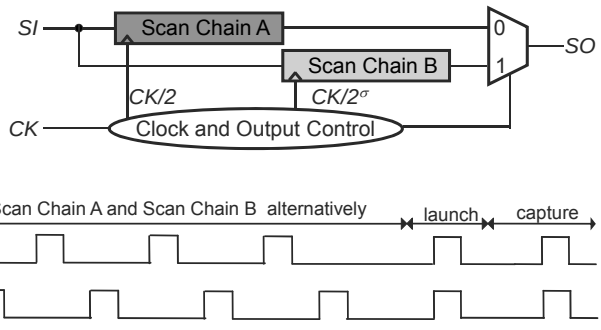
Design for Test Power Reduction

Example 5 (cont'd): Scan chain segmentation



- The original scan chain is segmented into two scan chains
- Each scan chain is driven by a clock whose speed is half of the normal speed
- At each clock cycle, only half of the circuit inputs can switch

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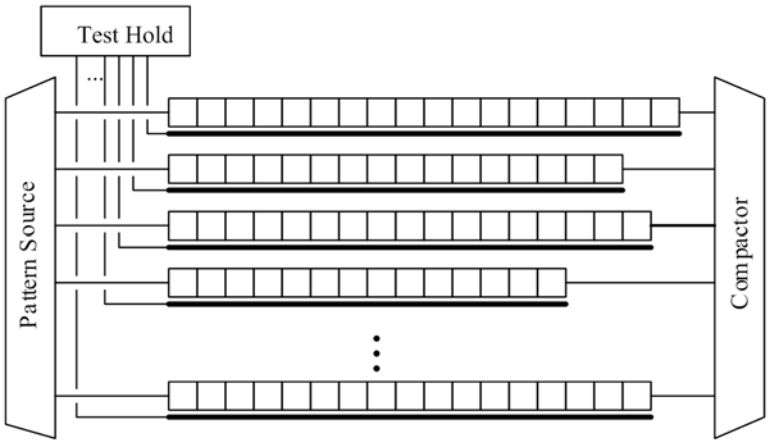
Design for Test Power Reduction

Example 6: Scan clock disabling

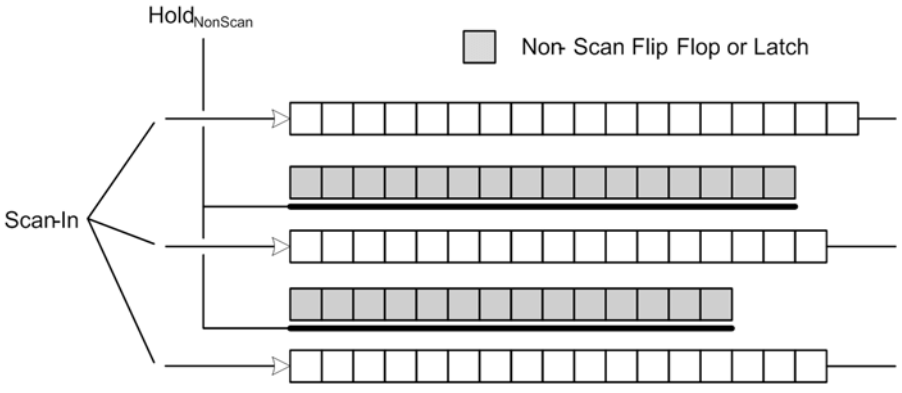


Clock gating per chain

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

Design for Test Power Reduction

Example 6 (cont'd): Scan clock disabling

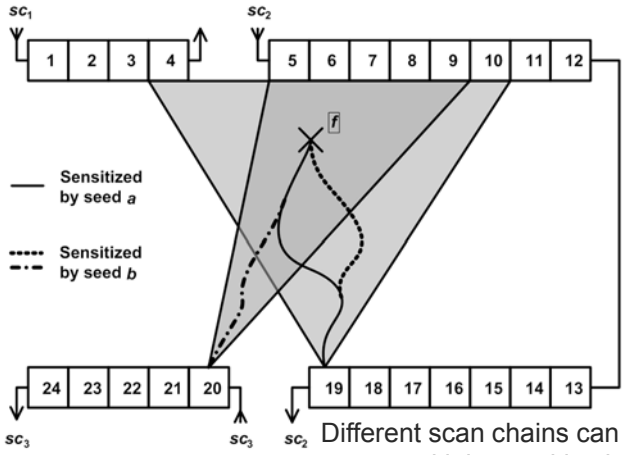


- Partial scan
  - Disable clocks on non-scan flip-flops or latches

(source: C. Zoellin et al., Proc. ITC, Paper 32.3, 2006)

Design for Test Power Reduction

Example 7: Scan partitioning



Different scan chains can be activated based on multiple sensitizations of the same fault

(source: C. Zoellin et al., Proc. ITC, Paper 32.3, 2006)

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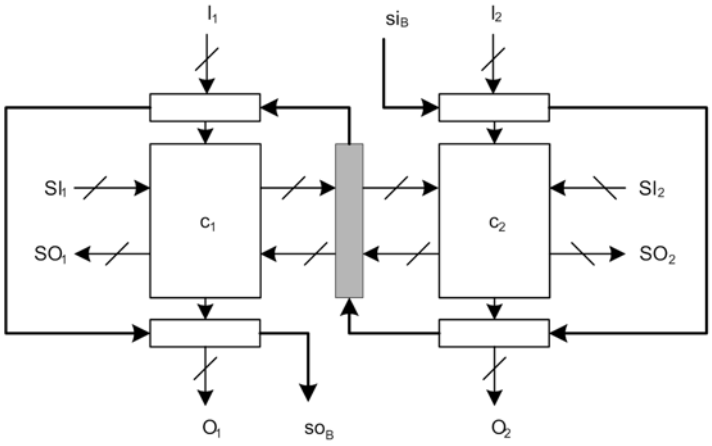
Design for Test Power Reduction

Example 8: Circuit partitioning



Isolating multiple blocks of logic using boundary registers

(source: P. Girard et al., Proc. ITC, pp. 652-661, 2000)

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Reducing Test Power

Main classes of dedicated solutions

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- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

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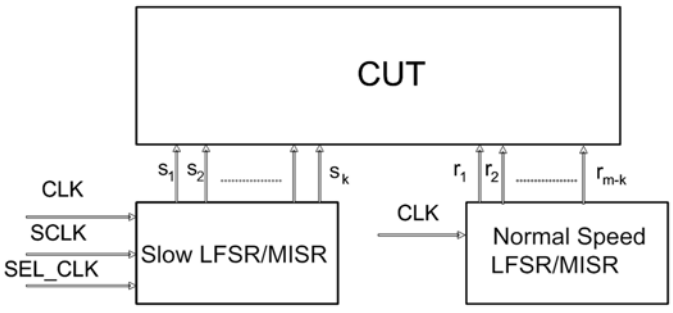
Power-Aware BIST and Compression

Example 1: Dual-speed LFSR for BIST



Dual-speed LFSR - concept

(source: S. Wang and S. Gupta, Proc. ITC, pp. 848-857, 1997)

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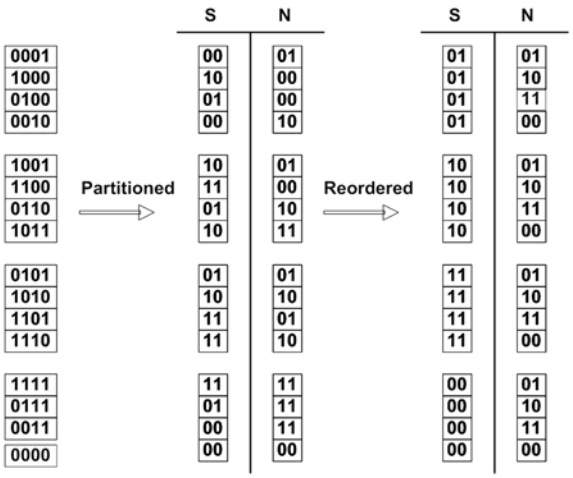
Power-Aware BIST and Compression

Example 1 (cont'd): Dual-speed LFSR for BIST



(source: S. Wang and S. Gupta, Proc. ITC, pp. 848-857, 1997)

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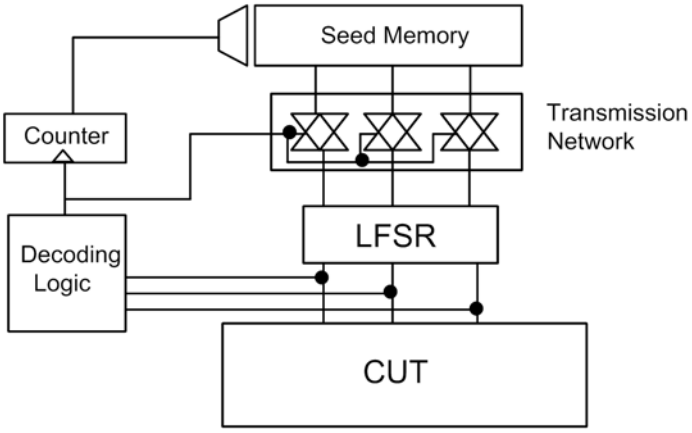
Power-Aware BIST and Compression

Example 2: Pattern suppression



Pattern suppression during BIST with re-seeding

(source: S. Manich, et al., JETTA, Vol. 16, Issue 3, 2000)

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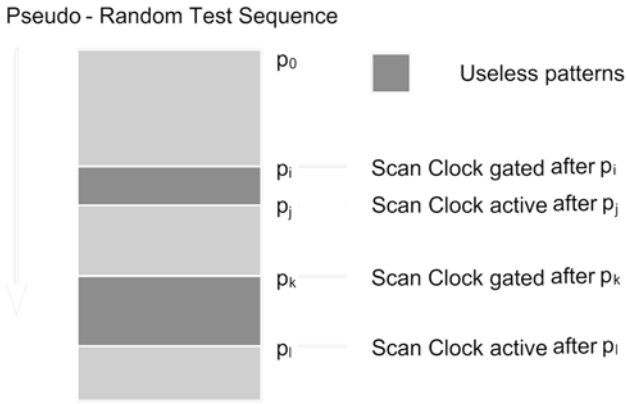
Power-Aware BIST and Compression

Example 2 (cont'd): Pattern suppression

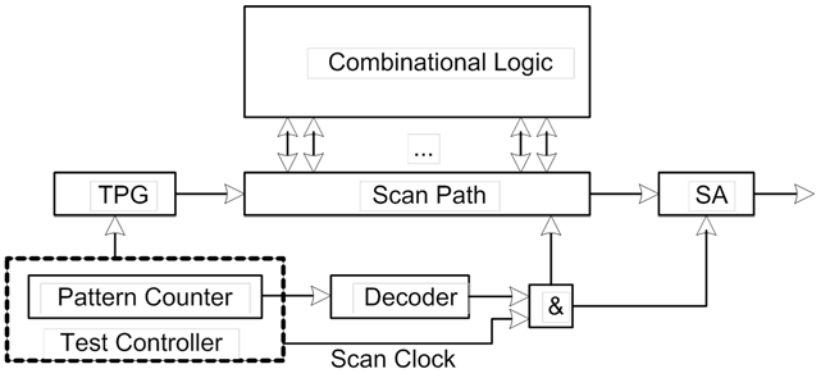


Useless patterns do not detect any faults
Deactivate scan clocks when no fault coverage improvement

(source: P. Girard et al., Proc. VTS, pp. 407-412, 1999)

Power-Aware BIST and Compression

Example 3: Pattern suppression in Scan BIST



- Decoder used for pattern suppression
  - Fault simulation
  - Logic minimization

(source: S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999)

Power-Aware BIST and Compression

Example 3 (cont'd): Pattern suppression in Scan BIST

index	binary	# faults
0	0000	17
1	0001	9
2	0010	4
3	0011	0
4	0100	5
5	0101	2
6	0110	3
7	0111	0

index	binary	#faults
8	1000	2
9	1001	0
10	1010	0
11	1011	1
12	1100	0
13	1101	0
14	1110	0
15	1111	0

{0000 , 0001 , 0010 , 0100 , 0101,
0110 , 1000 , 1011 , 1100} **on-set**

{0011 , 0111 , 1001 , 1010} **off-set**

{1101 , 1110 , 1111} **dc-set**

Implementing the pattern decoder

(source: S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999)

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Power-Aware BIST and Compression

Example 4: Application of Run-Length Coding

Group	Run-Length	Group Prefix	Tail	Codeword
A_1	0	0	00	000
	1		01	001
	2		10	010
	3		11	011
A_2	4	10	00	1000
	5		01	1001
	6		10	1010
	7		11	1011
A_3	8	110	00	11000
	9		01	11001
	10		10	11010
	11		11	11011

Golomb code

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)

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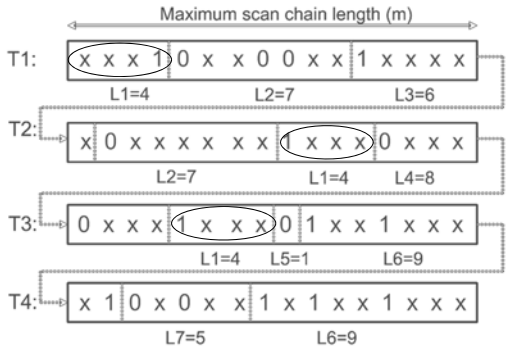
Power-Aware BIST and Compression

Example 5: Application of Huffman Coding



	Characters (Block Sizes) (Li)	Occurrence Frequency (fi)
N_1	1	1
	4	3
	5	1
	6	1
	7	2
	8	1
	9	2

Final Sequence (Li[v]):

4[1] 7[0] 6[1] 7[0] 4[1] 8[0] 4[1] 1[0] 9[1] 5[0] 9[1]

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)

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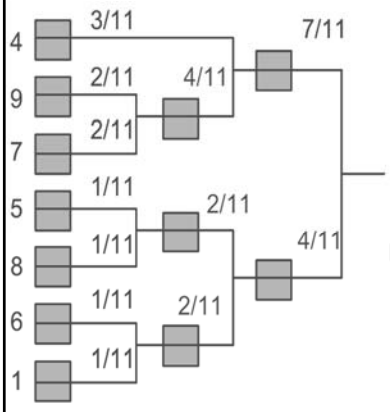
Power-Aware BIST and Compression

Example 5 (cont'd): Application of Huffman Coding



	Characters (Li)	Occurrence Frequency (fi)	Huffman Code (Ci)	Saving (Si)
N_1	4	3	00	+6
	9	2	010	+12
	7	2	011	+8
	5	1	100	+2
	8	1	101	+5
	6	1	110	+3
	1	1	111	-2
				S=+34

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)

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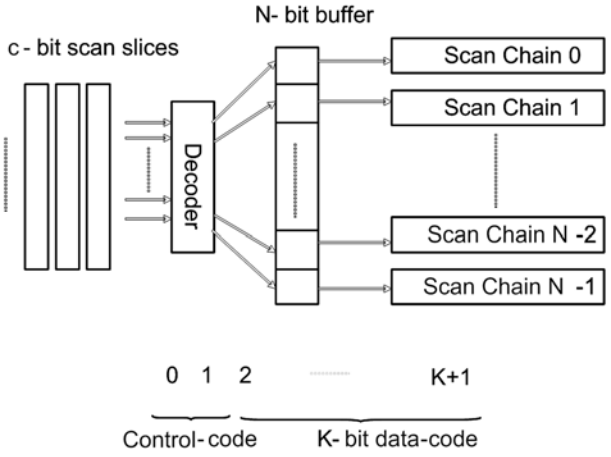
Power-Aware BIST and Compression

Example 6: Application of selective encoding



Selective encoding - concept

(source: Z. Wang and K. Chakrabarty, Proc. ITC, Paper 24.3, 2005)

Power-Aware BIST and Compression

Example 6 (cont'd): Application of selective encoding

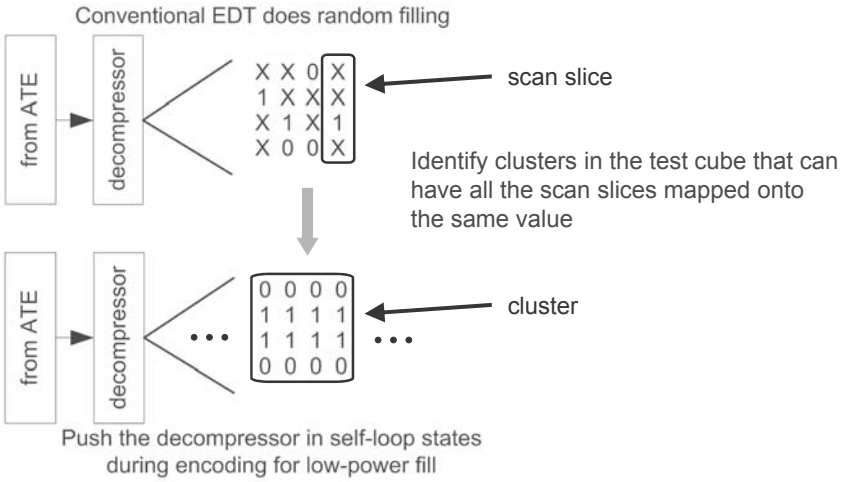
Slice	Slice code		Description
	Control code	Data code	
XX00 010X	00	0101	Start a new slice, map X to 0, set bit 5 to 1
1110 0001	00	0111	Start a new slice, map X to 0, set bit 7 to 1
	11	0000	Enter group-copy-mode, starting from bit 0 (i.e., group 0)
	11	1110	The data is 1110
XXXX XX11	01	1000	Start a new slice, map X to 1, no bits are set to 0

Selective encoding - example

(source: Z. Wang and K. Chakrabarty, Proc. ITC, Paper 24.3, 2005)

Power-Aware BIST and Compression

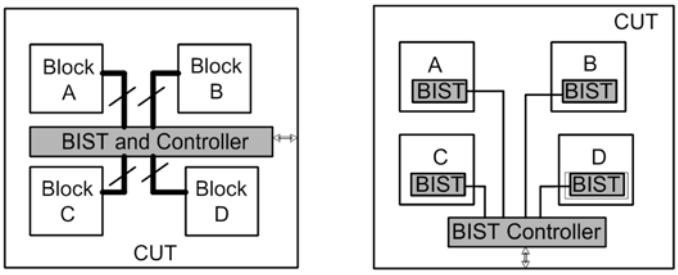
Example 7: Linear Finite State Machines



(source: F. Czysz et al., Proc. VTS, pp. 75-83, 2007)

Power-Aware BIST and Compression

Example 8: Centralized vs distributed BIST



- Circuit partitioning for low-power BIST
  - Centralized BIST and controller
  - Distributed approach where BIST sessions are power-conscious

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)

Reducing Test Power

Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

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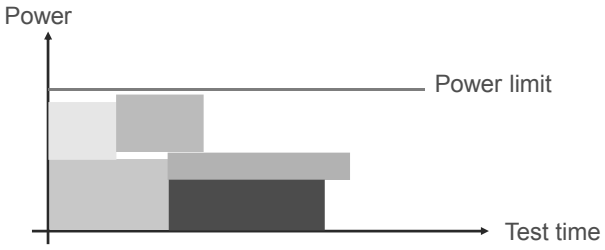
System-Level Power-Aware Scheduling

Improve Test Throughput by Exploiting Design Modularity



- The goal is to determine the blocks (memory, logic, analog, etc.) of an SOC to be tested in parallel at each stage of a test session in order to keep power dissipation under a specified limit while optimizing test time
- Some of the test resources (pattern generators and response analyzers) must be shared among the various blocks

(source: Y. Zorian, Proc. VTS, pp. 4-9, 1993)

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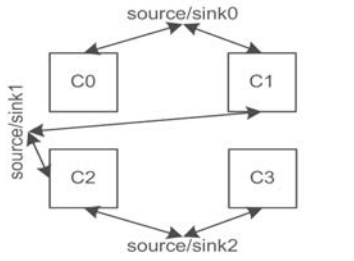
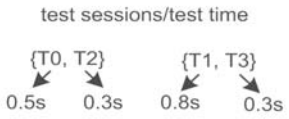
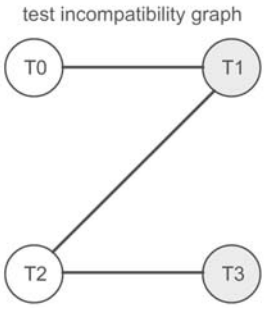
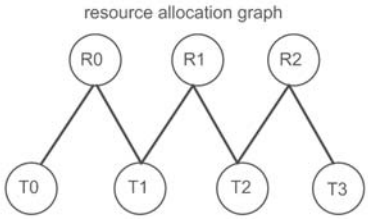
System-Level Power-Aware Scheduling

Example 1: Resource Allocation and Incompatibility Graphs









(source: R. Chou et al., IEEE Trans. on VLSI, Vol. 5, No. 2, pp. 175-185, 1997)

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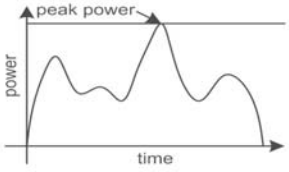
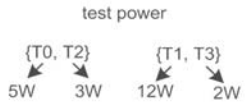
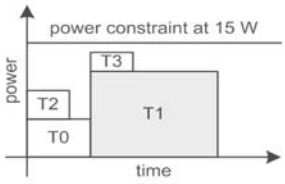
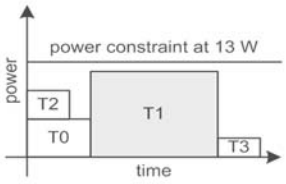
System-Level Power-Aware Scheduling

Example 2: Power Model and Test Schedule









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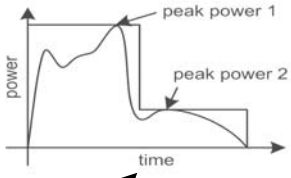
System-Level Power-Aware Scheduling

Example 3: Power Profile Manipulation

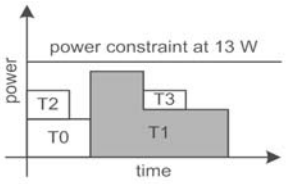


Power profile can be modified by pattern modification and/or test set reordering

test power

T1 — 12W for 0.3s

6W for 0.5s



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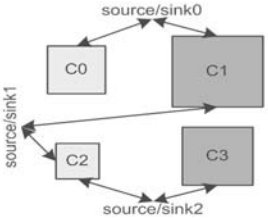
System-Level Power-Aware Scheduling

Example 4: Thermal Considerations



temperature dependent test

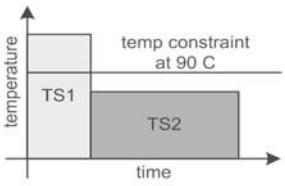
TS1 = {T0, T2} → 130 C

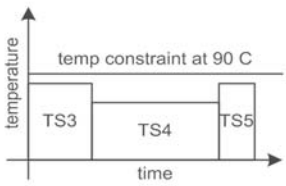
TS2 = {T1, T3} → 70 C

TS3 = {T0, T3} → 80 C

TS4 = {T1} → 60 C

TS5 = {T2} → 80 C





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Evaluating …

… Test Power Reduction Strategies

• Power reduction effectiveness	*High*
• Fault coverage impact	*Low*
• ATPG engine impact	*Minimum*
• Test data volume impact	*Low*
• Test time impact	*Low*
• Functional timing impact	*Low*
• Area overhead	*Low*
• Usability with test compression	*High*
• Design effort	*Minimum*
• Design flow change	*Low*

(source: S. Ravi, TI, ITC07)

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Test Power Estimation

- Needed for test space exploration (DfT/ATPG) early in the design cycle
- Availability of scan enhanced design and ATPG patterns only at the gate level in today's design flows imposes the usage of gate-level estimators for test power
- Conventional flow adopted to perform estimation is simulation-based
- Estimation is performed at various PVT corners
- Challenges for multi-million gate SoCs
  - Time-consuming !!
  - Dump sizes can be very large !!
- The weighted transition metric (WSA) is quick but approximate

Faster and low cost solutions for test power estimation are needed !

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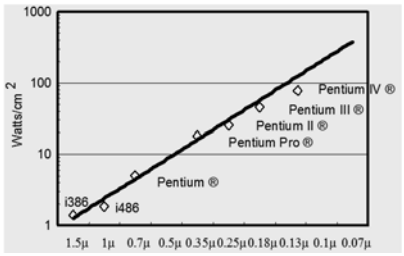
Low Power Design (LPD)

Power Consumption Trends

- Exponential growth in transistor density
  - More functionality
- But linear reduction in supply voltage
  - Not adequate to prevent power density to increase



(source: Tirimurti et al., DATE, 2004)

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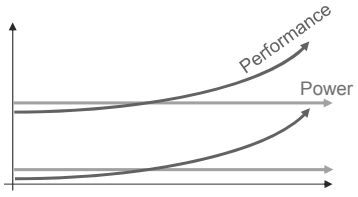
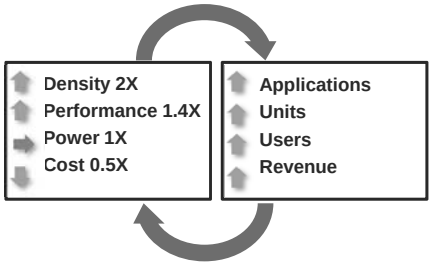
Low Power Design (LPD)

The new power-performance paradigm:

- Low (fixed) power budget to limit power density
- But ever increasing integration and performance …





Adoption of low-power design and power management techniques

(courtesy: M. Hirech, Synopsys, USA)

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Low Power Design (LPD)

System & Architecture	IC Design & Implementation
▪ Voltage / Frequency Scaling ▪ Architecture (parallel, well managed pipeline, etc.) ▪ Others (H/S partitioning, instruction set, algorithms, etc.)	▪ Clock Gating ▪ Multiple Supply Voltage ▪ Multiple Threshold Voltage ▪ Substrate-Bias ▪ Power Gating ▪ Others
Circuit (Logic) Design	**Process Technology**
▪ Low Power Cell Library ▪ Gate sizing (to equalize paths) ▪ Buffer insertion to reduce slew ▪ Logic restructuring to avoid hazards ▪ Memory Bit Cell and Compiler ▪ Others	▪ Reduce Vdd ▪ Threshold Voltage Option ▪ Low Capacitance Dielectric ▪ New Gate Oxide Material ▪ Transistor Sizing ▪ Others

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Low Power Design (LPD)

Main LPD techniques	**Power reduction**	
	Dynamic	Leakage
Clock gating	✓	
Power gating	✓	✓
Multi-Voltage domains	✓	
Multi-Threshold cells		✓

These techniques are often combined together to achieve the maximum power optimization value

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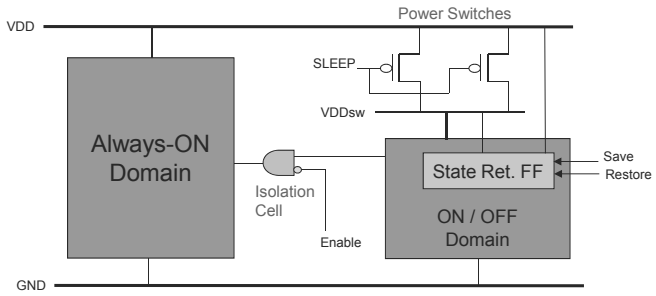
Power Management Infrastructure



PM Structure	Usage
Gated Clocks	Gates clock going to a sequential block
Power Switches	(SLEEP=1) cuts off VDD from going to core
Isolation Cells	(Enable=1) sets output of domain to 0 when power is shut down
State Retention FF	(Save=1) ensures that data is saved when power domain is OFF. (Restore=1) Restores the saved data when power domain wakes up

(courtesy: S. Ravi, TI)

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Power Specification Formats

- Need of specifying properties of a circuit block w.r.t. power dissipation during design, verification and implementation
- Interpreted by designers and design automation tools
- To achieve a unified and efficient design flow, various EDA tools need to use a common format
  - *Common Power Format* (CPF) created by Cadence
  - *Unified Power Format* (UPF) supported Synopsys, Mentor and Magma and standardized by IEEE (P1801 std. working group)
- 90% same concepts, but different syntaxes
- Both formats are based on the *Tool Control Language* (TCL) embedded in most EDA tools

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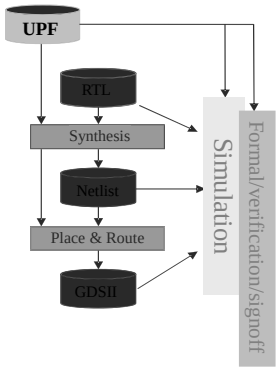
Power Specification Formats

- Used to describe the following specifications:
  - Voltage domains, Power domains, Isolation logic, Retention registers, Always-on cells, Power switches
  - The various power modes also need to be specified
  - Operating environment details (process, temperature, operating voltage data, and leakage calculation) are not part of UPF
  - UPF-based low power design flow →
- Example: creation of power domains

```
create_power_domain pdTOP
create_power_domain pd1 –elements U1
create_power_domain pd2 –elements U2
create_power_domain pd3 –elements U3
```



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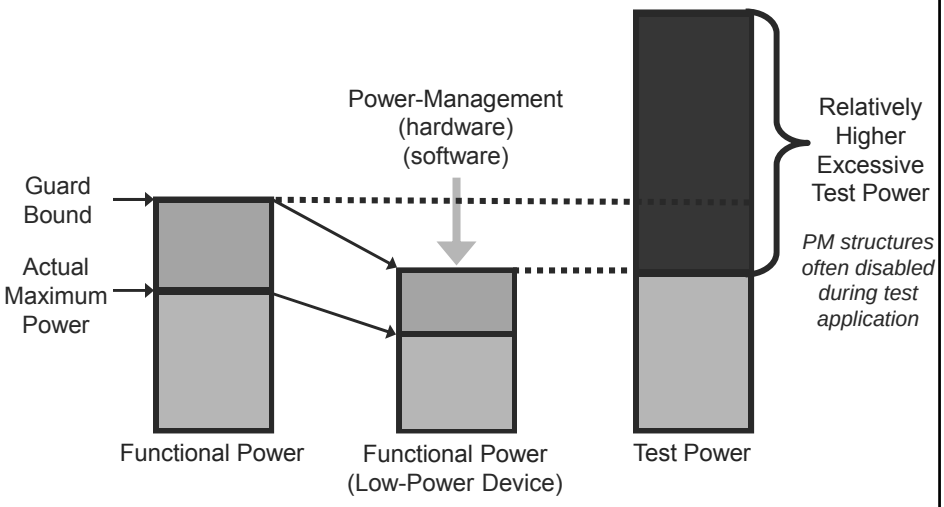
Power During Test …

Even more critical for Low-Power Design !!



(courtesy: X. Wen, KIT)

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Requirements for Test of LPD

- Reduce (even more) test power by using the power management (PM) infrastructure (and/or applying the previous dedicated solutions)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures

And still target:

High fault coverage, short test application time, small test data volume, low area overhead, etc … while making test power dissipation (dynamic and leakage) comparable to functional power

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Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

Objective (again)

Make test power dissipation comparable to functional power

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Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

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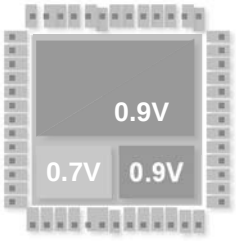
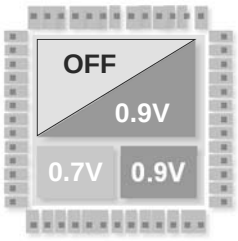
Test for Multi-Voltage Designs

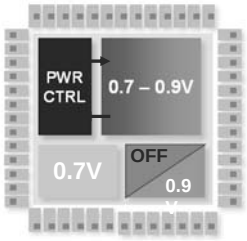
Multi-Voltage Design Styles



Multi-Voltage Multi-supply



Multi-Voltage with power gating



Dynamic Voltage Frequency Scaling (DVFS)

- Creation of “power islands”
- Vdd scaling results in quadratic power reduction ($P=kCV^2f$)
- Level shifters to let signals cross power domain boundaries

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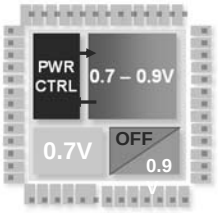
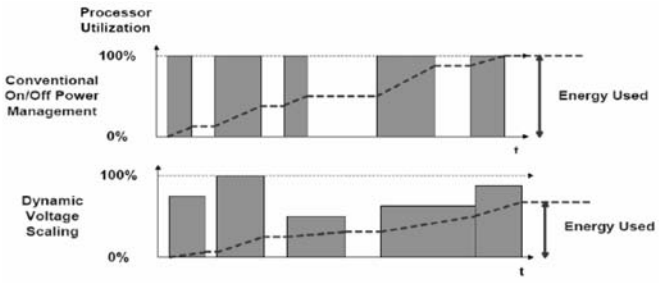
Test for Multi-Voltage Designs

DVFS Design Style

- When high performance is not required, V and F can be scaled down





- Design flow is similar to MSV flow, but more complex control mechanism and more complicated timing analysis

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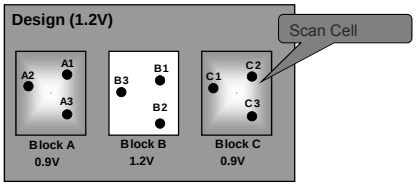
Test for Multi-Voltage Designs

Example 1: Multi-Voltage Aware Scan Cell Ordering

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93%)



Scan chain assembly

Ordering / Position	Logical	Physical	Multi-Voltage
1	A1	A2	A2
2	A2	A1	A1
3	A3	A3	A3
4	B1	B3	C1
5	B2	B1	C2
6	B3	B2	C3
7	C1	C1	B2
8	C2	C2	B3
9	C3	C3	B1

Level shifter

- Presented by Synopsys in JOLPE vol.1 n° 1 April 2005 and implemented in Synopsys Galaxy™ Test

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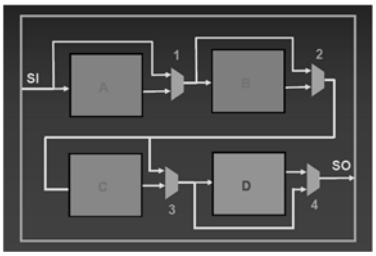
Test for Multi-Voltage Designs

Example 2: Power-Aware Scan Chain Assembly

- Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints
- Bypass multiplexers allow testing of specific power domains in MSMV environment (switched-off power domains are bypassed)
- Preserve test functionality !
- Presented by Cadence @ ITC 2008
  and implemented in Cadence *Encounter*™



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Test for Multi-Voltage Designs

Example 3: Voltage scaling in scan mode

- During scan shifting, the combinational logic needs not meet timing
- Goal: re-use the DVS infrastructure in test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
- At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
  - Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan FFs (V_t) = 0.35 V
  - If shift frequency (F_{shift}) = 125 MHz → V_{shift} = 0.635 V is enough !
- Presented by TI @ ITC 2007

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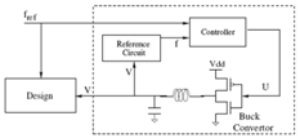
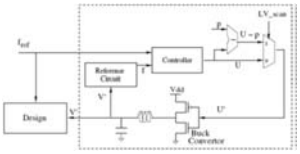
Test for Multi-Voltage Designs

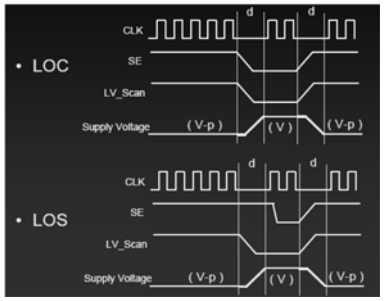
Example 3 (cont'd): Voltage scaling in scan mode



Conventional Voltage Scaling Apparatus



PMScan: Shift Voltage Scaling Apparatus



LV_scan: Control signal from tester for low-voltage scan

- Around 45% reduction of dynamic (average and peak) power and 90% reduction of leakage power, with negligible physical design impact and minimum area overhead

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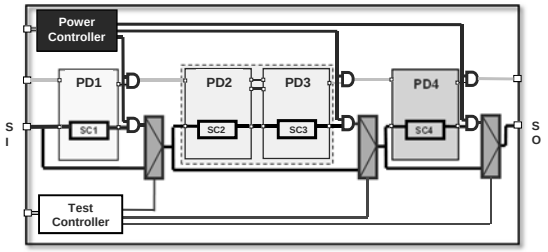
Test for Multi-Voltage Designs

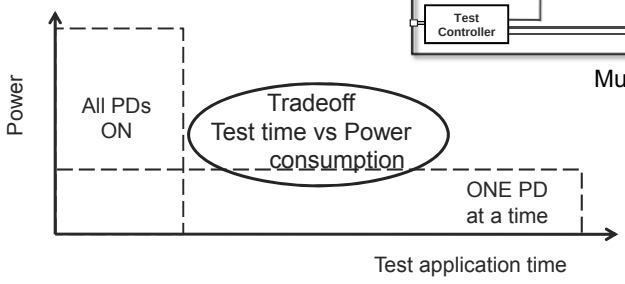
Example 4: Power Domain Test Planning

Objective:

Create distinct test modes (test partitioning) for power domains



Multi-mode DFT architecture



(Source: M. Hirech, Synopsys, DATE, 2008)

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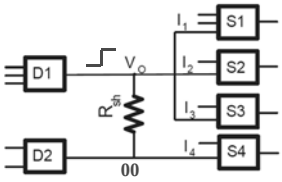
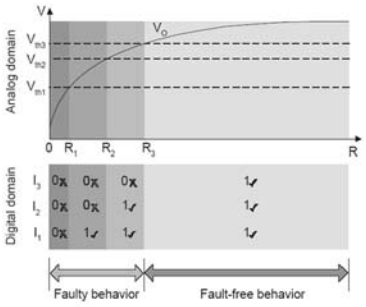
Test for Multi-Voltage Designs

Example 5: Test for MV Design – Bridge Defects

- **Bridge defects**
  - Most of them are resistive
  - Hard-shorts ~ stuck-at faults → detection is independent of Vdd
- **Resistive bridge defects**
  - A finite number of discrete intervals can be used to deal with all bridge R_{sh} values





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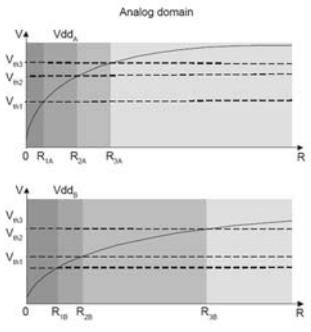
Test for Multi-Voltage Designs

Example 5: Test for MV Design – Bridge Defects

- **Resistive bridge behavior at MV settings**
  - Voltage Vo does not scale linearly with the input threshold voltage of S1, S2 and S3 when changing Vdd
  - Resistance intervals differ from one voltage setting to another
  - Example: a bridge with $R_{sh} = R_{3B}$ will cause a logic fault at V_{ddB} but not at V_{ddA}
  - A test pattern targeting a particular logic fault will detect different ranges of defects at different MV settings



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Test for Multi-Voltage Designs

Example 5: Test for MV Design – Bridge Defects

- **Goal of test generation for MV settings**
  - Generate test patterns for MV settings to maximize coverage of Resistive Bridging Faults (RBF) while minimizing test sequence length
  - Identification of Vdd specific test patterns for a given fault f
  - Example*: for a given circuit, 621 test patterns are needed at three Vdd settings with a commercial tool (207 at each Vdd), while only 391 test patterns applied at two Vdd settings (0.8V and 1.2V) are needed with the proposed technique (to achieve 100% fault coverage)

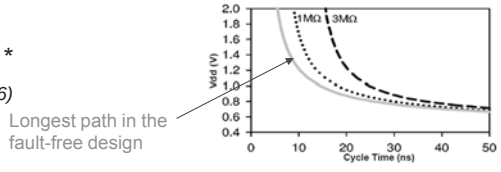
(source: U. Ingelson et al., ATS, 2007)

Test for Multi-Voltage Designs

Example 6: Test for MV Design – Open Defects

- **Open defects**
  - Due to unconnected nodes
  - Full opens → logic failures tested using static faults
- **Transmission gate opens**
  - Better detectability at low Vdd settings *(N. Zain Ali et al., ETS, 2006)*
- **Interconnect resistive opens**
  - Resistive opens → time-dependent → tested using delay tests
  - Better detectability at elevated Vdd settings *

(B. Kruseman et al., DATE, 2006)*



Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

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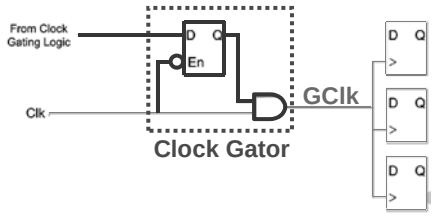
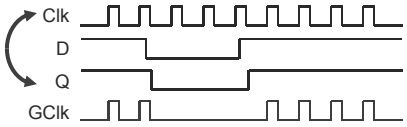
Test for Gated Clock Designs

Basic Clock Gating Design





- Not all FFs need to be triggered to perform a function (e.g., the camera control logic in a mobile-phone SoC can be inactive during a call).
- Gating-off the clock to functionally-noncontributing FFs reduces dynamic power dissipation, *not only in logic portions but also in clock trees (> 50%)*.
- One of the major techniques for reducing functional power.
- Widely adopted and supported by existing EDA tools.

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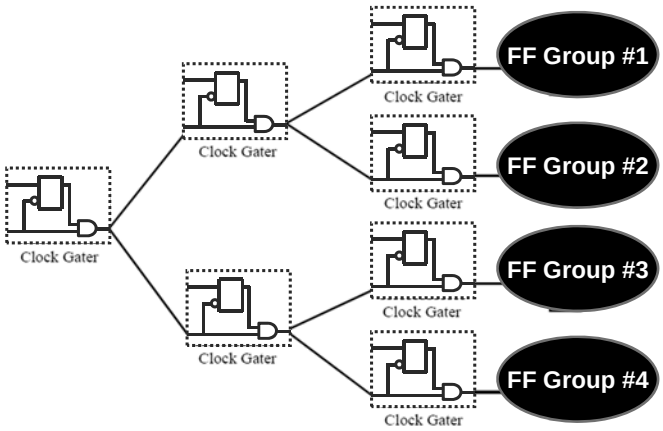
Test for Gated Clock Designs

Hierarchical Clock Gating Structure



- Higher flexibility in power control due to the availability of both fine-level and coarse-level clock gating.

(Source: X. Lin, Mentor Graphics, IGCC, 2011)

Test for Gated Clock Designs

Impact of Clock Gating on Test

- Clock gating prevents all scan FFs from being active at the same time.
- **Impact on Shift Mode**
  Negative → Scan shift realized through shift registers may become impossible if some FFs are inactive.

  ↓

  Shift Operation Guarantee Needed

  └ *DfT for Clock Gating Logic* ✓
- **Impact on Capture Mode**
  Positive → Dynamic power can be reduced.

  ↓

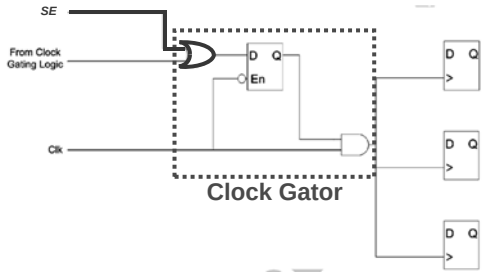
  Good for LTC Power Reduction

  ├ *Dynamic In-ATPG Techniques*
  ├ *Static In-ATPG Techniques* ✓
  └ *Post-ATPG X-Filling Techniques* ✓

Test for Gated Clock Designs

Example 1: DfT for Clock Gating Logic

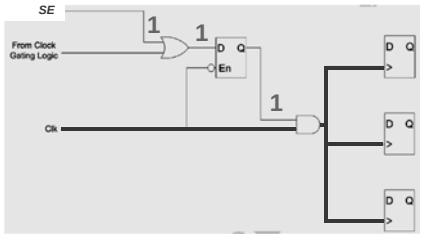
- **Shift Mode** (*SE* = 1): All scan FFs must be active to form one or more shift registers to shift-in test stimuli / shift-out test responses. Clock gating logic needs to be overridden (by *SE*) in shift mode.
- **Capture Mode** (*SE* = 0): Scan FFs are allowed to be controlled by clock gating logic. Nothing needs to be done.



- Automatically implemented by commercial DfT tools.

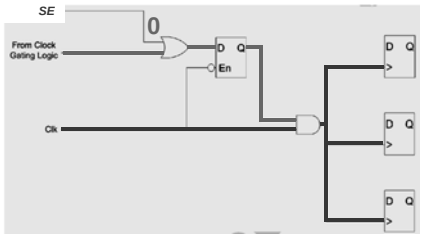
Test for Gated Clock Designs

Example 1 (cont'd): DfT for Clock Gating Logic



- Disable clock gating in ***shift mode*** (*SE* = 1): Unconditionally-ON Clock

Shift Register Operation



- Enable clock gating in ***capture mode*** (*SE* = 0): Conditionally-ON Clock

LTC Power Reduction

Test for Gated Clock Designs

Example 2: LTC Power Reduction by Clock Gating

Static In-ATPG Technique 1

- A **default value** is a value to be assigned to an input in order to gate-off a clock.
  - ➔ *A preset value is to be used to fill an X-bit in a test cube*.
- Flow for obtaining default values for clock gating:
  - ➔ *Identify all clock gators*.
  - ➔ *For each clock gator, calculate a set of input settings that set the clock off*.
  - ➔ *The values in each input setting are default values.*
- Flow for using default values for clock gating:
  - ➔ *Generate a test cube for fault detection*.
  - ➔ *Assign default values to the X-bits in the test cube*.
    (*If there are multiple choices of default values, use the one that can turn-off more FFs.*)

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

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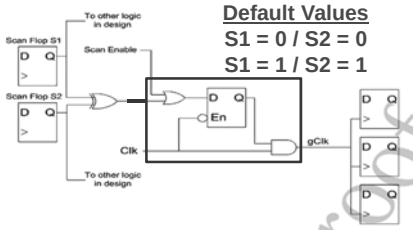
Test for Gated Clock Designs

Example 2 (cont'd): LTC Power Reduction by Clock Gating

Static In-ATPG Technique 1



Default Values
S1 = 0 / S2 = 0
S1 = 1 / S2 = 1

Test Cubes after ATPG

Test Cubes	Scan flops in design					
	S0	S1	S2	S3	S4	S5
T1	X	0	X	1	0	X
T2	0	1	X	X	X	0
T3	X	X	0	1	0	X

Test Cubes after Assigning Default Values
(S1=0 / S2=0)

Test Cubes	Scan flops in design						Merge "default values"?
	S0	S1	S2	S3	S4	S5	
T1	X	0	0	1	0	X	Yes
T2	0	1	X	X	X	0	Conflict
T3	X	0	0	1	0	X	Yes

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

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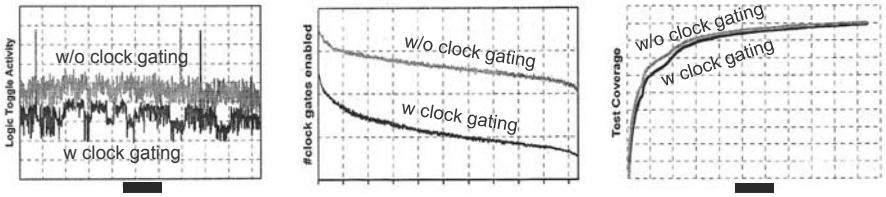
Test for Gated Clock Designs

Example 2 (cont'd): LTC Power Reduction by Clock Gating

Static In-ATPG Technique 1

Circuit Statistics
89K FFs
6 Scan Clocks
2200 Clock Gators



- The number of active clocks are reduced by more than 50%.
- LTC toggle activity is reduced by 35%.
- Fault coverage and test set size remain almost unchanged.

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

Test for Gated Clock Designs

Example 3: LTC Power Reduction by Clock Gating

Static In-ATPG Technique 2

Before Test Generation

- Conduct structural analysis to identify all clock gators for each clock.
- Obtain ***clock control cubes*** (***CCCs***).
  - ➔ *A CCC is a combination of 0s, 1s, and Xs that disables one or more clock gators.*
- Order CCCs by the decreasing number of FFs that a CCC turns off.

During Test Generation

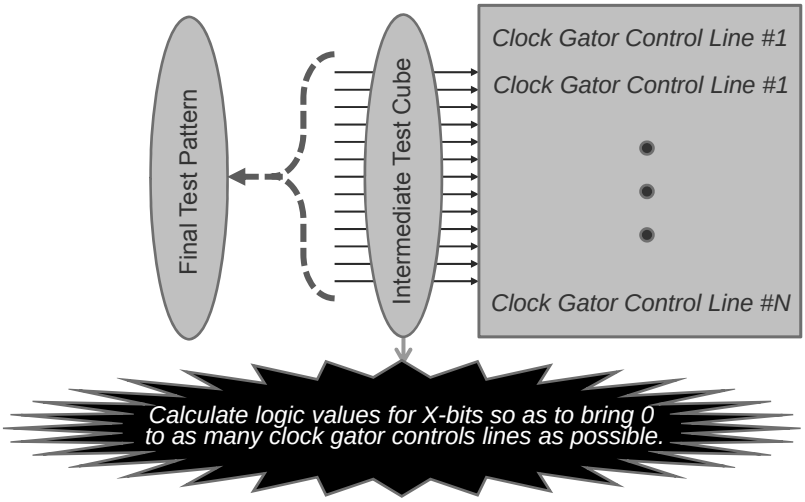
- Generate a test cube for detecting one or more faults.
- Merge the test cube with all compatible CCCs in the determined order.

(source: D. Czysz et al., Proc. ITC, Paper 13.2, 2008)

Test for Gated Clock Designs

Example 4: LTC Power Reduction by Clock Gating

Post-ATPG X-Filling Technique



(source: K. Enokimoto et al., Proc. ATS, pp. 99-104, 2009)

Test for Gated Clock Designs

Summary

- Functional clock gating is indispensable in reducing dynamic power.
- Functional clock gating logic needs to be modified in order to guarantee correct operation in *shift mode*.
- Clock gating can be used in *capture mode* to reduce LTC power.
  - ➔ Static In-ATPG Techniques
    (*Assign pre-determined clock-gator disabling values to don't-care bits (X-bits) in a test cube initially generated for fault detection.*)
  - ➔ Post-ATPG X-Filling Techniques
    (*Find and assign proper logic values to don't-care (X-bits) in a test cube so as to disable as many clock gators as possible.*)

Reducing Test Power of LPD

Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

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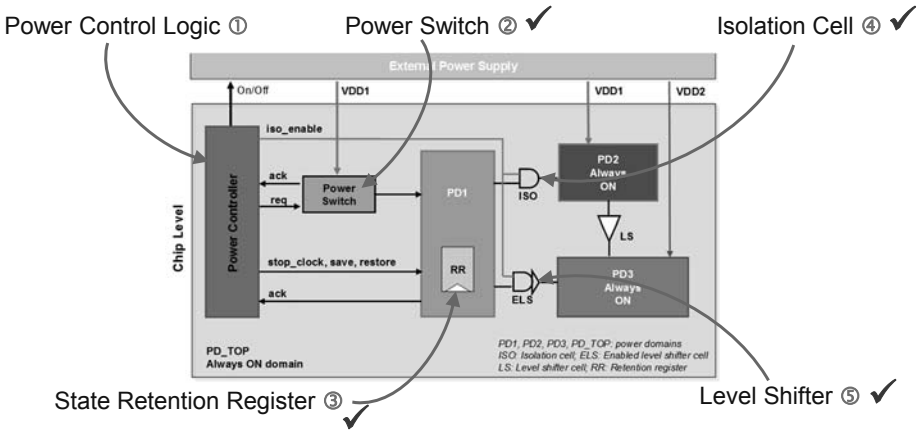
Test for Power Management Structures

Typical Power Management (PM) Structures



- Conditionally turning on or off power domains) to reduce dynamic and static power.
- Can be described in UPF (*Unified Power Format*) or CPF (*Common Power Format*).
- PM structures (①~⑤) require dedicated DfT methods and test patterns.

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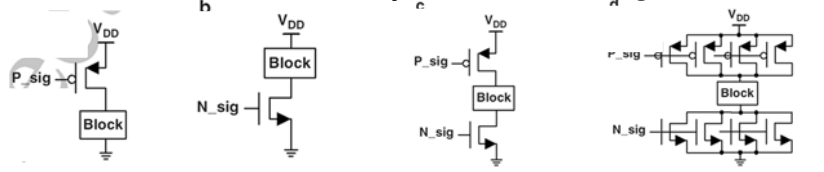
Test for Power Management Structures

Example 1: Test for Power Switches

Header Switch ***Footer Switch*** ***Symmetric Switch*** ***Segmented Switch***



Header Switch / Footer Switch / Symmetric Switch

- Also called sleep transistors and used to shut down blocks (power domains) that are not in use (idle mode), hence reducing leakage power and dynamic power.
- Should be large enough to provide sufficient current to the circuit.

Segmented Switch

- Individual switch transistors can be small.
- Preferable in practice due to concerns about layout, design for manufacturability, and limiting inrush current when switching on a power domain.

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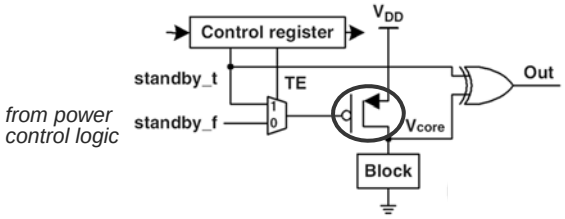
Test for Power Management Structures

Example 1 (cont'd): Test for Power Switches



- Pattern 1 (*Test for Short*): *TE* = 1 / *standby_t* = 1
  ➔ Turn-off the power switch. After sufficient discharge, Vcore should be much lower than VDD, and thus *Out* (fault-free) = 1 / *Out* (faulty) = 0
- Pattern 2 (*Test for Open*): *TE* = 1 / *standby_t* = 0
  ➔ Turn-on the power switch. Vcore should be close to VDD, and thus *Out* (fault-free) = 1 / *Out* (faulty) = 0

(source: Goal et al., Proc. ETS, pp. 145-150, 2006)

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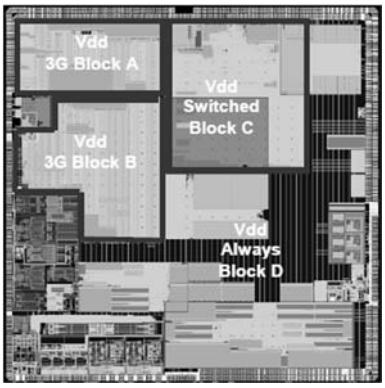
Test for Power Management Structures

Example 2: Parametric Test of Micro Switches



- Presented by ST-Ericson (Sophia) at International Test Conference 2008.
- Sigle-die 3G mobile phone base band Chip fabricated in 65nm technology.
- Includes multimedia features, such as video decoder, MP3 player, camera, games, and designed to be extremely low power.
- Rush current during power up → specific functional mode → test mode has to map functional mode !

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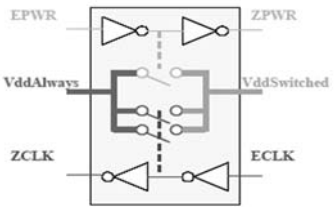
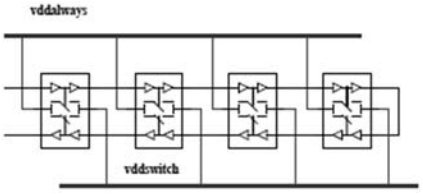
Test for Power Management Structures

Example 2 (cont'd): Parametric Test of Micro Switches





- The micro switches are daisy-chained. First, all the EPWR control signals are propagated in the chain. This gives a progressive ramp-up of the VddSwitched. Then, the ECLK control signal follows, turning 'on' all the transistors of the micro switches.
- Testing micro-switches individually is needed to detect resistive defects in each of them, and testing the micro switches' control chain is important to ensure the chain is not broken.

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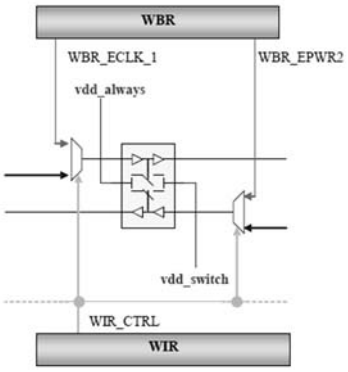
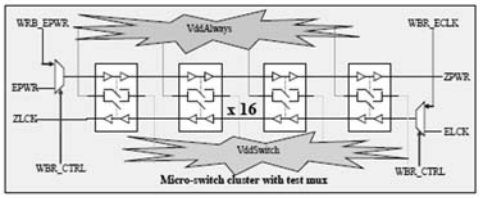
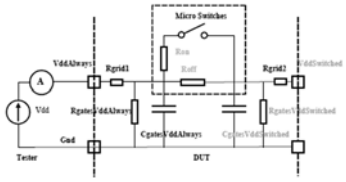
Test for Power Management Structures

Example 2 (cont'd): Parametric Test of Micro Switches







- DfT to add controllability and observability
- Test environment modeling needed to allow R_{off}/R_{on} measurement
- Test time for 150 clusters (each composed of 16 switches): 36 ms

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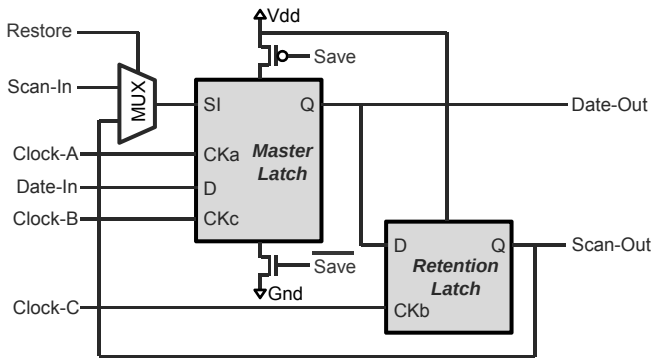
Test for Power Management Structures

Example 3: Test for State Retention Registers (SRR's)

- A SRR cell is for keeping its state when the power supply is turned off.
- Scan function can be designed into a SRR cell.



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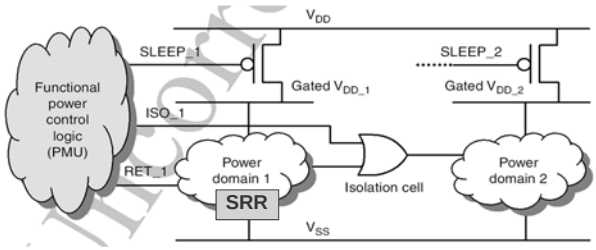
Test for Power Management Structures

Example 3 (cont'd): Test for State Retention Registers (SRR's)



Retention Capability Test

(1) Shift-in value *V* to SRR.
(2) Enable retention by setting *Save* to 1.
(3) Enable the isolation cell.
(4) Turn-off Power Domain 1.
(5) Turn-on Power Domain 1 after a few cycles.
(6) Disable the isolation cell.
(7) Disable retention by setting *Restore* to 1.
(8) Shift out the value of SRR and check if it is *V*.

Repeat for V = 0 and V = 1

Other tests, such as test for retention robustness to the state element's clock, asynchronous set/reset, etc., may also need to be applied.

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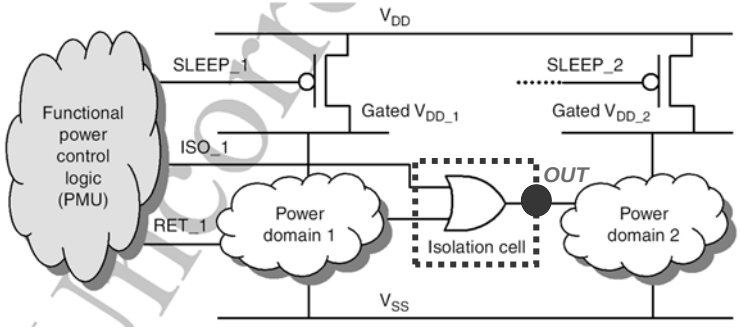
Test for Power Management Structures

Example 4: Test for Isolation Cells - (1)



(1) Turn-off Power Domain 1 (*SLEEP_1* = 1).
(2) Turn-on Power Domain 2 (*SLEEP_2* = 0).
(3) Set 1 to *ISO_1* and check if the isolation cell output (*OUT*) is 1.

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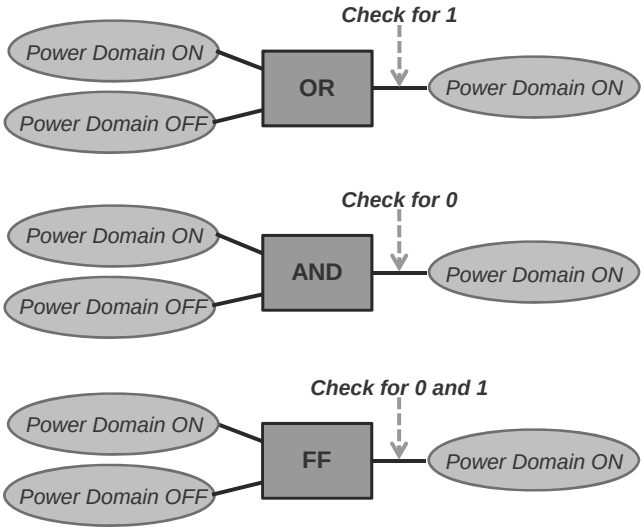
Test for Power Management Structures

Example 4: Test for Isolation Cells - (2)



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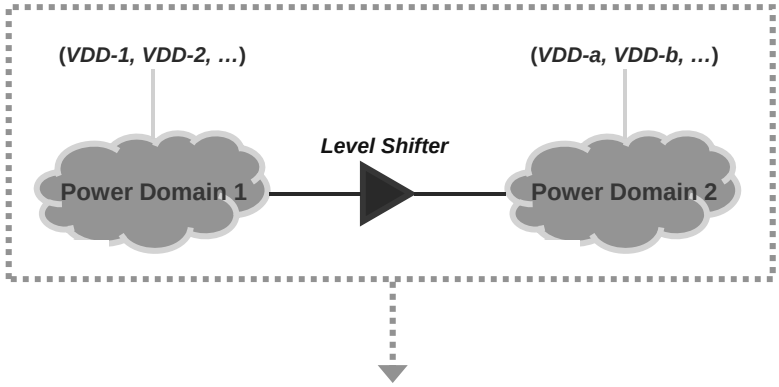
Test for Power Management Structures

Example 5: Test for Level Shifters



Test as a whole under all power supply voltage combinations of Power Domain 1 and Power Domain 2.

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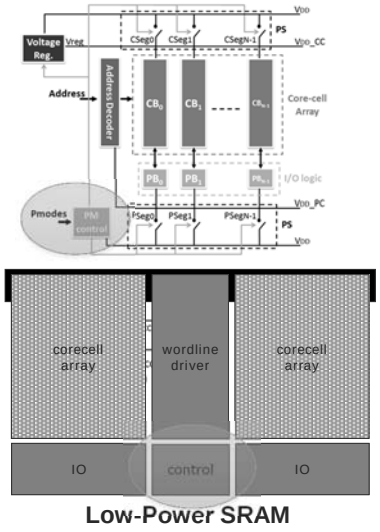
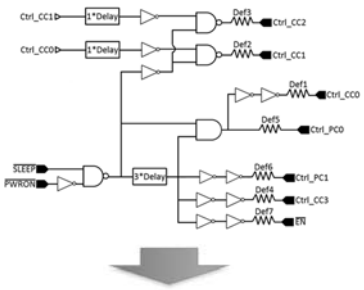
Test for Power Management Structures

Example 6: Test for Power Mode Control Logic in SRAMs



Low-Power SRAM



- Study performed on Intel MC products in 2011
- Impact of resistive-open defects on the PMC logic
- Definition of appropriate fault models (FFM)
- Proposal of a new March test (LZ) solution

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Test for Power Management Structures

Summary

- More and more power management structures are used in various IC designs in order to reduce power (dynamic and static) dissipation.
- Conventional ATPG does not target power management structures, leading to potential quality problems.
- There is a strong need to fully understand the basics of various power management structures and their operation modes.
- Special considerations and even new algorithms are needed to fully test various power management structures.
  - Clock Gating Logic (Clock Gator, Control Logic)
  - Power Gating Logic
    - → PMU (Power Management Unit)
    - → Power Switch
    - → State Retention Register, Isolation Cell, Level Shifter
  - Power Distribution Network

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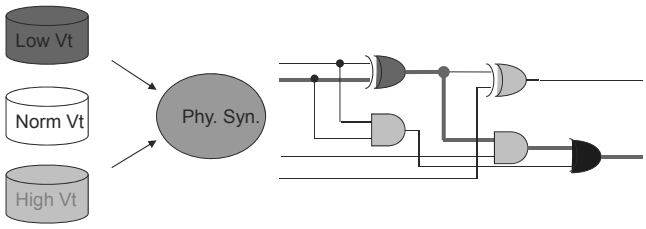
Impact of MTV Design on Test

- Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction → speed cost to decrease leakage !!
- MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)
- Leakage power reduction while meeting timing and no area overhead
- Well established and supported by existing EDA tools



(source: CADENCE, 2007)

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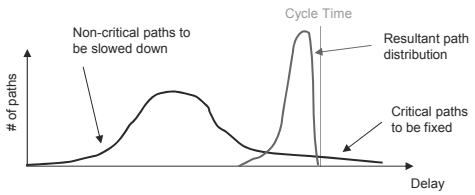
Impact of MTV Design on Test

- By using such power optimization techniques, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations
  - PDF selection more complex
  - More test data are needed
  - Sensitivity to variations



- PSN has a significant impact on the timing behavior
  - Need to integrate PSN effects in delay test pattern generation

Solutions for high quality at-speed fault coverage are needed !

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Power-Aware DFT Tools

- **Synopsys:**
  - Galaxy™ Test is a comprehensive test automation solution.
  - DFT Compiler and its low power features (for more details on this tools, see "Power and Design for Test: A Design Automation Perspective", A. De Colle et al, Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, April 2005)
  - DFT MAX and its low power features (for more details on this tools, see "DFT MAX and Power", R. Kapur et al, Journal of Low Power Electronics (JOLPE), Vol. 3, N° 2, August 2007)
  - TetraMAX® - power-aware test patterns for defect detection
  - Details
    http://www.synopsys.com/Tools/Implementation/RTLSynthesis/Test/Pages/default.aspx

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Power-Aware DFT Tools

- **Mentor:**
  - Tessent™ FastScan™ and Tessent™ TestKompress™ provide comprehensive low-power and power-aware test solutions.
  - Details at http://www.mentor.com/products/silicon-yield/logic_test/
- **Cadence:**
  - Encounter® Test, a key technology in the Cadence® Encounter digital IC design platform
  - To support manufacturing test of low-power devices, Encounter Test uses power intent information to create distinct test modes automatically for power domains and shut-off requirements.
  - Details
    http://www.cadence.com/products/ld/test_architect/pages/default.aspx

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Conclusion

- Power consumption during Test is a real issue !!
- Not only during manufacturing test but also during on-line test
- Not only ATPG and DFT but also BIST, test compression, and test scheduling have been addressed
- No generic solution, but rather a combination of solutions. Example: power-aware DfT for reducing shift power and power-aware ATPG for reducing LTC power
- New test solutions for Low-Power Design that preserve test functionality are needed !!

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Thank You !

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