Tutorial intitulé "Power-Aware Testing and Test Strategies for Low Power Devices"

Patrick Girard, Nicola Nicolici, Xiaoqing Wen

▶ **To cite this version:**

Patrick Girard, Nicola Nicolici, Xiaoqing Wen. Tutorial intitulé "Power-Aware Testing and Test Strategies for Low Power Devices". ITC'2012: International Test Conference, Nov 2012, Anaheim, CA, United States. lirmm-00820734

HAL Id: lirmm-00820734

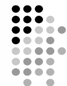
https://hal-lirmm.ccsd.cnrs.fr/lirmm-00820734v1

Submitted on 6 May 2013

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

ITC 2012 – Anaheim, USA

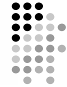


Power-Aware Testing and Test Strategies for Low Power Devices

Patrick GIRARD
LIRMM / CNRS
France

Nicola NICOLICI
McMaster University
Canada

Xiaoqing WEN
Kyushu Institute of Technology
Japan



Power-Aware Testing and Test Strategies for Low Power Devices

P. Girard; N. Nicolici; X. Wen (Eds.)

390 p., 222 illus., Hardcover

ISBN: 978-1-4419-0927-5

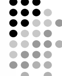
November 2009

Springer web site:

http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4419-0927-5

2

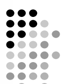
Motivation and Objectives



- Power constraints have severe impact on test
- Implications for test engineers / test tool developers:
  - Reduce power consumption in test mode becomes mandatory
  - Dedicated test strategies for low-power devices are needed
- **Objectives of this tutorial:**
  - Learning more about the impact of power during test
  - How to alleviate test power issues
  - How low-power devices and power management structures can be tested safely

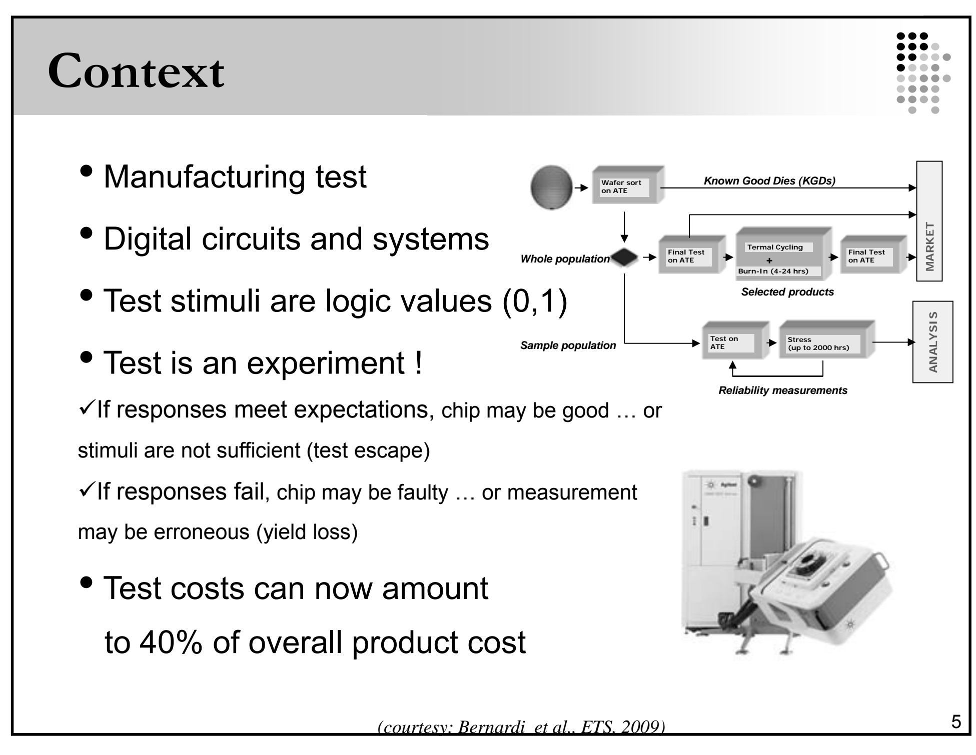
3

Outline

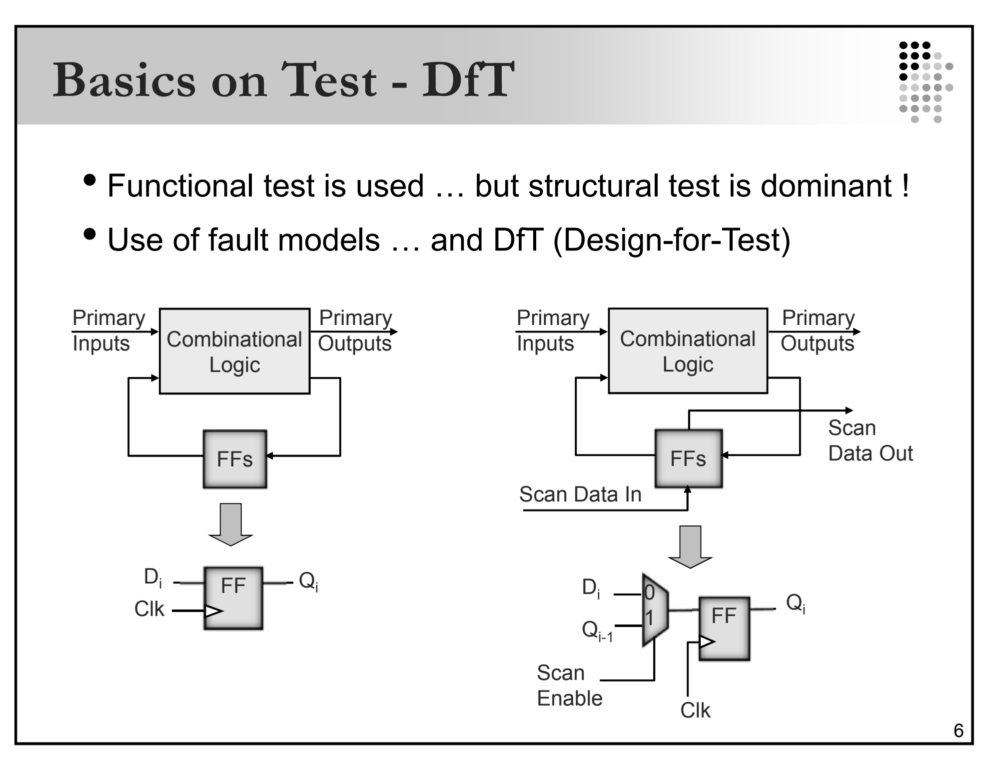


1. Basics on Test
2. Relevance of power during test
3. Main test power issues
4. Reducing test power by dedicated techniques
5. Low power design and its implications on test
6. Reducing test power of low power circuits
7. Conclusion

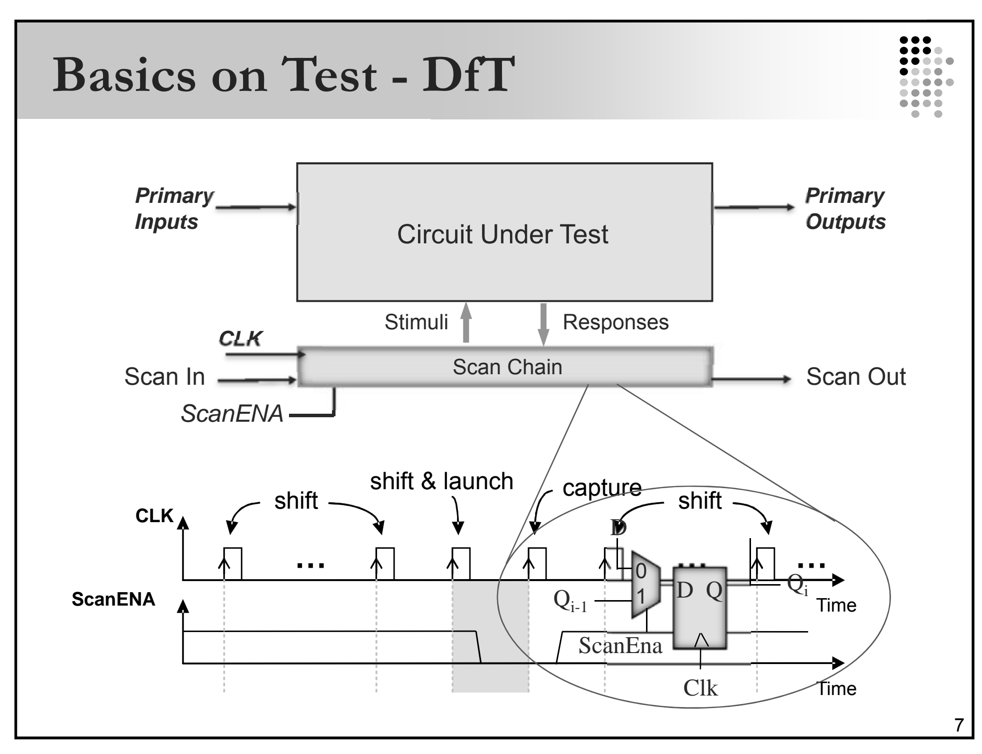
4

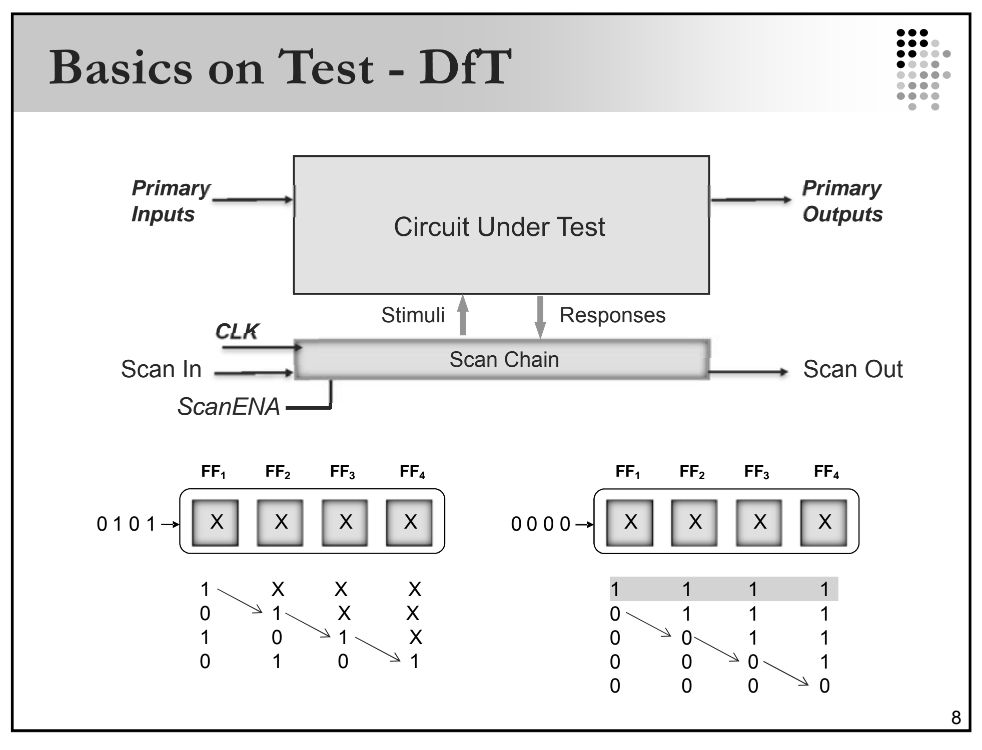


Context
• Manufacturing test
• Digital circuits and systems
• Test stimuli are logic values (0,1)
• Test is an experiment !
✓If responses meet expectations, chip may be good … or stimuli are not sufficient (test escape)
✓If responses fail, chip may be faulty … or measurement may be erroneous (yield loss)
• Test costs can now amount to 40% of overall product cost
Wafer sort on ATE
Known Good Dies (KGDs)
Whole population
Final Test on ATE
Termal Cycling
+
Burn-In (4-24 hrs)
Final Test on ATE
Selected products
MARKET
Sample population
Test on ATE
Stress (up to 2000 hrs)
Reliability measurements
ANALYSIS
(courtesy: Bernardi et al., ETS, 2009)
5

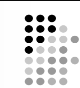


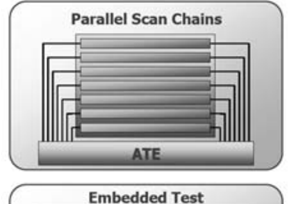
Basics on Test - DfT
• Functional test is used … but structural test is dominant !
• Use of fault models … and DfT (Design-for-Test)
Primary Inputs
Combinational Logic
Primary Outputs
FFs
Di
Clk
FF
Qi
Primary Inputs
Combinational Logic
Primary Outputs
Scan Data Out
FFs
Scan Data In
Di
Qi-1
0
1
FF
Qi
Scan Enable
Clk
6

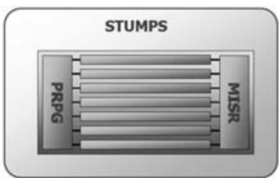

Basics on Test - DfT
Primary Inputs
Circuit Under Test
Primary Outputs
Stimuli
Responses
CLK
Scan In
Scan Chain
Scan Out
ScanENA
shift & launch
shift
capture
shift
CLK
ScanENA
Time
Time
D
0
1
D Q
Q_{i-1}
Q_i
ScanEna
Clk
7

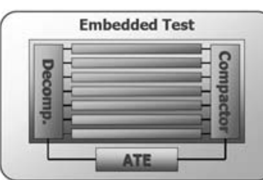

Basics on Test - DfT
Primary Inputs
Circuit Under Test
Primary Outputs
Stimuli
Responses
CLK
Scan In
Scan Chain
Scan Out
ScanENA
FF_1 FF_2 FF_3 FF_4
0 1 0 1
X X X X
0 0 0 0
X X X X
1 X X X
0 1 X X
1 0 1 X
0 1 0 1
1 1 1 1
0 1 1 1
0 0 1 1
0 0 0 1
0 0 0 0
8

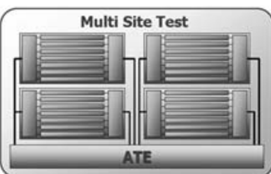
Basics on Test - DfT

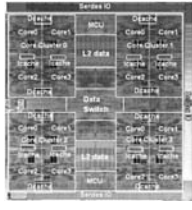










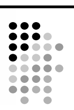


Example (presented @ ITC 2008):

- 16 core CMT microprocessor from Sun Microsystems
- 410 millions of transistors, 250W @ 2.3GHz, 1.2V
- **1.35 millions of flip-flops, all are scannable !!**

9

Power Consumption in CMOS

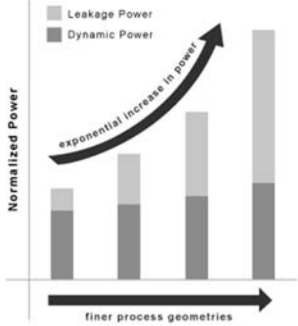


Switching (dynamic) Power

- Due to charge/discharge of load capacitance during switching
- $P_{DYN} \propto V_{DD}^2 . F_{CLK}$

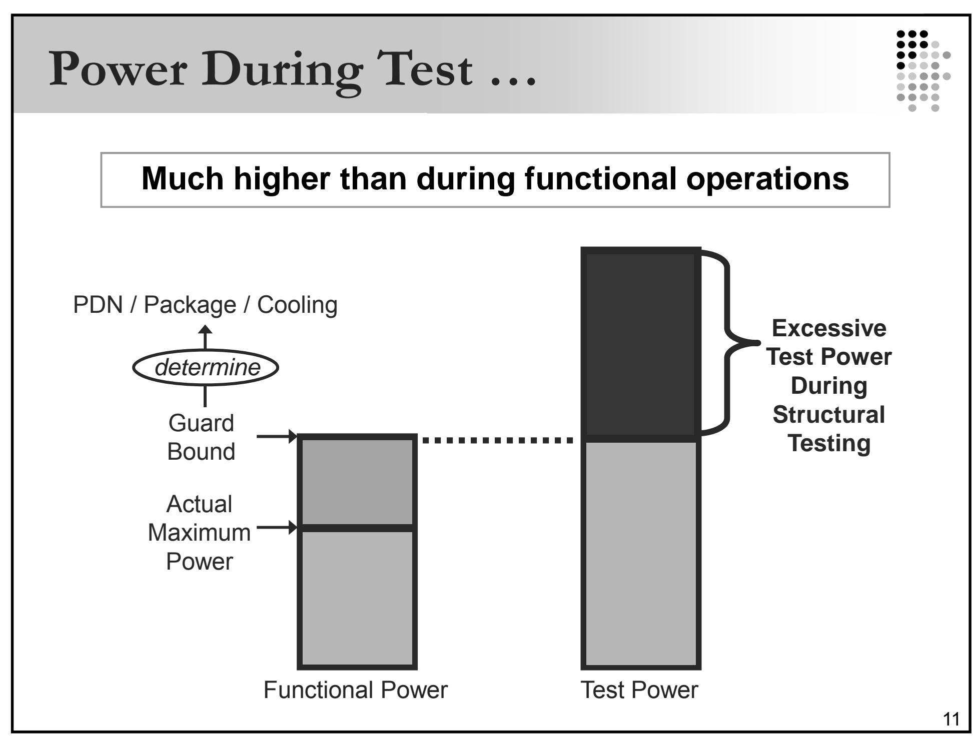
Leakage (static) Power

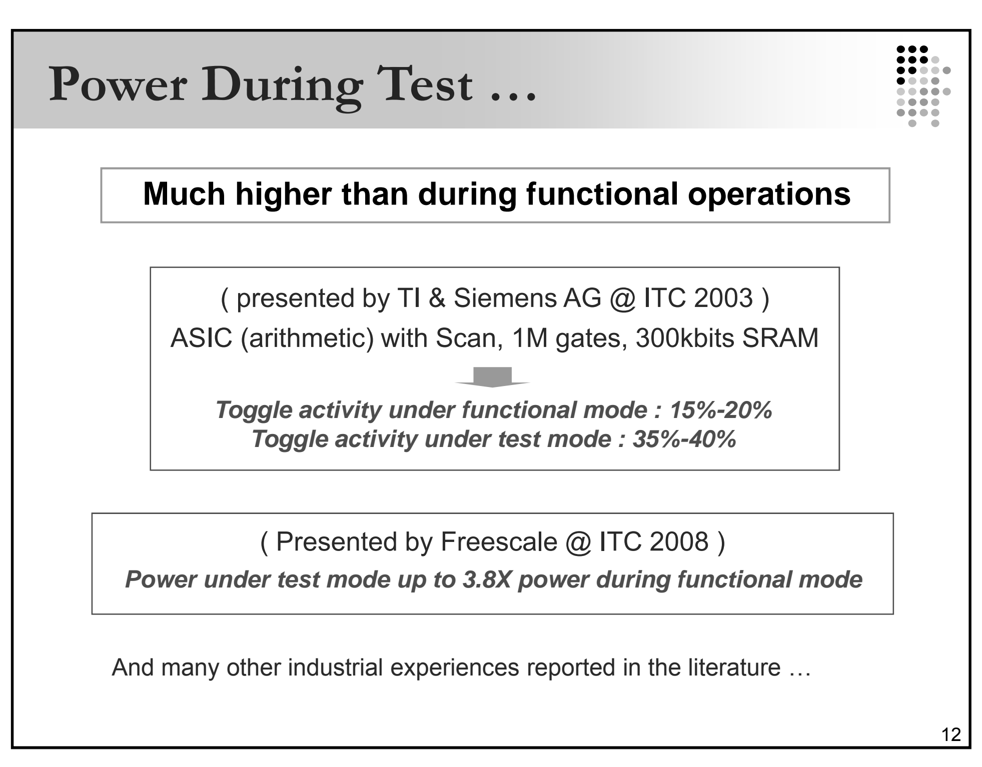
- Power consumed when the circuit is idle
- Mainly due to sub-threshold leakage
- $I_{SUB} \propto V_{DD} / V_{TH}$



Short-circuit (dynamic) power due to direct current path from VDD to GND during output switching is considered as negligible

10


Power During Test …
Much higher than during functional operations
PDN / Package / Cooling
determine
Guard Bound
Actual Maximum Power
Excessive Test Power During Structural Testing
Functional Power
Test Power
11


Power During Test …
Much higher than during functional operations
(presented by TI & Siemens AG @ ITC 2003)
ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM
Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%
(Presented by Freescale @ ITC 2008)
Power under test mode up to 3.8X power during functional mode
And many other industrial experiences reported in the literature …
12

Power During Test …

Main reasons for excessive test power

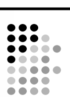
- Conflict of objectives between test and functional mode
- No correlation between consecutive test vectors
- Non-functional clocking during test (e.g. LOC or LOS)
- DFT (e.g. scan) circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction

For conventional (non low-power) designs, dynamic power is the main responsible for excessive test power !!

Leakage power is a real issue during IDDQ test (reduced sensitivity) and during burn-in test (can result in thermal runaway condition and yield loss)

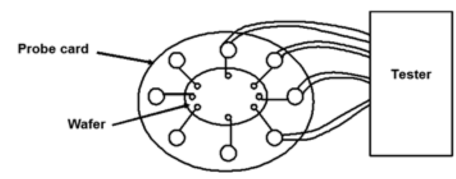
13

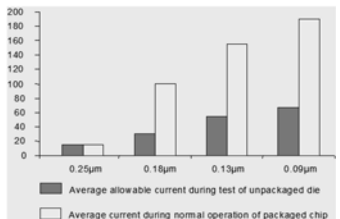
Power During Test …



Power availability and quality may be limited

- During wafer sort test, all power pins may not be connected to the Tester Power Supply (TPS), resulting in reduced power availability



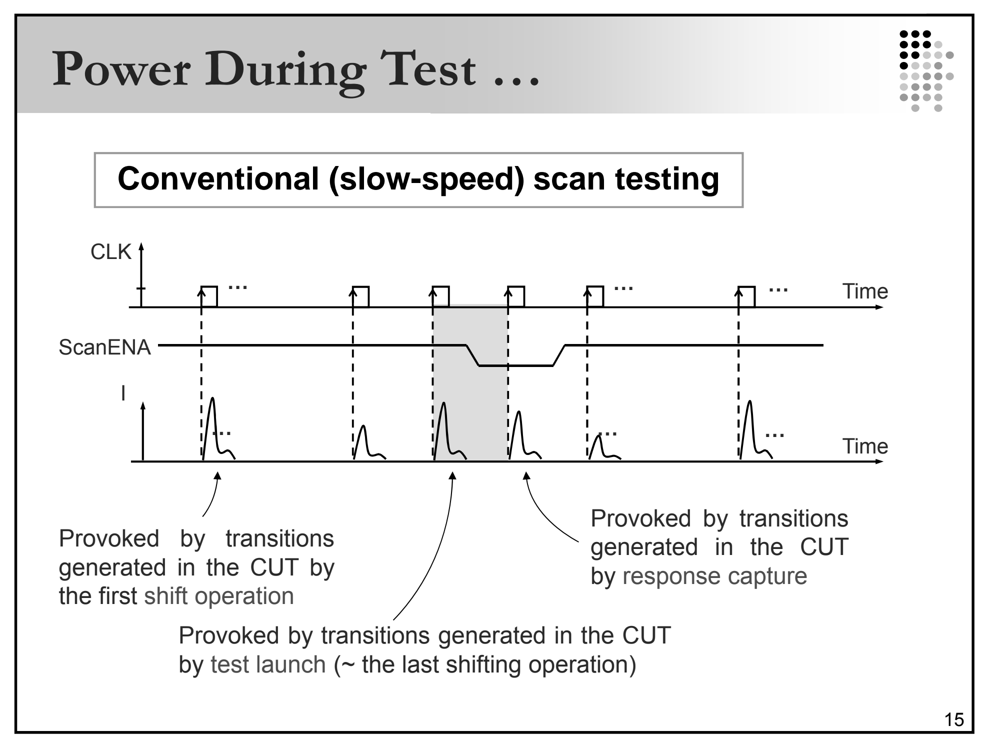


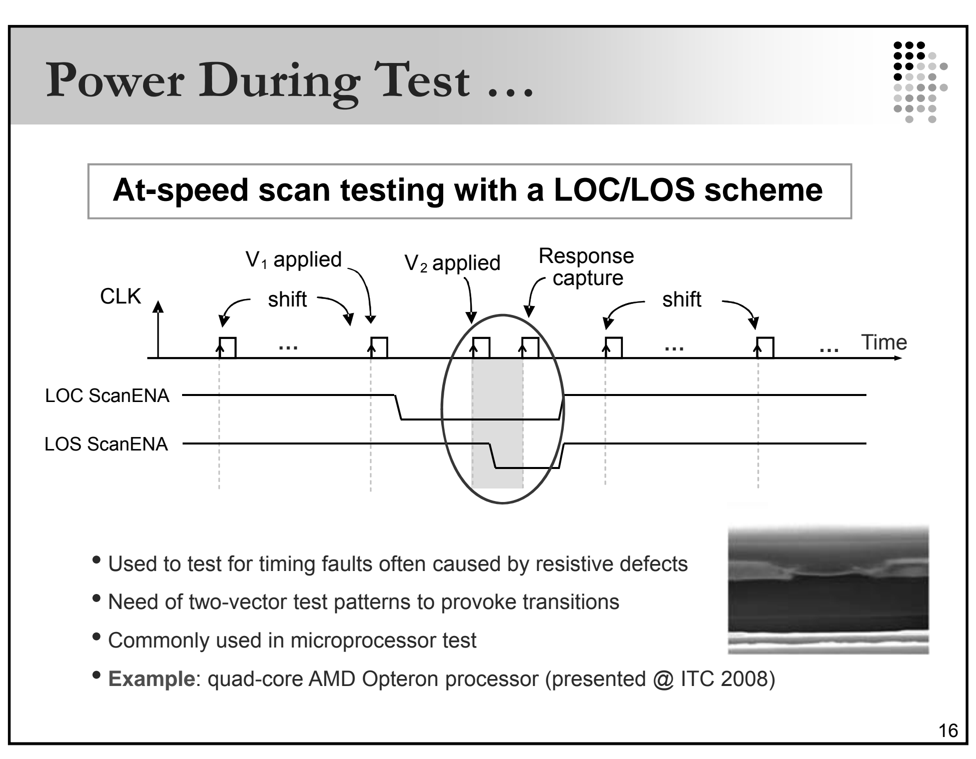
(Kundu et al. 2004)

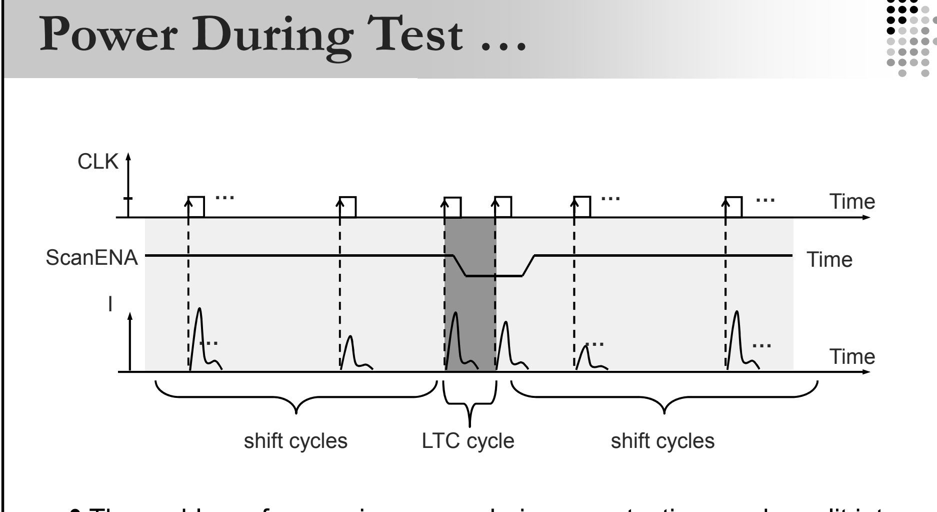
- Current limiters placed on TPS to prevent burn-out due to short-circuit current may affect power availability and quality

Wafer sort test targets gross defect (stuck-at fault) coverage

14

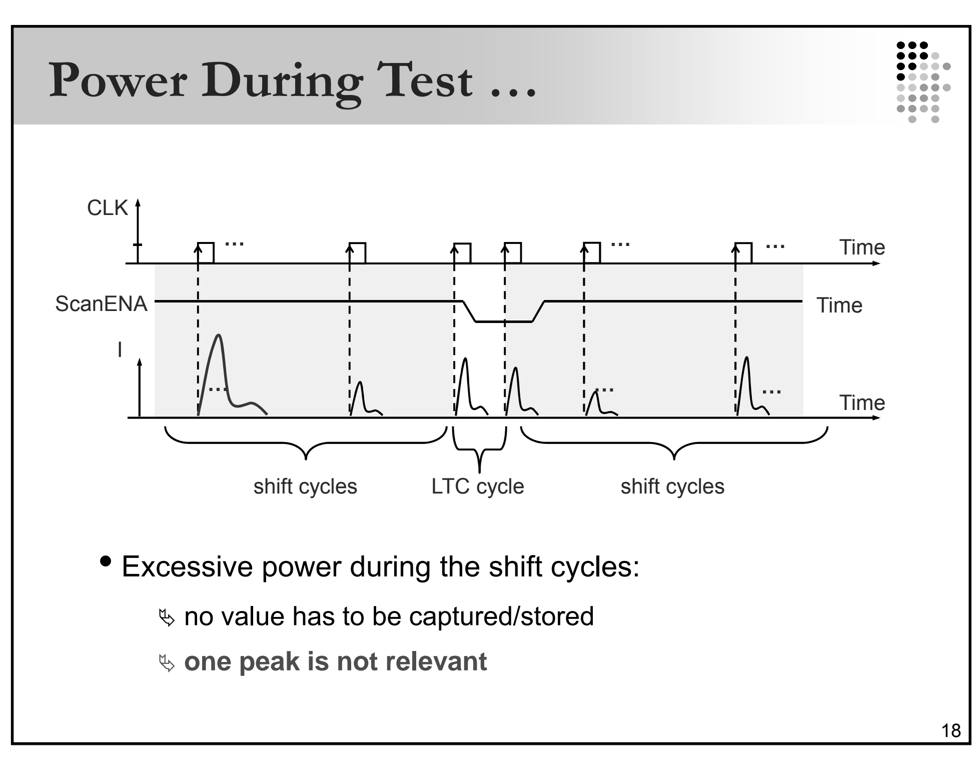

Power During Test …
Conventional (slow-speed) scan testing
CLK
Time
ScanENA
I
Time
Provoked by transitions generated in the CUT by the first shift operation
Provoked by transitions generated in the CUT by test launch (~ the last shifting operation)
Provoked by transitions generated in the CUT by response capture
15

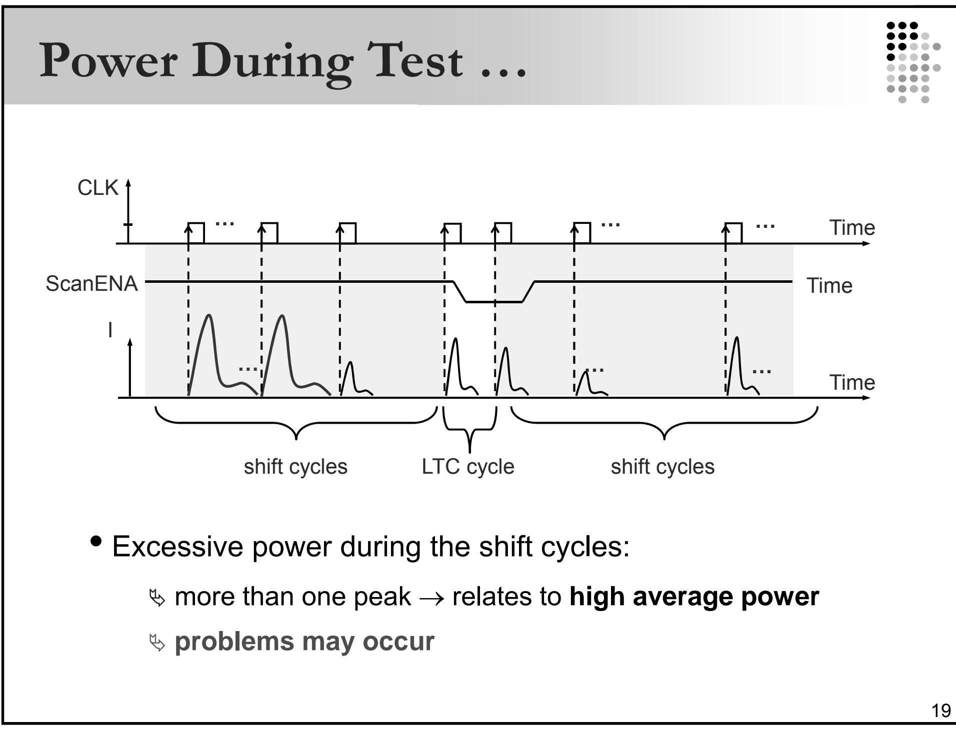

Power During Test …
At-speed scan testing with a LOC/LOS scheme
V1 applied
V2 applied
Response capture
shift
shift
CLK
Time
LOC ScanENA
LOS ScanENA
Used to test for timing faults often caused by resistive defects
Need of two-vector test patterns to provoke transitions
Commonly used in microprocessor test
Example: quad-core AMD Opteron processor (presented @ ITC 2008)
16

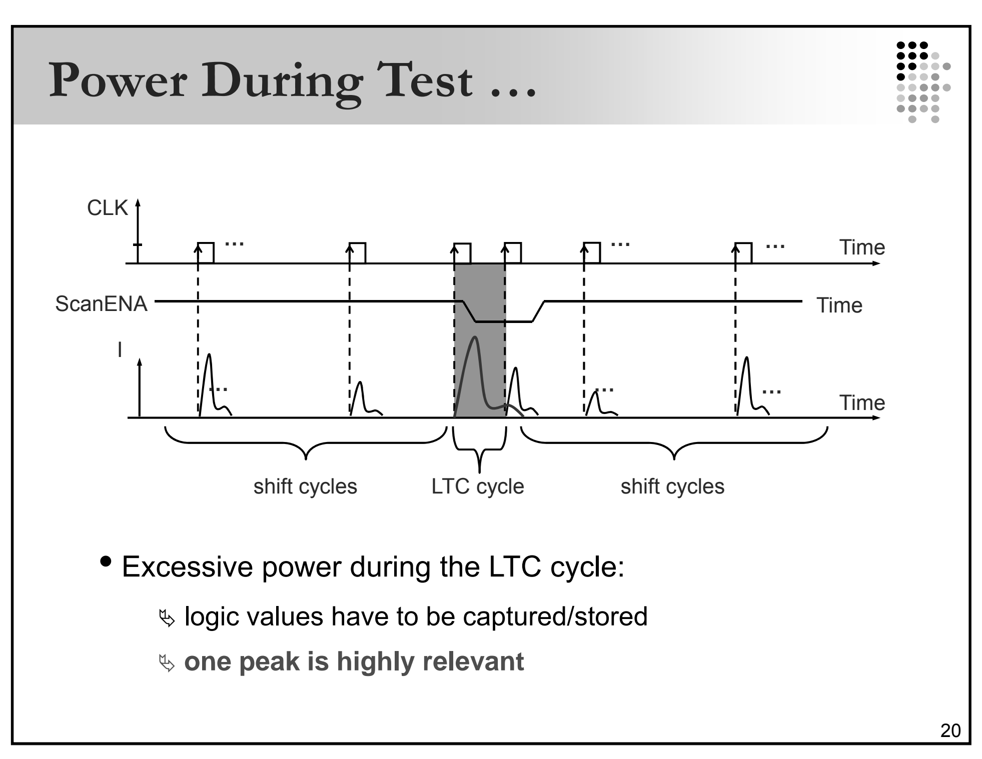


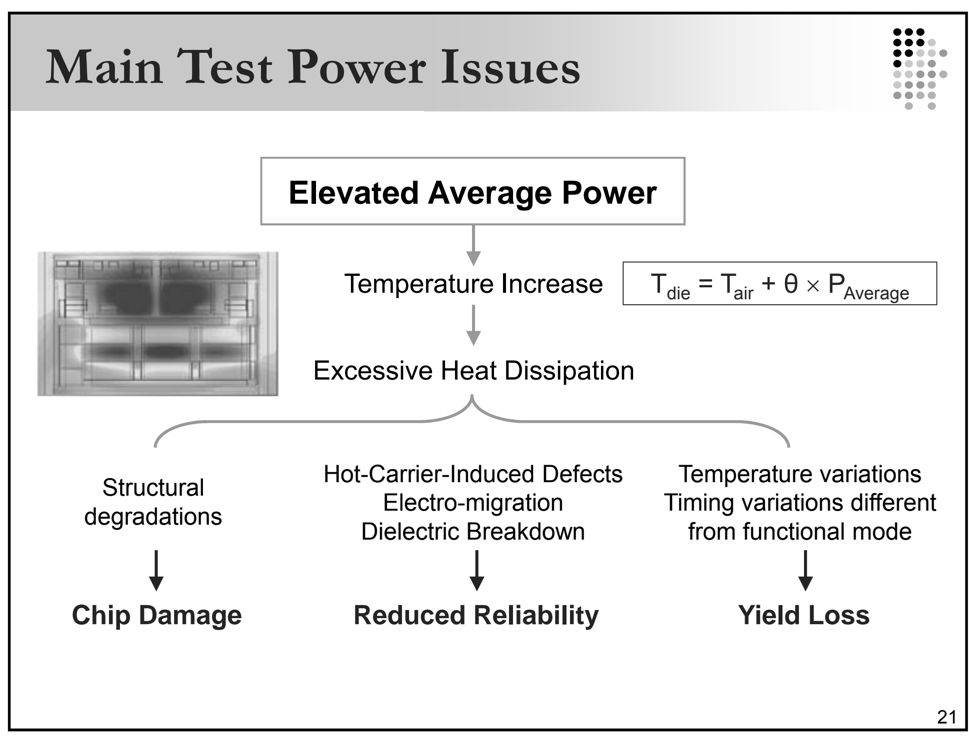
- The problem of excessive power during scan testing can be split into two sub-problems: excessive power during the shift cycles and excessive power during the Launch-To-Capture (LTC) cycle

17

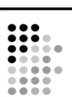


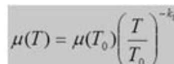

Power During Test …
CLK
Time
ScanENA
Time
I
Time
shift cycles
LTC cycle
shift cycles
• Excessive power during the shift cycles:
more than one peak → relates to high average power
problems may occur
19

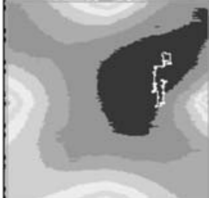

Power During Test …
CLK
Time
ScanENA
Time
I
Time
shift cycles
LTC cycle
shift cycles
• Excessive power during the LTC cycle:
logic values have to be captured/stored
one peak is highly relevant
20



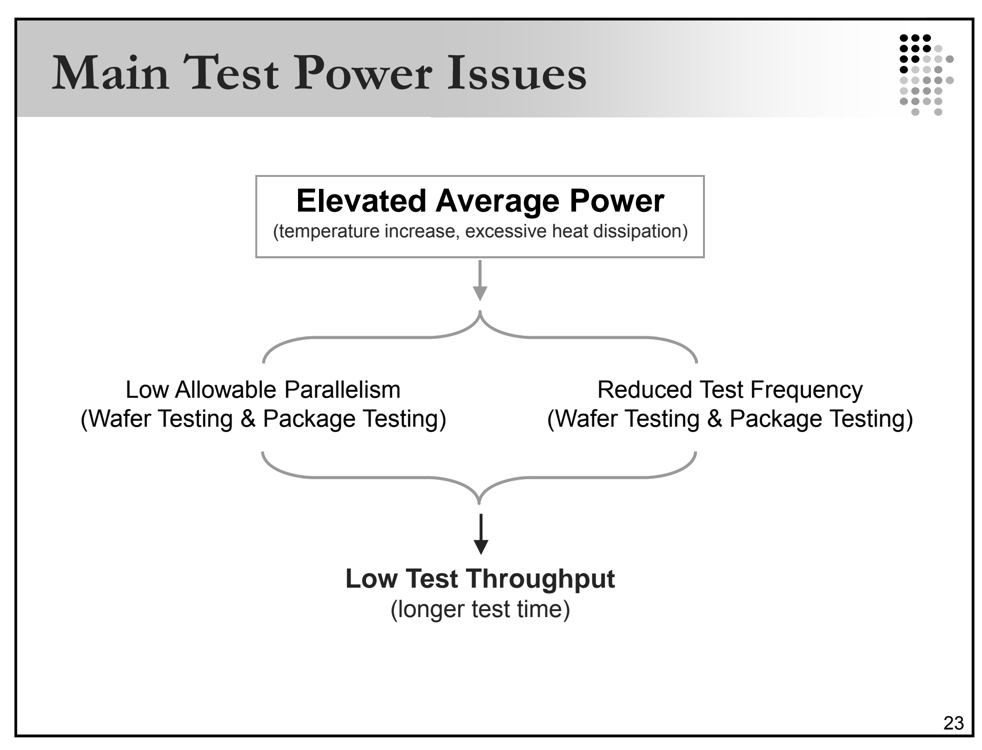
Main Test Power Issues

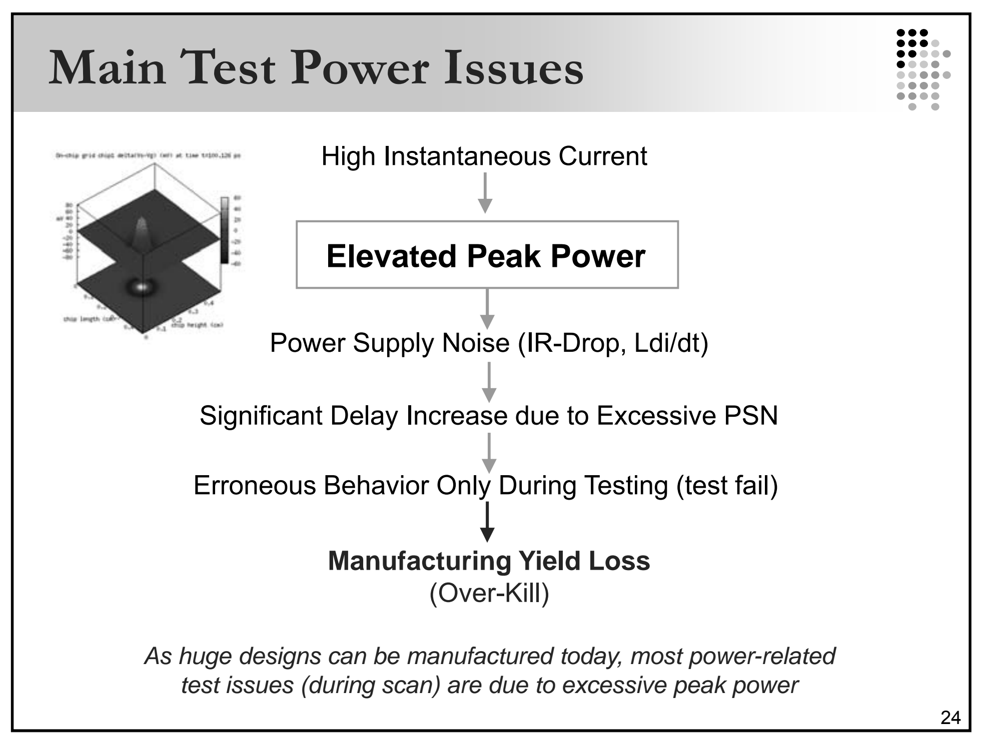


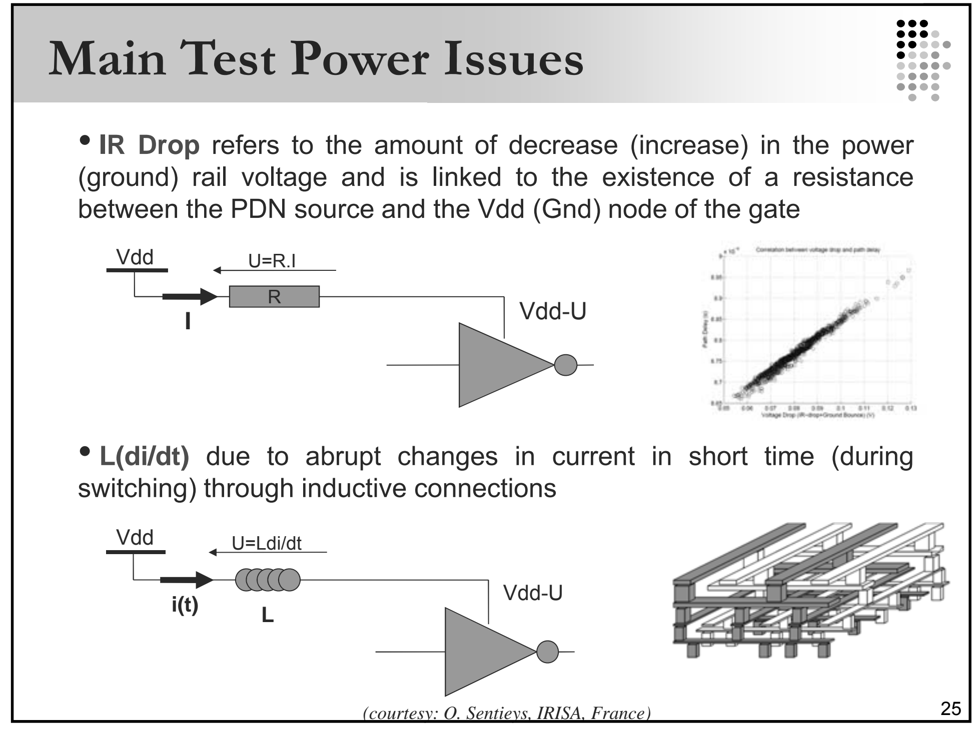
- **Thermal hot-spot** results from localized overheating due to non-uniform spatial on-die power distribution
- Thermal hot-spot are likely to increase during package testing since test power dissipation can be high
- Main impact on the carrier's mobility  $\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-k_1}$
- Slow down the device in the thermal hot-spot affected region of the chip
- Increase gate delays → yield loss
- Structural degradation → permanent damage !

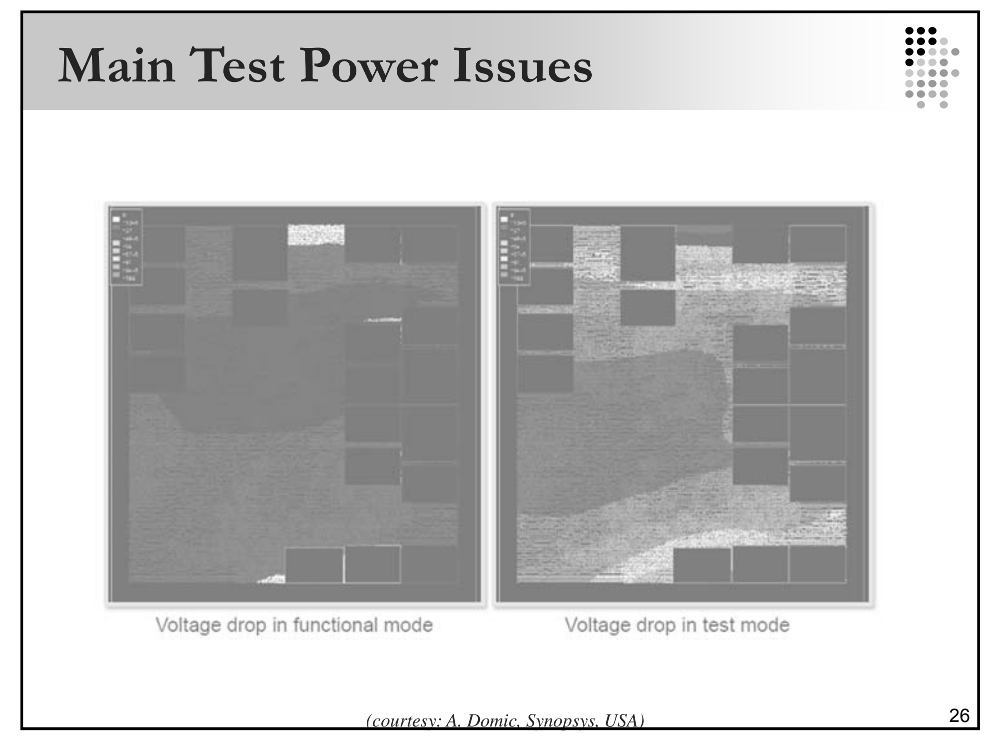


22

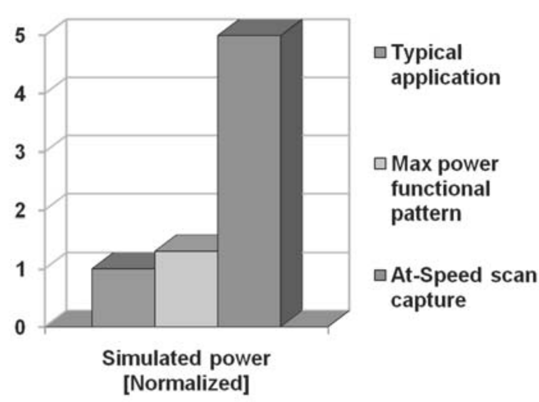

Main Test Power Issues
Elevated Average Power
(temperature increase, excessive heat dissipation)
Low Allowable Parallelism
(Wafer Testing & Package Testing)
Reduced Test Frequency
(Wafer Testing & Package Testing)
Low Test Throughput
(longer test time)
23


Main Test Power Issues
High Instantaneous Current
Elevated Peak Power
Power Supply Noise (IR-Drop, Ldi/dt)
Significant Delay Increase due to Excessive PSN
Erroneous Behavior Only During Testing (test fail)
Manufacturing Yield Loss
(Over-Kill)
As huge designs can be manufactured today, most power-related
test issues (during scan) are due to excessive peak power
24


Main Test Power Issues
• IR Drop refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a resistance between the PDN source and the Vdd (Gnd) node of the gate
Vdd
U=R.I
R
I
Vdd-U
• L(di/dt) due to abrupt changes in current in short time (during switching) through inductive connections
Vdd
U=Ldi/dt
i(t)
L
Vdd-U
(courtesy: O. Sentieys, IRISA, France)
25


Main Test Power Issues
Voltage drop in functional mode
Voltage drop in test mode
(courtesy: A. Domic, Synopsys, USA)
26

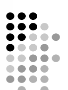
Main Test Power Issues



- Voltage drop: the main suspect for increased delay during capture
- Presented by Freescale @ ITC 2008

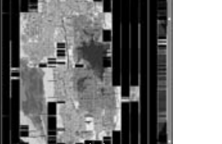
27

Main Test Power Issues



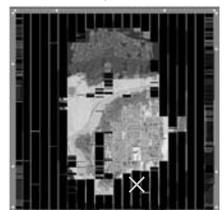
- Local IR-drop can be an issue even though total test power is reduced

activate all modules



peak: 1.2V ® 1.026V
(176mV(14.5%) drop)

activate only one module

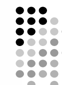


peak: 1.2V ® 1.029V
(171mV(14.3%) drop)

(courtesy: K. Hatayama, STARC, Japan)

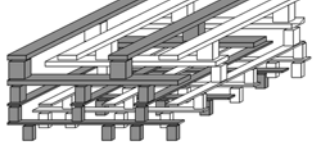
28

Reducing Test Power



Straightforward Solutions

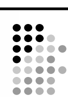
- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing power distribution network (PDN)
  - Grid Sizing based on functional power requirements
    - all parts not active at a time
  - Grid Sizing for test purpose too expensive !!



Costly or longer test time

29

Reducing Test Power



Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

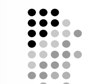
Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

30

Reducing Test Power



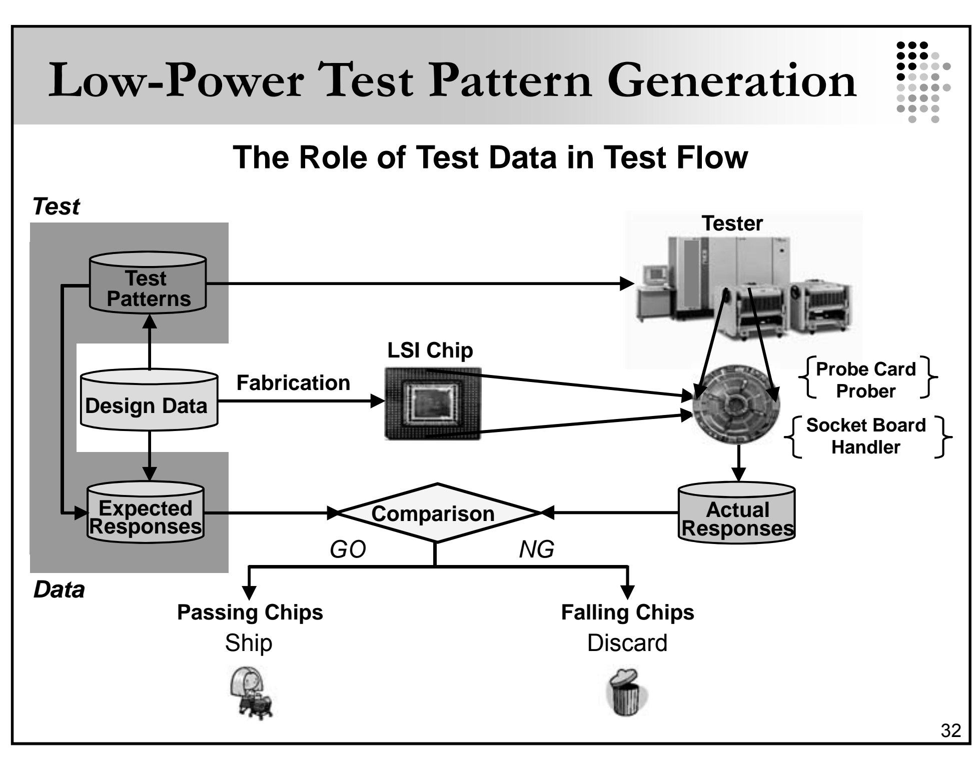
Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

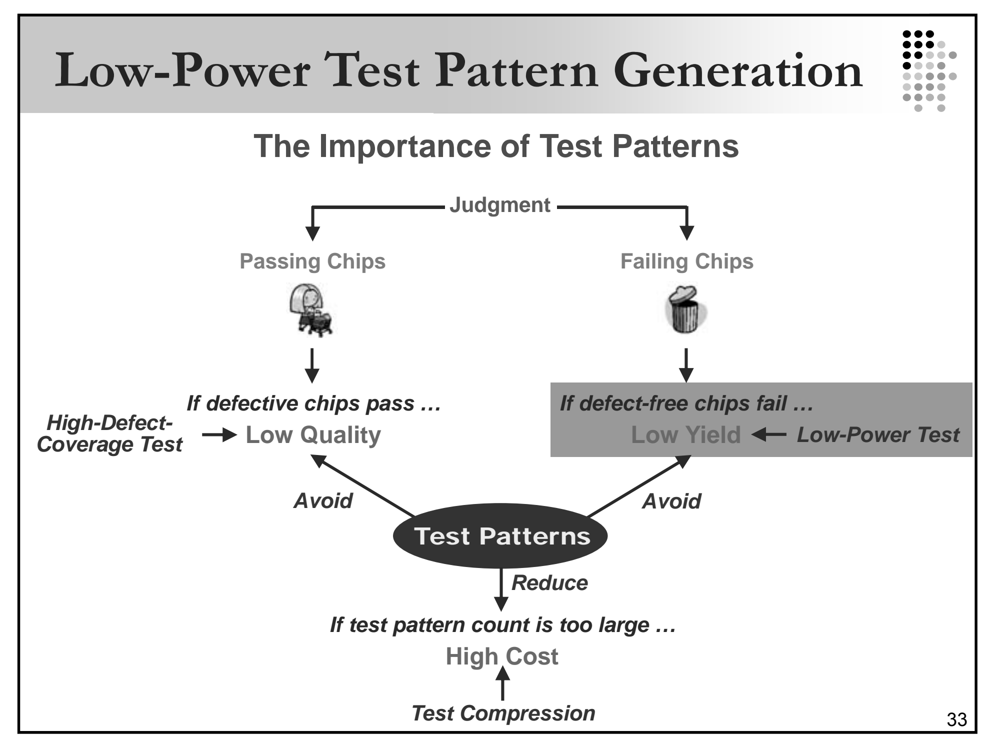
31

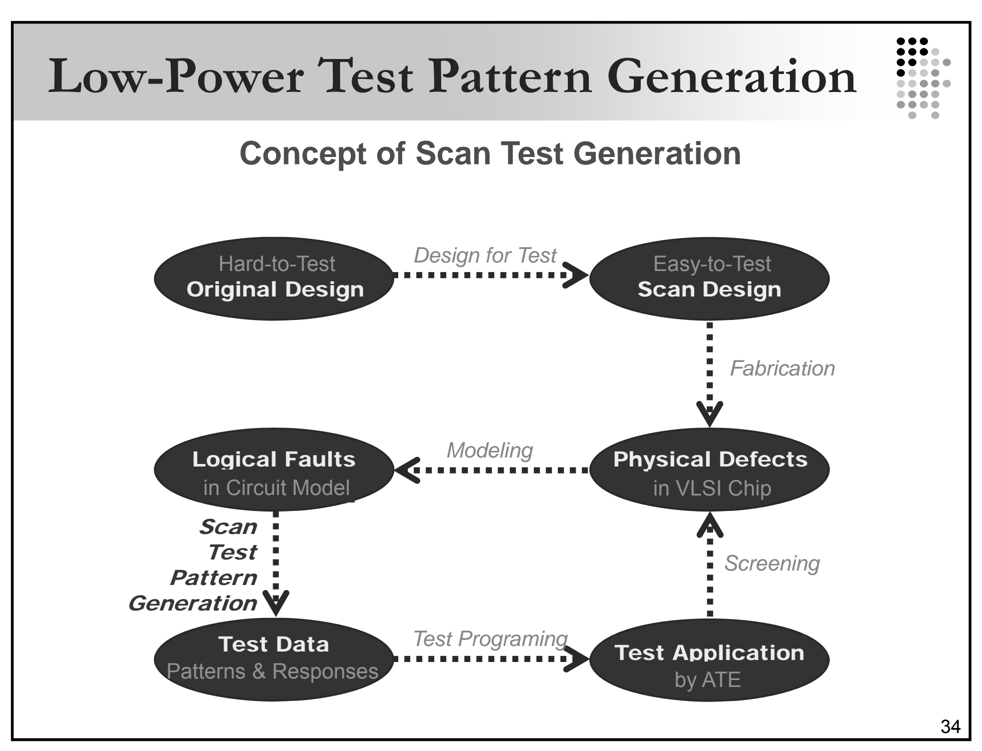
Low-Power Test Pattern Generation

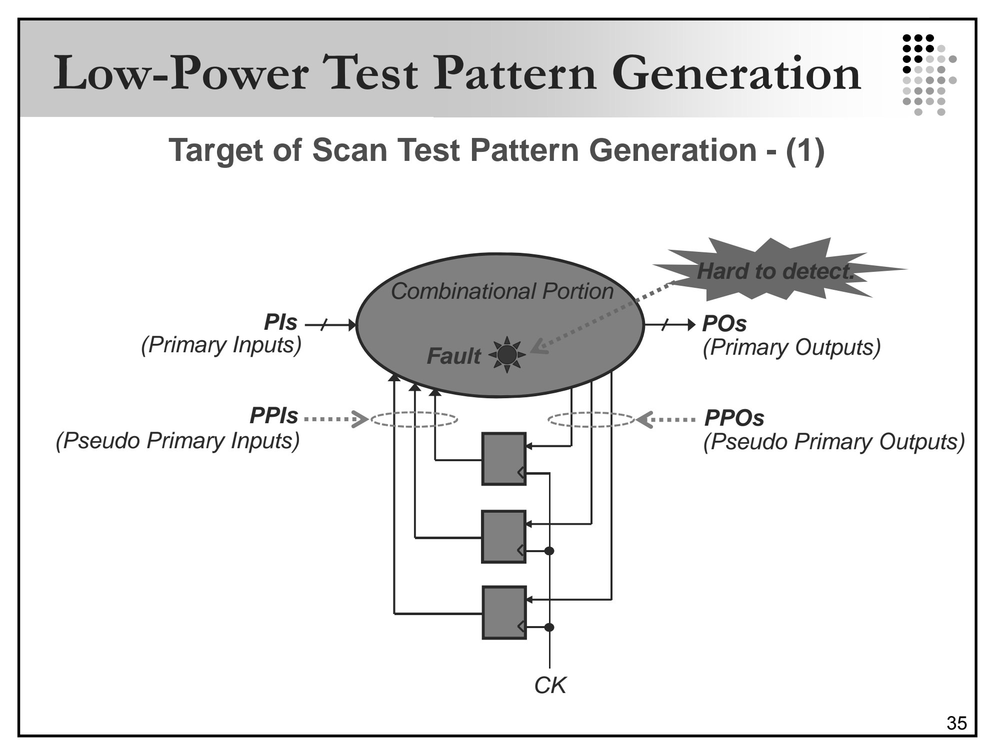
The Role of Test Data in Test Flow

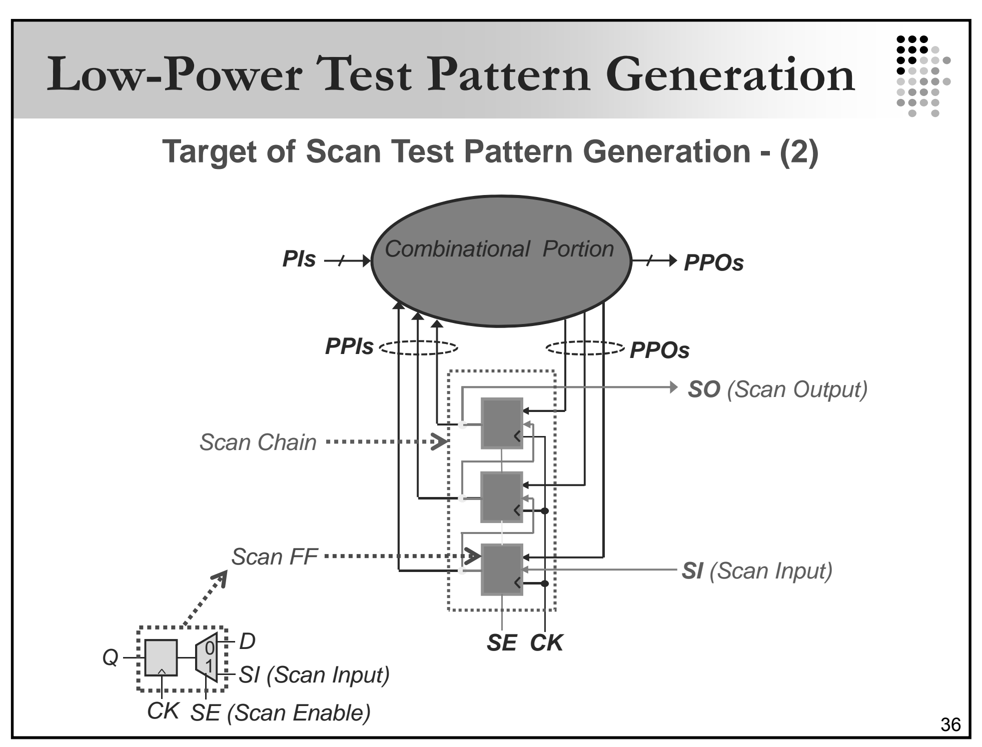


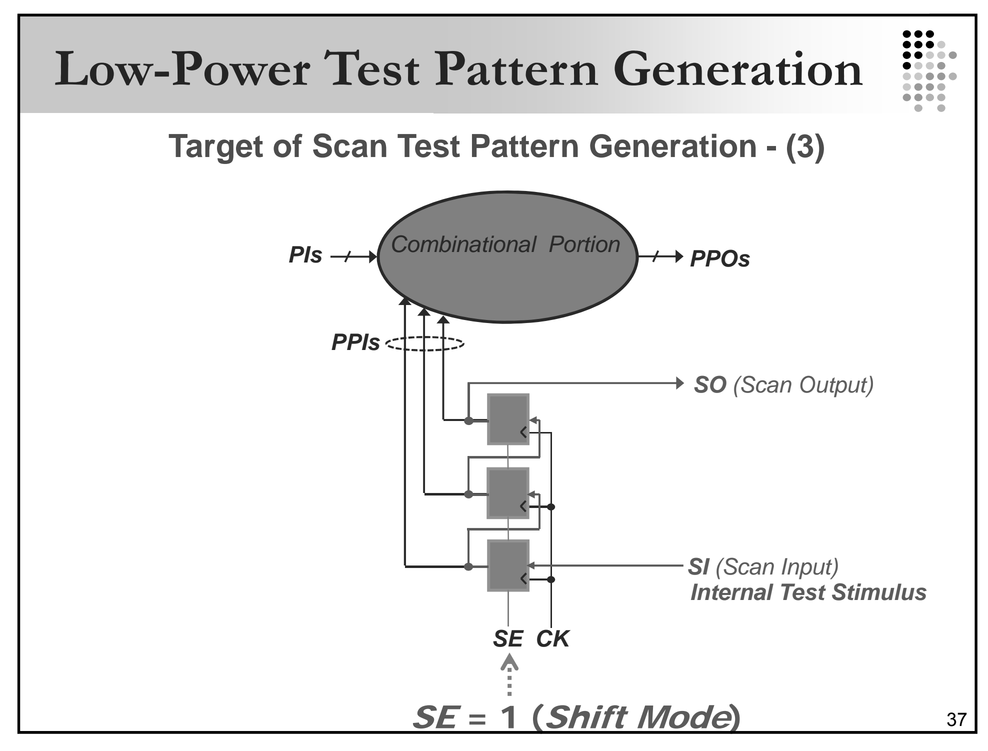
32

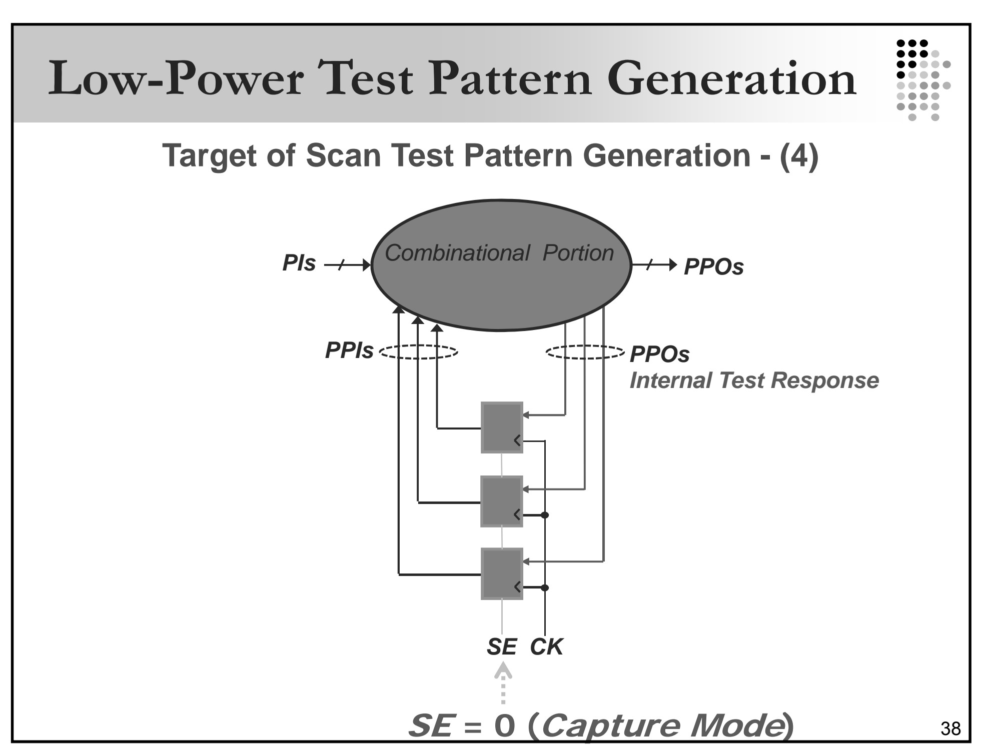

Low-Power Test Pattern Generation
The Importance of Test Patterns
Judgment
Passing Chips
Failing Chips
If defective chips pass …
High-Defect-
Coverage Test
Low Quality
If defect-free chips fail …
Low Yield
Low-Power Test
Avoid
Avoid
Test Patterns
Reduce
If test pattern count is too large …
High Cost
Test Compression
33

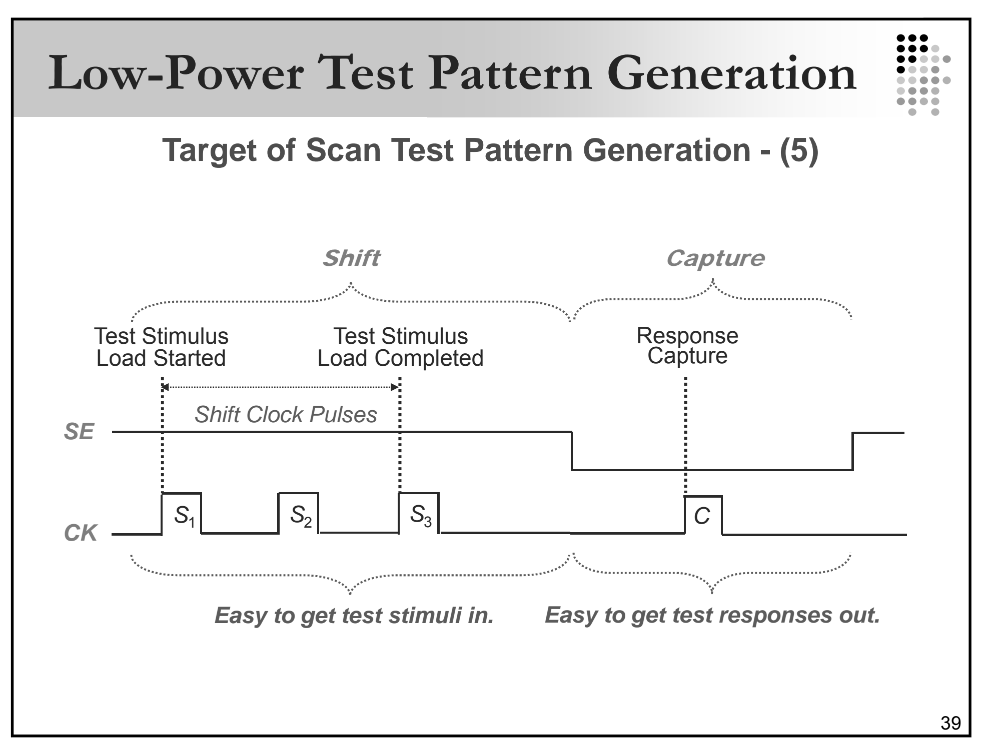

Low-Power Test Pattern Generation
Concept of Scan Test Generation
Hard-to-Test
Original Design
Design for Test
Easy-to-Test
Scan Design
Fabrication
Logical Faults
in Circuit Model
Modeling
Physical Defects
in VLSI Chip
Scan
Test
Pattern
Generation
Screening
Test Data
Patterns & Responses
Test Programing
Test Application
by ATE
34

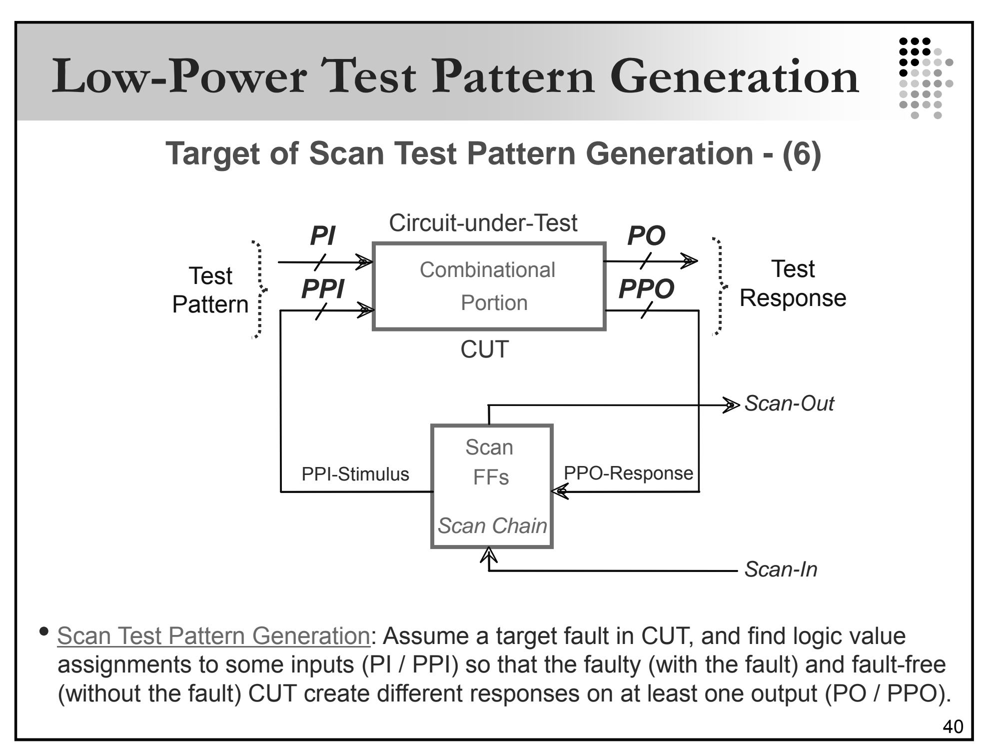

Low-Power Test Pattern Generation
Target of Scan Test Pattern Generation - (1)
Hard to detect.
Combinational Portion
PIs
(Primary Inputs)
Fault
POs
(Primary Outputs)
PPIs
(Pseudo Primary Inputs)
PPOs
(Pseudo Primary Outputs)
CK
35

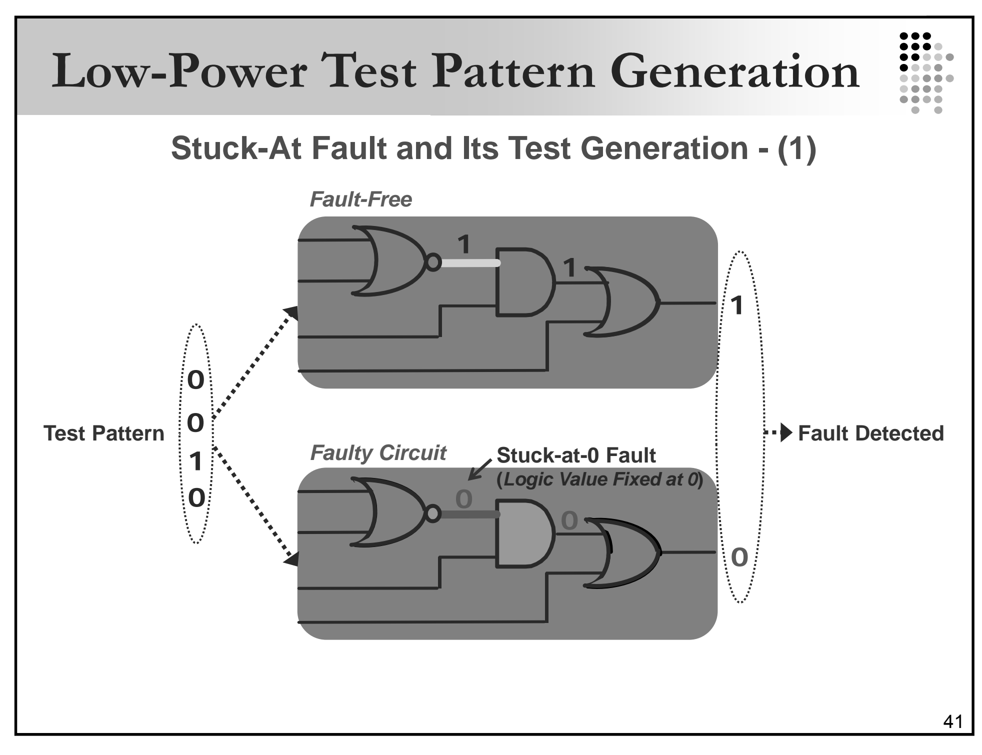

Low-Power Test Pattern Generation
Target of Scan Test Pattern Generation - (2)
Combinational Portion
PIs
PPOs
PPIs
PPOs
SO (Scan Output)
Scan Chain
Scan FF
SI (Scan Input)
SE CK
Q
D
SI (Scan Input)
CK
SE (Scan Enable)
36

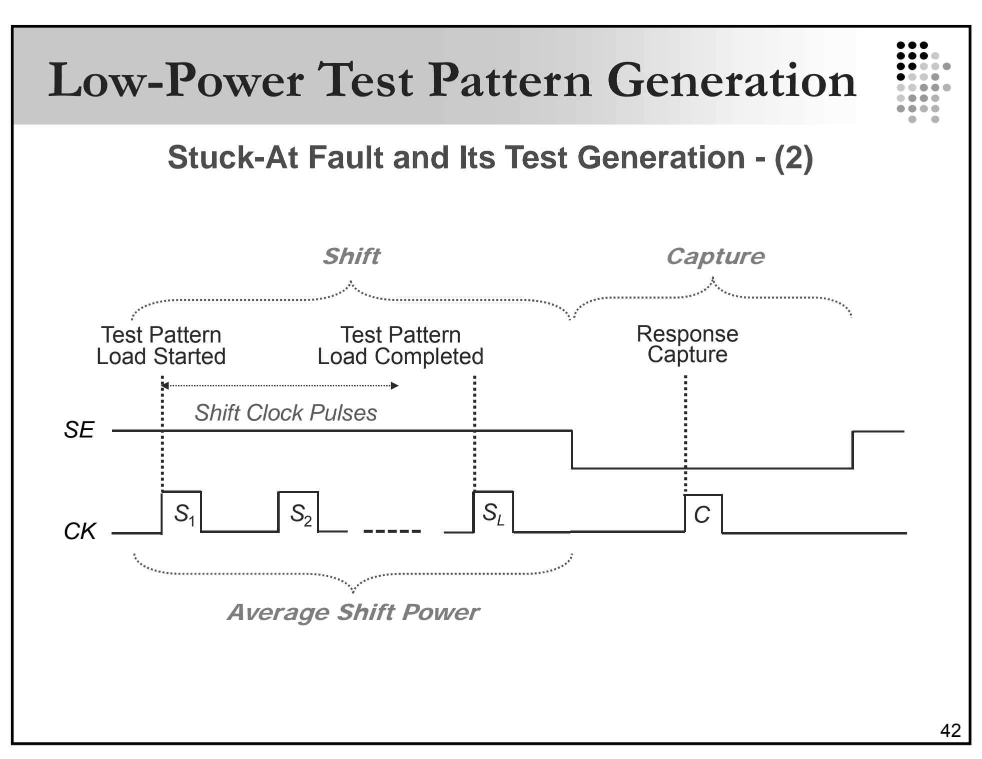

Low-Power Test Pattern Generation
Target of Scan Test Pattern Generation - (3)
PIs
Combinational Portion
PPOs
PPIs
SO (Scan Output)
SI (Scan Input)
Internal Test Stimulus
SE CK
SE = 1 (Shift Mode)
37

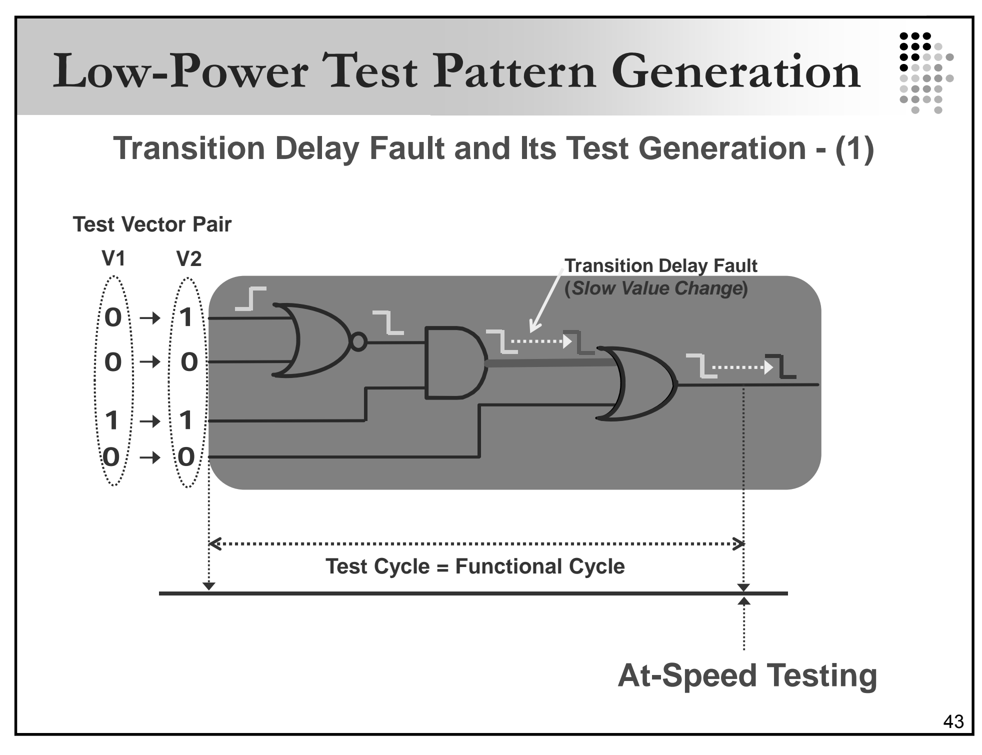

Low-Power Test Pattern Generation
Target of Scan Test Pattern Generation - (4)
PIs
Combinational Portion
PPOs
PPIs
PPOs
Internal Test Response
SE CK
SE = 0 (Capture Mode)
38

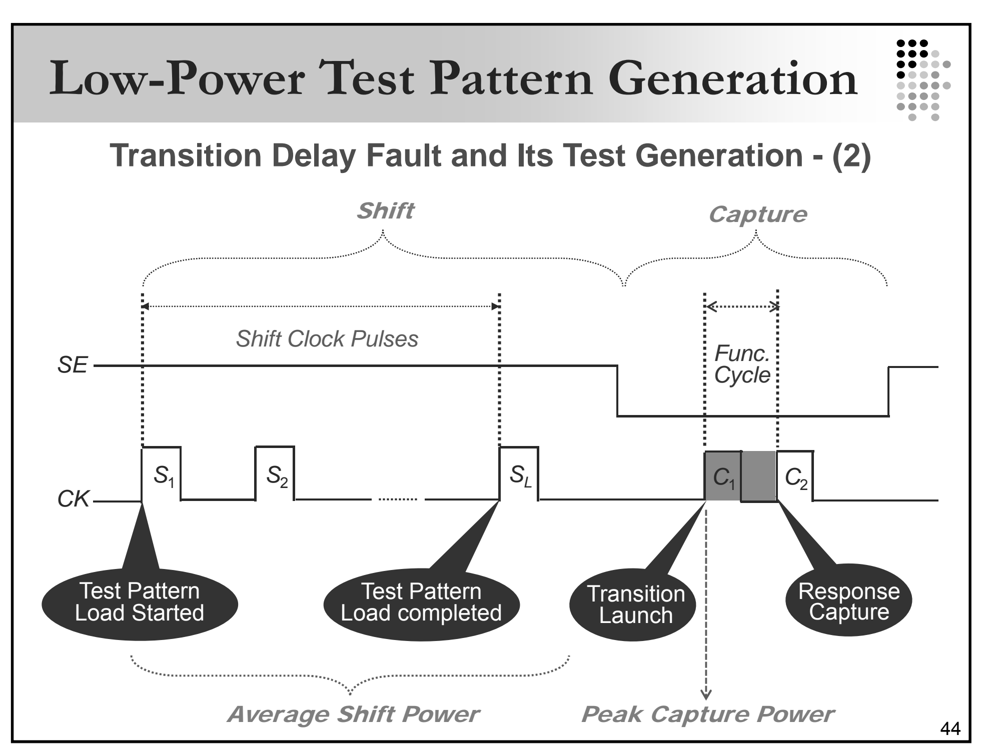

Low-Power Test Pattern Generation
Target of Scan Test Pattern Generation - (5)
Shift
Capture
Test Stimulus Load Started
Test Stimulus Load Completed
Response Capture
Shift Clock Pulses
SE
CK
S1
S2
S3
C
Easy to get test stimuli in.
Easy to get test responses out.
39


Low-Power Test Pattern Generation
Target of Scan Test Pattern Generation - (6)
Circuit-under-Test
PI
PO
PPI
PPO
Test Pattern
Test Response
Combinational Portion
CUT
Scan-Out
Scan FFs
Scan Chain
PPI-Stimulus
PPO-Response
Scan-In
• Scan Test Pattern Generation: Assume a target fault in CUT, and find logic value assignments to some inputs (PI / PPI) so that the faulty (with the fault) and fault-free (without the fault) CUT create different responses on at least one output (PO / PPO).
40

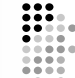

Low-Power Test Pattern Generation
Stuck-At Fault and Its Test Generation - (1)
Fault-Free
1
1
1
Test Pattern
0
0
1
0
Fault Detected
Faulty Circuit
Stuck-at-0 Fault
(Logic Value Fixed at 0)
0
0
0
41


Low-Power Test Pattern Generation
Stuck-At Fault and Its Test Generation - (2)
Shift
Capture
Test Pattern Load Started
Test Pattern Load Completed
Response Capture
Shift Clock Pulses
SE
CK
S1
S2
SL
C
Average Shift Power
42

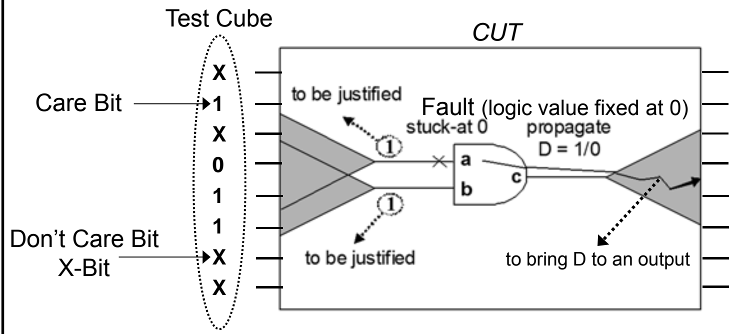

Low-Power Test Pattern Generation
Transition Delay Fault and Its Test Generation - (1)
Test Vector Pair
V1
V2
0 → 1
0 → 0
1 → 1
0 → 0
Transition Delay Fault
(Slow Value Change)
Test Cycle = Functional Cycle
At-Speed Testing
43


Low-Power Test Pattern Generation
Transition Delay Fault and Its Test Generation - (2)
Shift
Capture
Shift Clock Pulses
Func.
Cycle
SE
CK
S1
S2
SL
C1
C2
Test Pattern
Load Started
Test Pattern
Load completed
Transition
Launch
Response
Capture
Average Shift Power
Peak Capture Power
44

Low-Power Test Pattern Generation



Automatic Test Pattern Generation (ATPG)



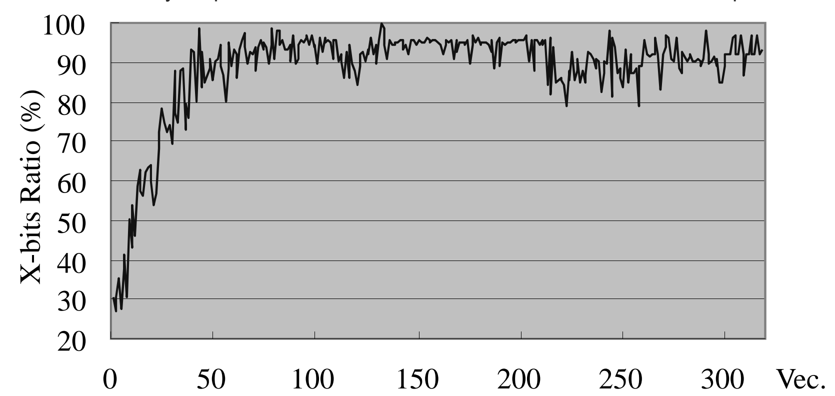
- ATPG is based on complex algorithms and is used to determine logic values for input bits in order to detect a fault in the given CUT.
- Not all input bits need to be assigned with logic values in order to detect a fault.
- The immediate result of ATPG is a test cube, which contains both specified bits (care bits) and unspecified bits (don't care bits or X-bits).

45

Low-Power Test Pattern Generation

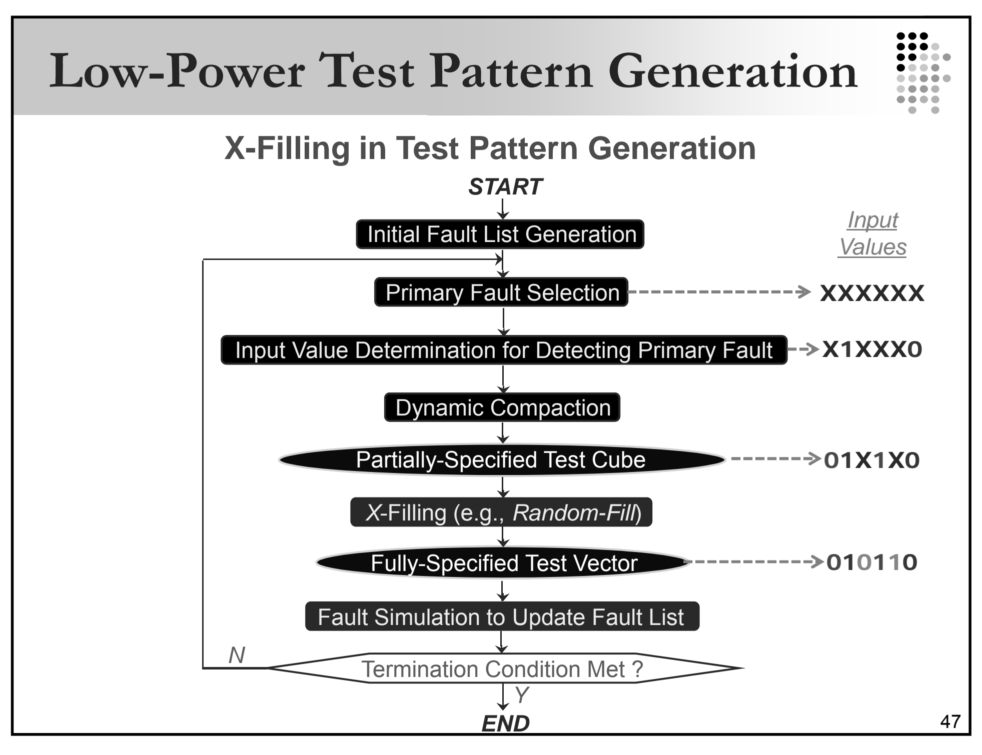
X-Bits in Test Cubes

(Block in an Industry Chip: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)



- A large percentage of input bits in a test cube are don't care bits (X-bits).
- Need X-filling (*i.e., assigning logic values to X-bits*) to create a complete test pattern.

46



Low-Power Test Pattern Generation

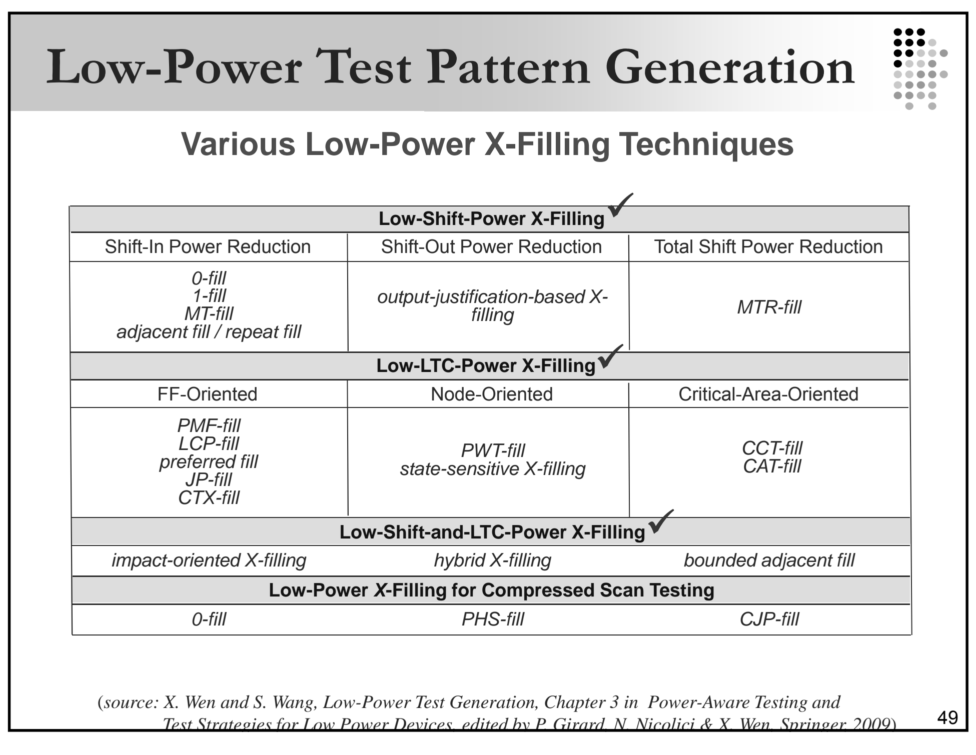
Conventional X-Filling Technique: *Random-Fill*

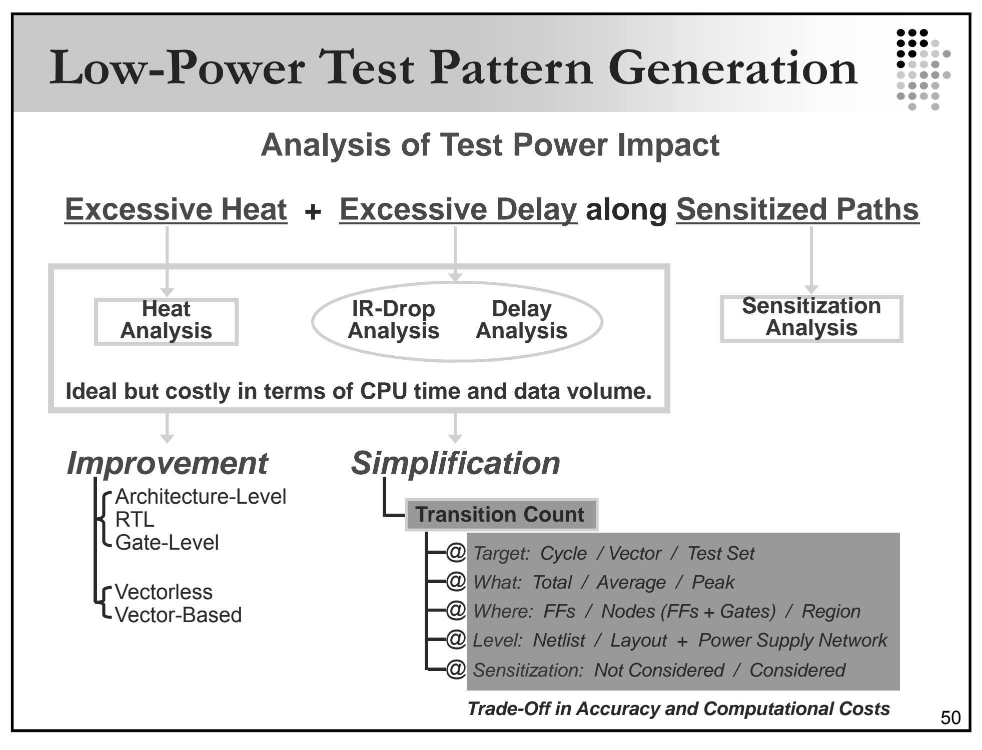
ATPG care bits

Random fill

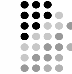
- Conventionally, X-bits in a test cube are filled with random logic values.
- Advantages → *Small test pattern count due to "fortuitous detection"*
- Disadvantage → *High test (shift and LTC) power*

48


Low-Power Test Pattern Generation
Various Low-Power X-Filling Techniques
Low-Shift-Power X-Filling
Shift-In Power Reduction
Shift-Out Power Reduction
Total Shift Power Reduction
0-fill
1-fill
MT-fill
adjacent fill / repeat fill
output-justification-based X-filling
MTR-fill
Low-LTC-Power X-Filling
FF-Oriented
Node-Oriented
Critical-Area-Oriented
PMF-fill
LCP-fill
preferred fill
JP-fill
CTX-fill
PWT-fill
state-sensitive X-filling
CCT-fill
CAT-fill
Low-Shift-and-LTC-Power X-Filling
impact-oriented X-filling
hybrid X-filling
bounded adjacent fill
Low-Power X-Filling for Compressed Scan Testing
0-fill
PHS-fill
CJP-fill
(source: X. Wen and S. Wang, Low-Power Test Generation, Chapter 3 in Power-Aware Testing and Test Strategies for Low Power Devices, edited by P. Girard, N. Nicolici & X. Wen, Springer, 2009)
49

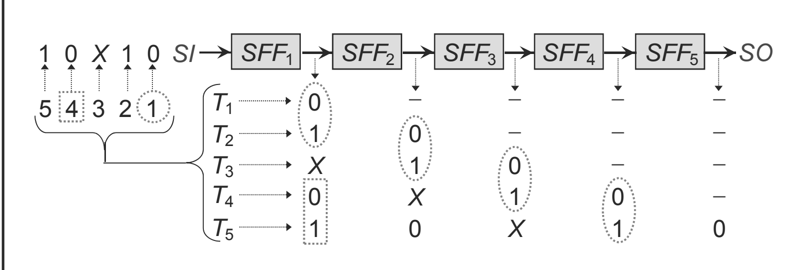

Low-Power Test Pattern Generation
Analysis of Test Power Impact
Excessive Heat + Excessive Delay along Sensitized Paths
Heat Analysis
IR-Drop Analysis
Delay Analysis
Sensitization Analysis
Ideal but costly in terms of CPU time and data volume.
Improvement
Architecture-Level
RTL
Gate-Level
Vectorless
Vector-Based
Simplification
Transition Count
@ Target: Cycle / Vector / Test Set
@ What: Total / Average / Peak
@ Where: FFs / Nodes (FFs + Gates) / Region
@ Level: Netlist / Layout + Power Supply Network
@ Sensitization: Not Considered / Considered
Trade-Off in Accuracy and Computational Costs
50

Low-Power Test Pattern Generation



Typical Metric for Shift Power Analysis

Weighted Transition



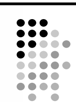
Weighted_Transitions = Σ (*Scan_Chain_Length* – *Transition_Position*)

- Transitions closer to *SI* in a test vector cause more transitions in a scan chain.
- This metric has a good correlation with the total switching activity in a circuit.

(source: R. Sankaralingam et al., Proc. VTS, pp. 35-40, 2000)

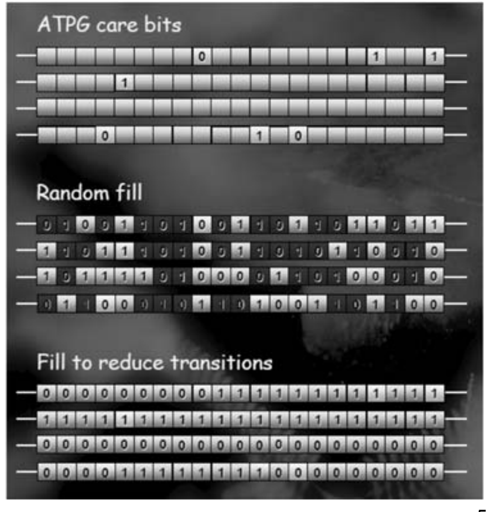
51

Low-Power Test Pattern Generation

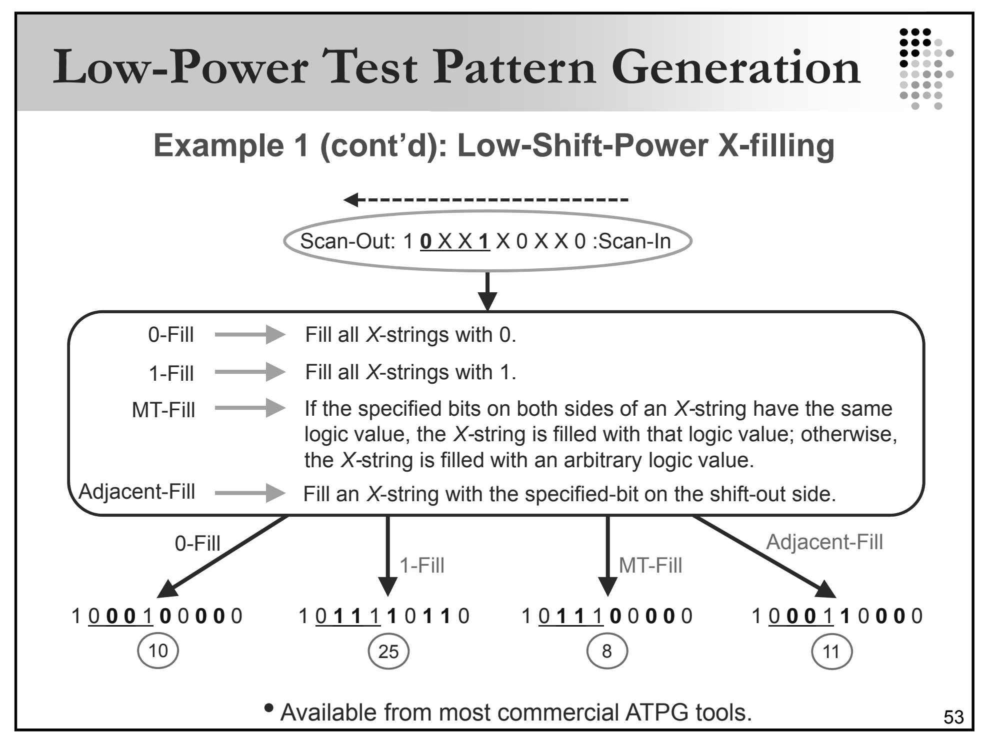


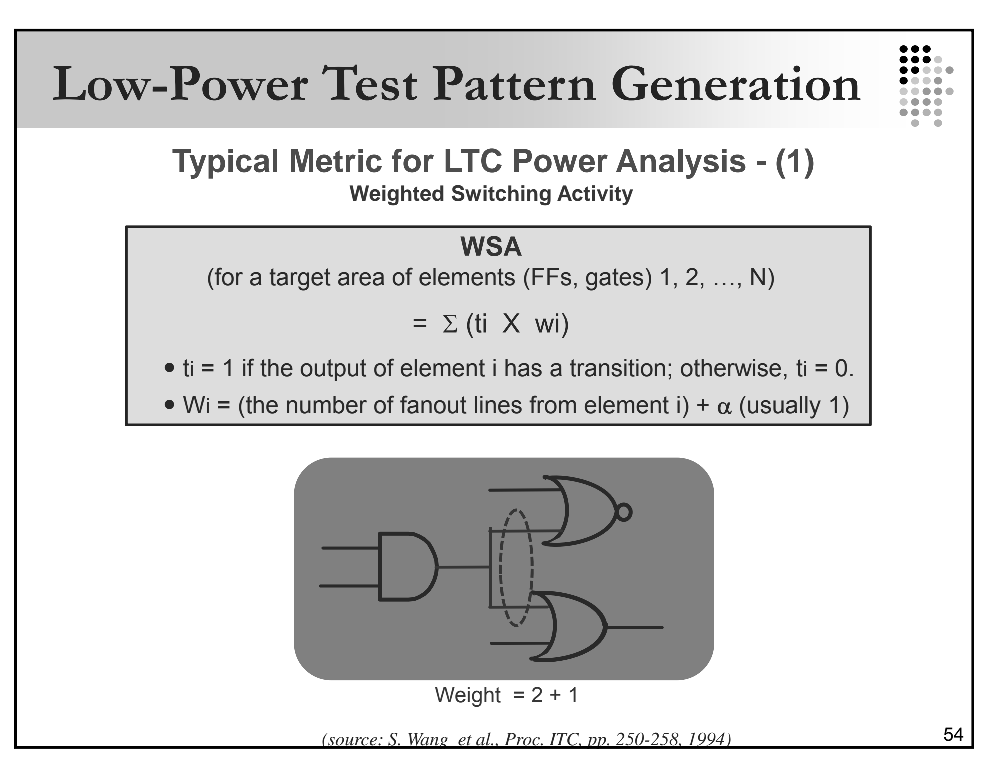
Example 1: Low-Shift-Power X-filling

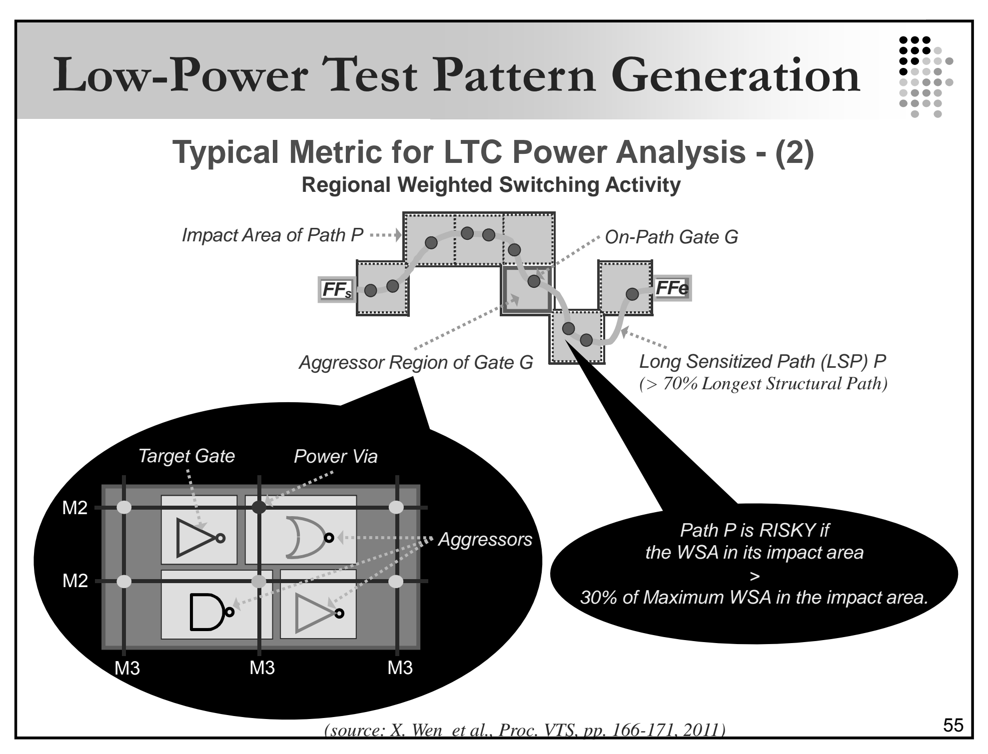
- **Goal**: To assign proper logic values to don't care bits (X-bits) in a test cube so as to reduce transitions in scan chains (and thus also in the combinational logic).
- Popular techniques include ***0-fill***, ***1-fill***, ***MT-fill***, and ***adjacent-fill***.
- Mostly shift-in power is reduced. Occasionally, shift-out power and LTC power are also reduced, especially by ***0-fill***.
- Reported by TI at ITC 2003.
- No area overhead but may increase test pattern count.

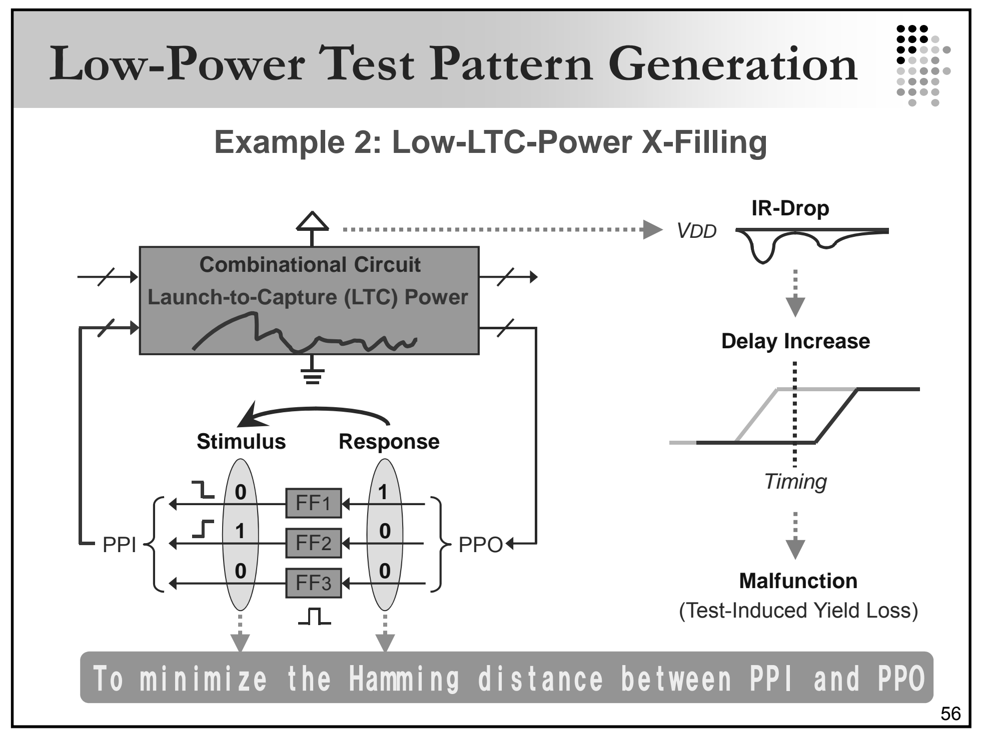


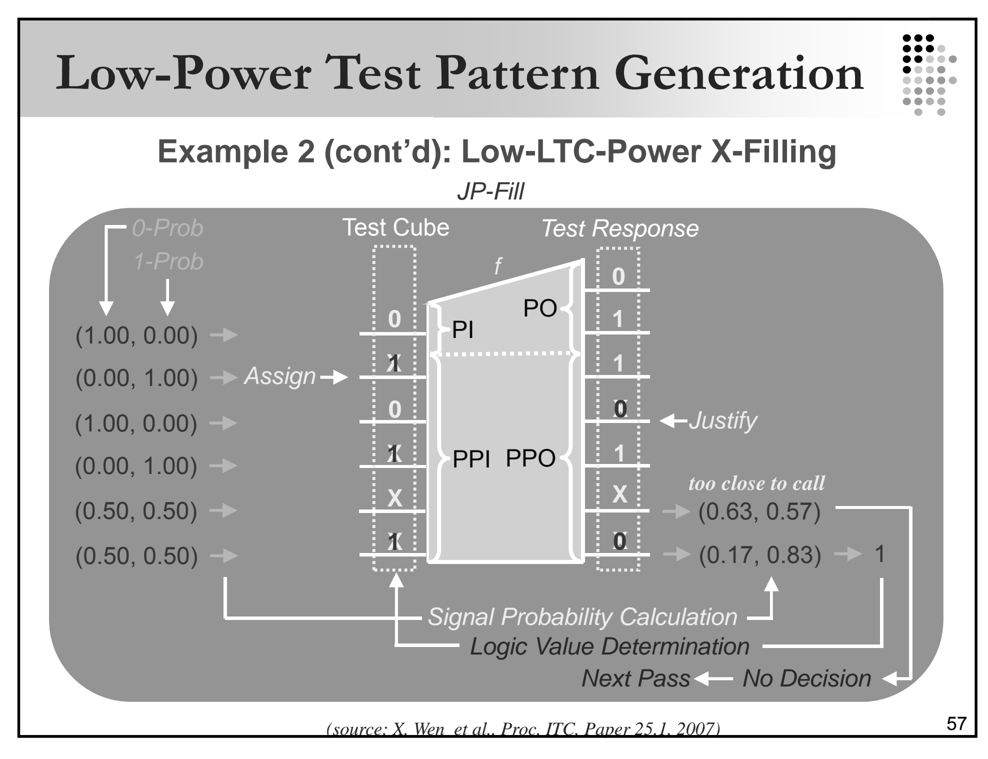
52


Low-Power Test Pattern Generation
Example 1 (cont'd): Low-Shift-Power X-filling
Scan-Out: 1 0 X X 1 X 0 X X 0 :Scan-In
0-Fill
Fill all X-strings with 0.
1-Fill
Fill all X-strings with 1.
MT-Fill
If the specified bits on both sides of an X-string have the same logic value, the X-string is filled with that logic value; otherwise, the X-string is filled with an arbitrary logic value.
Adjacent-Fill
Fill an X-string with the specified-bit on the shift-out side.
0-Fill
1-Fill
MT-Fill
Adjacent-Fill
1 0 0 0 1 0 0 0 0 0
1 0 1 1 1 1 0 1 1 0
1 0 1 1 1 0 0 0 0 0
1 0 0 0 1 1 0 0 0 0
10
25
8
11
• Available from most commercial ATPG tools.
53

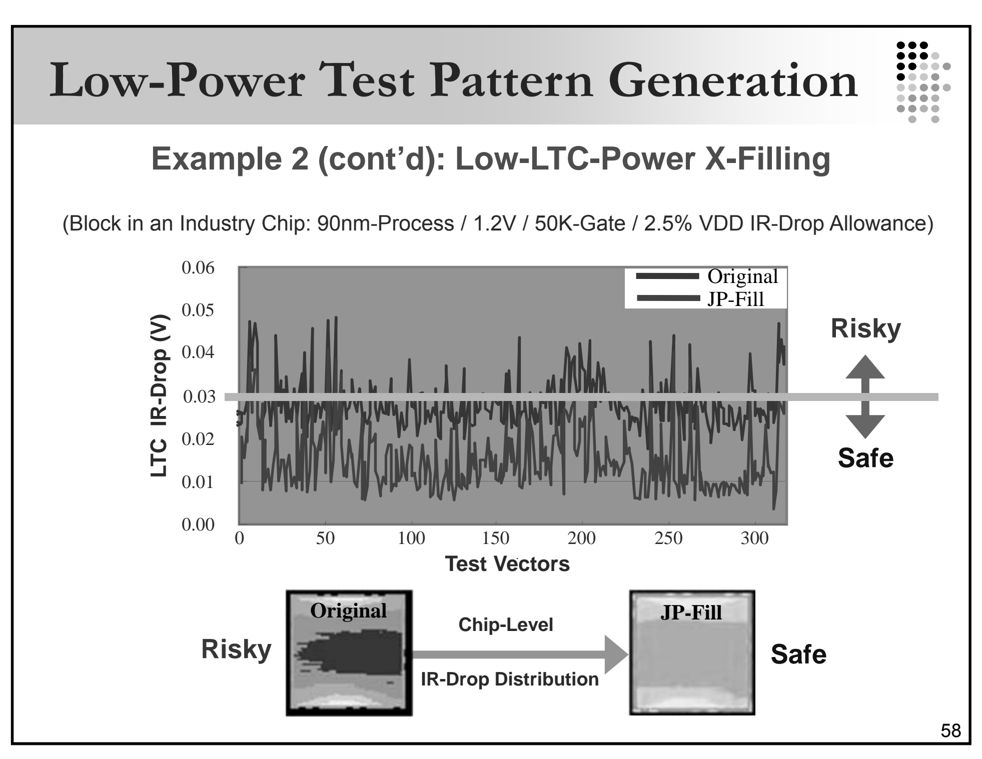

Low-Power Test Pattern Generation
Typical Metric for LTC Power Analysis - (1)
Weighted Switching Activity
WSA
(for a target area of elements (FFs, gates) 1, 2, …, N)
= Σ (ti X wi)
• ti = 1 if the output of element i has a transition; otherwise, ti = 0.
• Wi = (the number of fanout lines from element i) + α (usually 1)
Weight = 2 + 1
(source: S. Wang et al., Proc. ITC, pp. 250-258, 1994)
54


Low-Power Test Pattern Generation
Typical Metric for LTC Power Analysis - (2)
Regional Weighted Switching Activity
Impact Area of Path P
On-Path Gate G
FFs
FFe
Aggressor Region of Gate G
Long Sensitized Path (LSP) P
(> 70% Longest Structural Path)
Target Gate
Power Via
M2
M2
Aggressors
M3
M3
M3
Path P is RISKY if
the WSA in its impact area
>
30% of Maximum WSA in the impact area.
(source: X. Wen et al., Proc. VTS, pp. 166-171, 2011)
55


Low-Power Test Pattern Generation
Example 2: Low-LTC-Power X-Filling
IR-Drop
VDD
Combinational Circuit
Launch-to-Capture (LTC) Power
Delay Increase
Timing
Malfunction
(Test-Induced Yield Loss)
Stimulus
Response
PPI
PPO
FF1
FF2
FF3
To minimize the Hamming distance between PPI and PPO
56



Low-Power Test Pattern Generation
Example 2 (cont'd): Low-LTC-Power X-Filling
JP-Fill
0-Prob
1-Prob
Test Cube
Test Response
f
PI
PO
PPI PPO
(1.00, 0.00)
(0.00, 1.00)
(1.00, 0.00)
(0.00, 1.00)
(0.50, 0.50)
(0.50, 0.50)
Assign
Justify
too close to call
(0.63, 0.57)
(0.17, 0.83)
1
Signal Probability Calculation
Logic Value Determination
Next Pass
No Decision
(source: X. Wen et al., Proc. ITC, Paper 25.1, 2007)
57



Low-Power Test Pattern Generation
Example 2 (cont'd): Low-LTC-Power X-Filling
(Block in an Industry Chip: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)
LTC IR-Drop (V)
Test Vectors
Original
JP-Fill
Risky
Safe
Chip-Level
IR-Drop Distribution
58

Low-Power Test Pattern Generation

Example 3: Low-Shift-&-LTC-Power X-Filling

0-Fill 0**0000**01**00000**10**00000**1

Adjacent Fill 0**0000**01**11111**10**00000**1

Test Cube: 0X**X**XX01XX**X**XX10XX**X**XX1 ← Shift Direction

Bounded Adjacent Fill

0X**0**XX01XX**0**XX10XX**0**XX1

1st 0-Constraint Bit → Bounding Interval = 6

00**0**00011**10**0010000**0**001

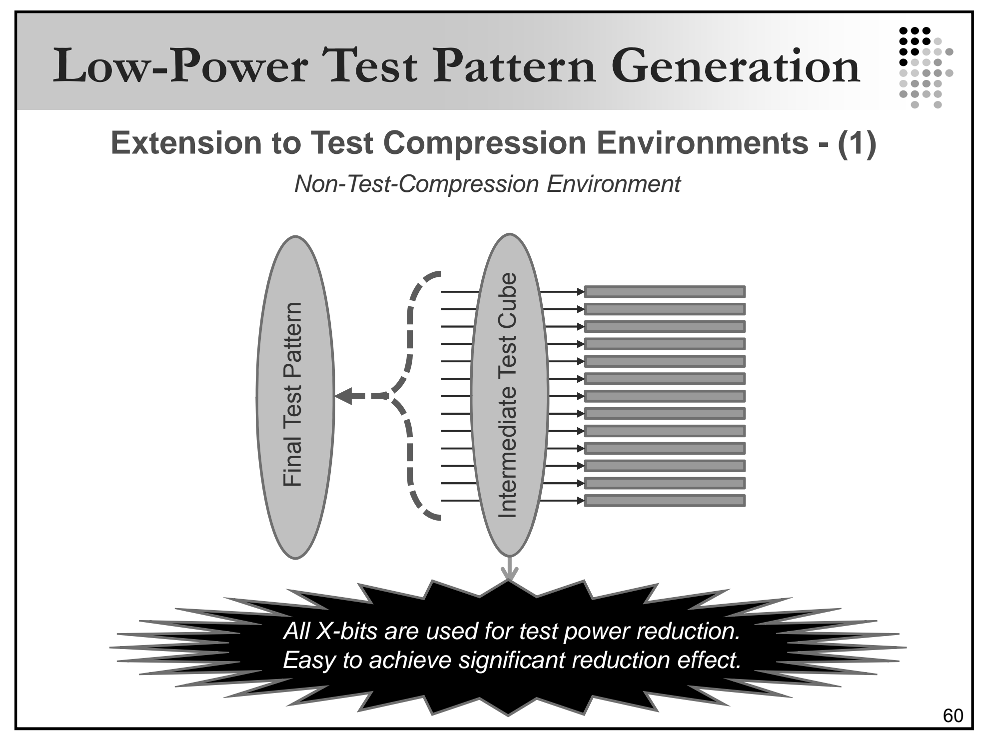
- The basic idea is to first set several *X*-bits in a test cube to 0 and then conduct *adjacent fill*.

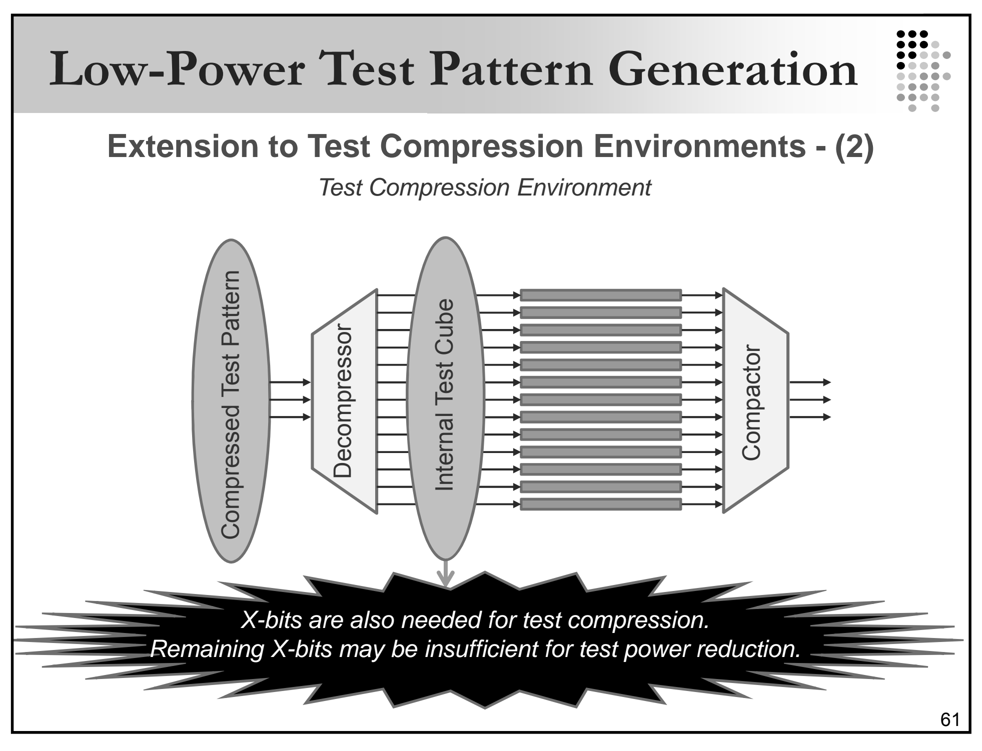
➔ *The occurrence of 0 in the resulting fully-specified test vector is increased, which helps reduce shift-out and LTC power. → making use of the benefit of 0-fill*

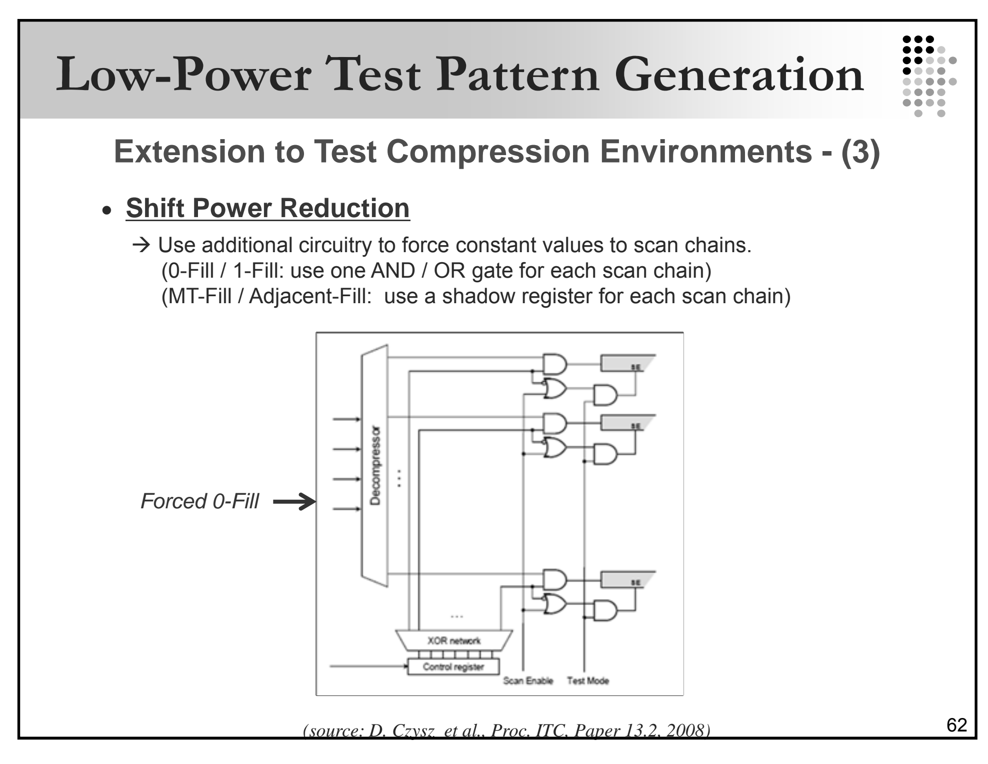
➔ *At the same time, applying adjacent fill helps reduce shift-in power.*

(source: A. Chandra et al., Proc. VTS, pp. 131-138, 2008)

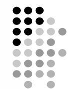
59




Low-Power Test Pattern Generation
Extension to Test Compression Environments - (2)
Test Compression Environment
Compressed Test Pattern
Decompressor
Internal Test Cube
Compactor
X-bits are also needed for test compression.
Remaining X-bits may be insufficient for test power reduction.
61


Low-Power Test Pattern Generation
Extension to Test Compression Environments - (3)
• Shift Power Reduction
→ Use additional circuitry to force constant values to scan chains.
(0-Fill / 1-Fill: use one AND / OR gate for each scan chain)
(MT-Fill / Adjacent-Fill: use a shadow register for each scan chain)
Forced 0-Fill
Decompressor
XOR network
Control register
Scan Enable
Test Mode
(source: D. Czysz et al., Proc. ITC, Paper 13.2, 2008)
62

Low-Power Test Pattern Generation



Extension to Test Compression Environments - (4)

- **LTC Power Reduction**
  - ***Combinational-Decompressor-Based Test Compression***
    - → Disable clock gators in test generation.
    - → Expand the combinational decompressor and apply low-LTC-power X-filling.
    - → Conduct pinpoint LTC power reduction.
  - ***Sequential-Decompressor-Based Test Compression***
    - → Disable clock gators in test generation.
    - → Apply low-LTC-power X-filling to independent or free X-bits.
    - → Conduct pinpoint LTC power reduction.

63

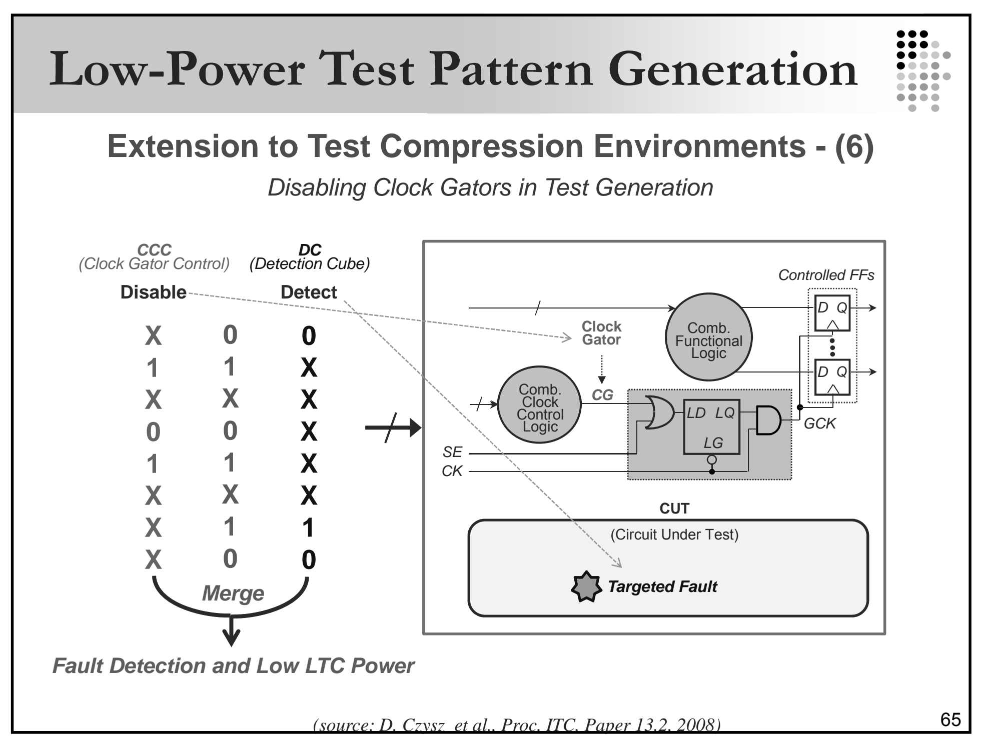
Low-Power Test Pattern Generation

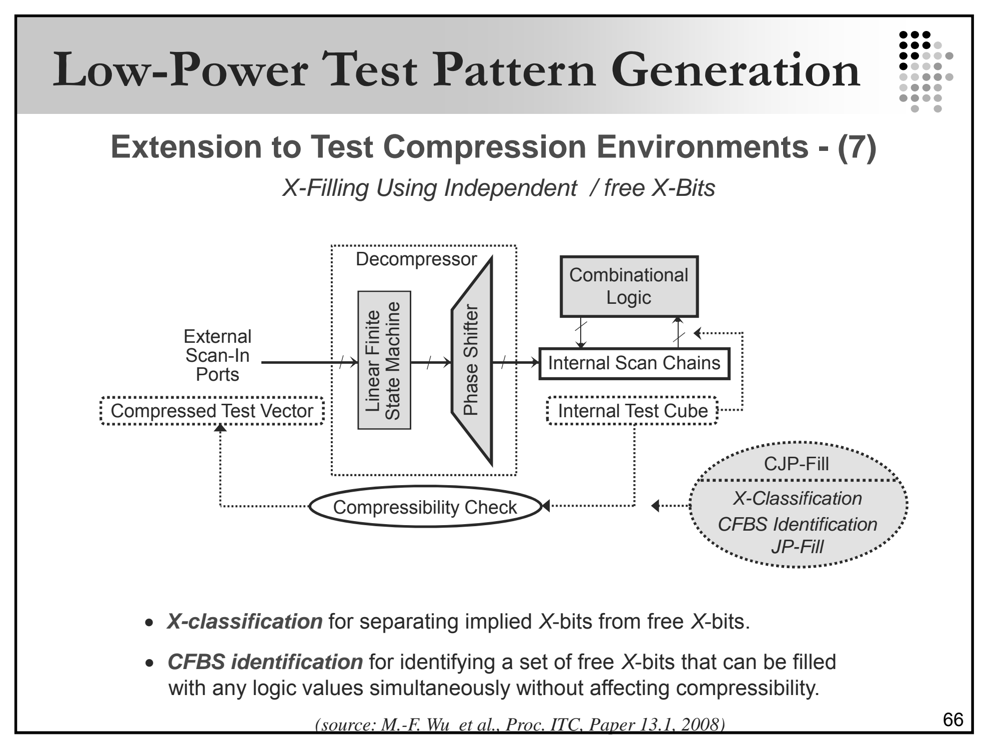
Extension to Test Compression Environments - (5)

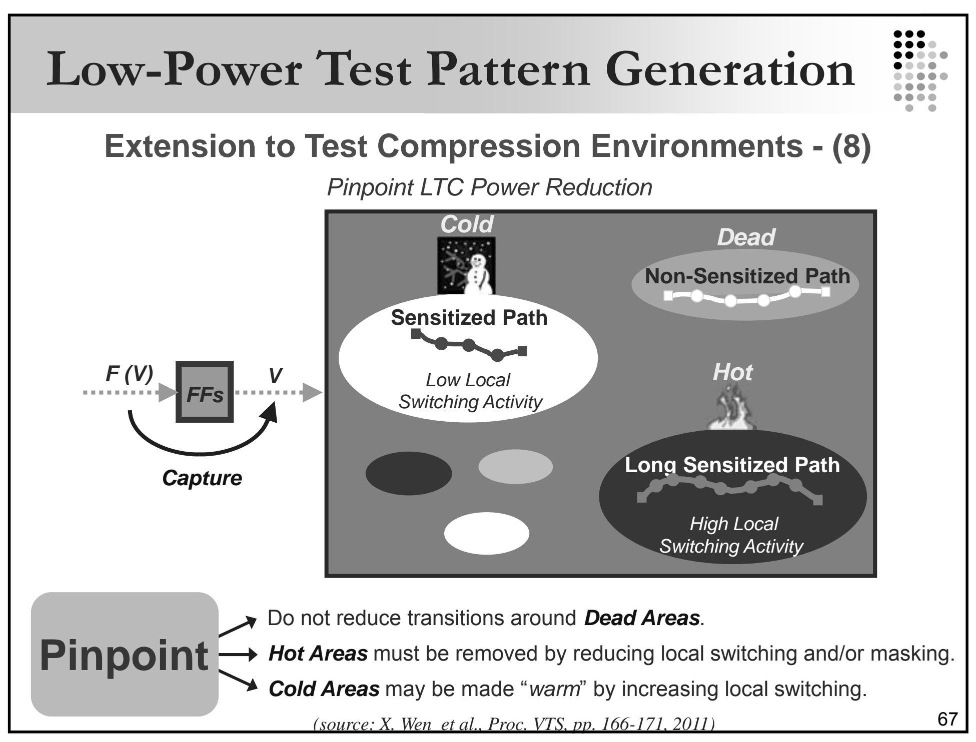
Low-LTC-Power X-Filling based on Combinational Decompressor Expansion

(source: K. Miyase et al., Proc. ICCAD, pp. 97-104, 2009)

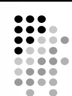
64


Low-Power Test Pattern Generation
Extension to Test Compression Environments - (6)
Disabling Clock Gators in Test Generation
CCC
(Clock Gator Control)
DC
(Detection Cube)
Disable
Detect
Merge
Fault Detection and Low LTC Power
Controlled FFs
Clock Gator
Comb. Functional Logic
Comb. Clock Control Logic
CG
LD LQ
LG
GCK
SE
CK
CUT
(Circuit Under Test)
Targeted Fault
(source: D. Czysz, et al., Proc. ITC, Paper 13.2, 2008)
65


Low-Power Test Pattern Generation
Extension to Test Compression Environments - (7)
X-Filling Using Independent / free X-Bits
Decompressor
Linear Finite State Machine
Phase Shifter
Combinational Logic
External Scan-In Ports
Internal Scan Chains
Compressed Test Vector
Internal Test Cube
CJP-Fill
X-Classification
CFBS Identification
JP-Fill
Compressibility Check
• X-classification for separating implied X-bits from free X-bits.
• CFBS identification for identifying a set of free X-bits that can be filled with any logic values simultaneously without affecting compressibility.
(source: M.-F. Wu, et al., Proc. ITC, Paper 13.1, 2008)
66



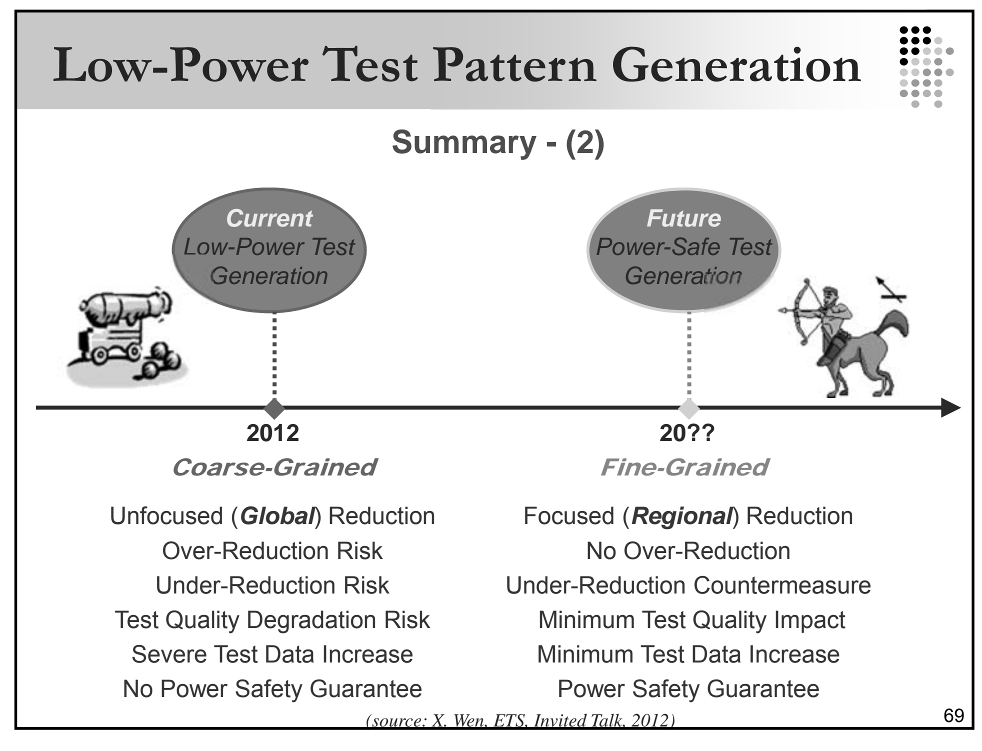
Low-Power Test Pattern Generation



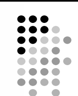
Summary - (1)

- A large portion of input bits in test cubes are don't care bits (X-bits) even after aggressive test compaction in ATPG.
- X-bits can be used for reducing various shift and/or LTC power. Especially, 0-fill can reduce shift-in, shift-out, and LTC power to some extent.
- X-filling-based low-power test generation causes neither area overhead nor performance degradation.
- Most commercial ATPG tools now support low-power X-filling.
- Test pattern count may increase due to low-power X-filling. This problem can be solved by
  (1: *Vector-Pinpoint*) identifying high-test-power test patterns and conducting X-filling only for those patterns, or
  (2: *Area-Pinpoint*) identifying high-test-power areas and conducting X-filing only to reduce test power in those areas.

68



Reducing Test Power



Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

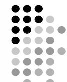
Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, …

70

Design for Test Power Reduction



During scan testing (standard or at-speed):

Shift Power Reduction	LTC Power Reduction
• **Shift Impact Blocking** - *blocking gate, special scan cell* - *first-level power supply gating* • **Scan Chain Modification** - *scan cell reordering* - *scan chain segmentation* - *scan chain disable* • **Scan Clock Manipulation** - *splitting, staggering* - *multi-duty clocking*	• **Partial Capture** - *circuit modification* - *scan chain disable* - *one-hot clocking* - *capture-clock staggering*

71

Design for Test Power Reduction

Example 1: Low power scan cell

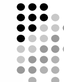
Scan Enable
D
Q
Scan In
Scan Enable
CLK
0
1
Data Out
Scan Out

An implementation of toggle suppression during shift using a latch at the output of the mux-D flip-flop with scan

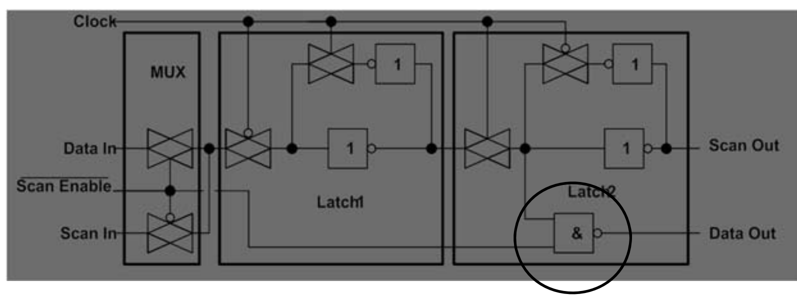
(source: X. Zhang and K. Roy, Proc. IOLTW, pp. 133-138, 2000)

72

Design for Test Power Reduction



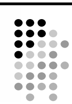
Example 1 (cont'd): Low power scan cell



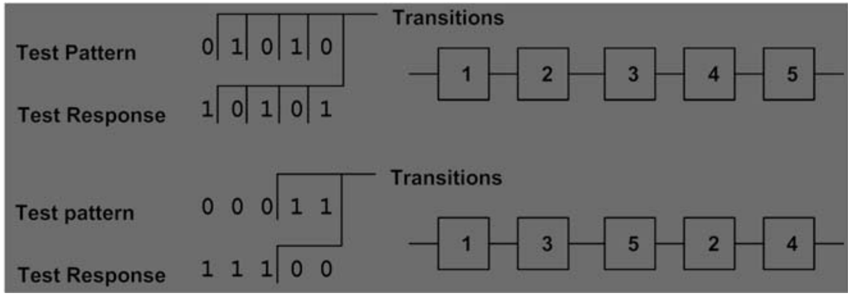
- Master-slave structure of a mux-D flip-flop is modified
- Gate the data output during shift
- Toggle suppression during shift
- But modification of all flip-flops → impact on area and performance

(source: A. Hertwig and H.-J. Wunderlich, Proc. ETW, pp. 49-53, 1998)

Design for Test Power Reduction

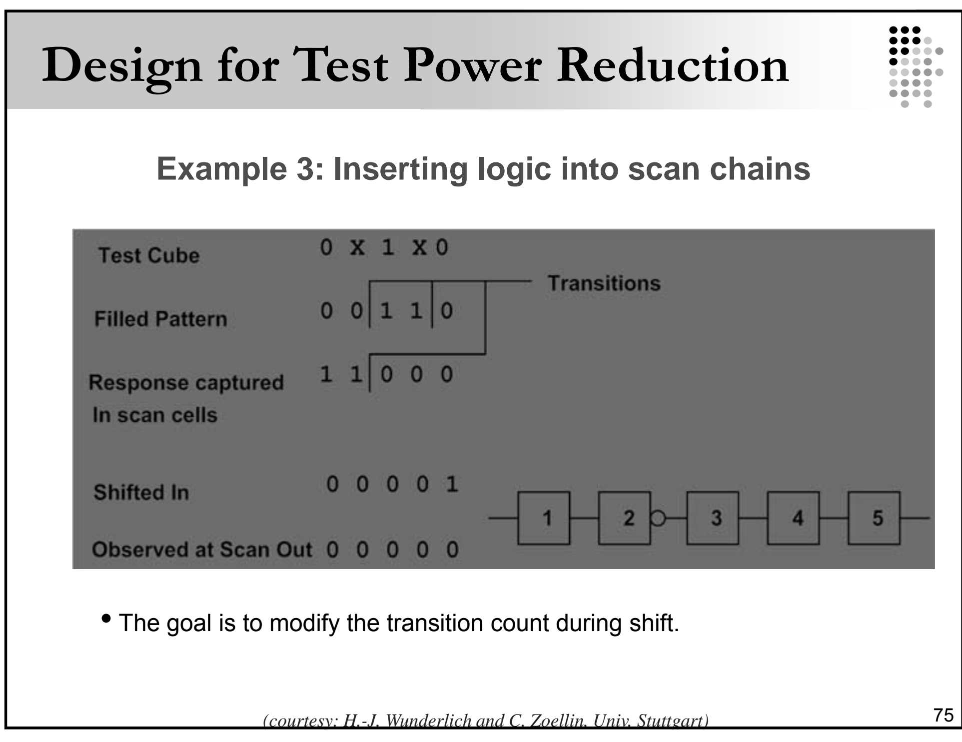


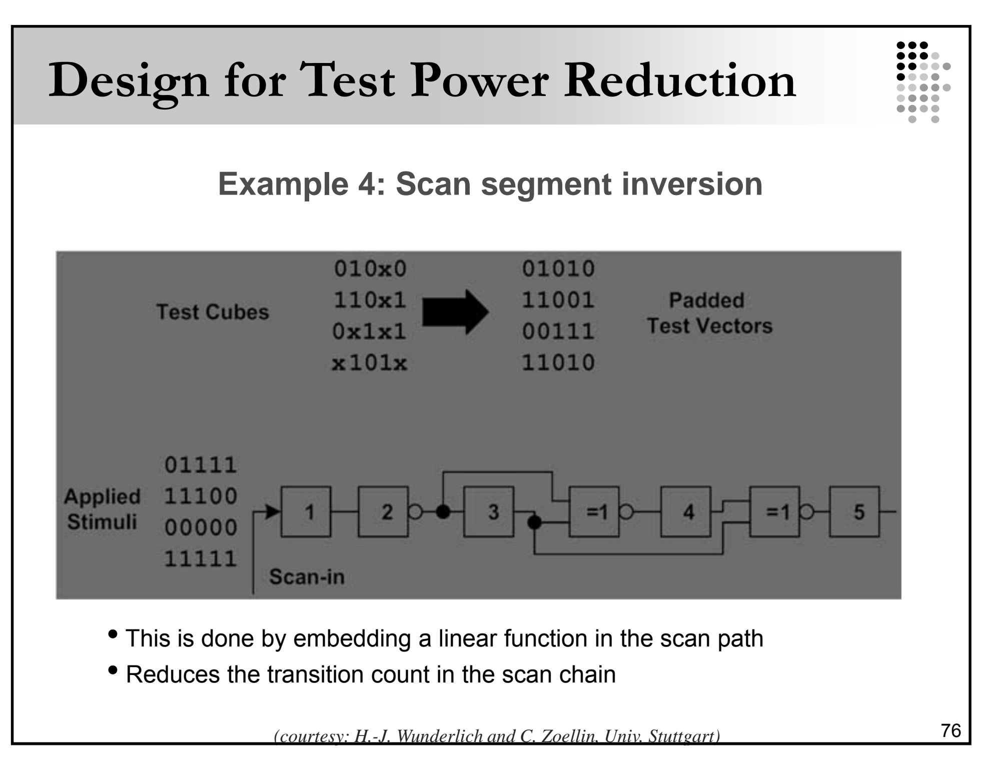
Example 2 : Scan cell reordering



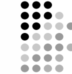
- Scan cell order influences the number of transitions
- Need to change the order of bits in each vector during test application
- No overhead, FC and test time unchanged, low impact on design flow
- May lead to routing congestion problems …

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

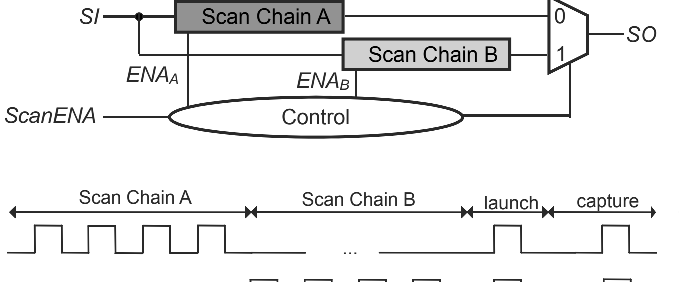

Design for Test Power Reduction
Example 3: Inserting logic into scan chains
Test Cube
0 X 1 X 0
Transitions
Filled Pattern
0 0 1 1 0
Response captured
In scan cells
1 1 0 0 0
Shifted In
0 0 0 0 1
Observed at Scan Out
0 0 0 0 0
1
2
3
4
5
The goal is to modify the transition count during shift.
(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)
75


Design for Test Power Reduction
Example 4: Scan segment inversion
Test Cubes
010x0
110x1
0x1x1
x101x
01010
11001
00111
11010
Padded
Test Vectors
Applied
Stimuli
01111
11100
00000
11111
Scan-in
1
2
3
=1
4
=1
5
This is done by embedding a linear function in the scan path
Reduces the transition count in the scan chain
(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)
76

Design for Test Power Reduction



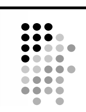
Example 5: Scan chain segmentation



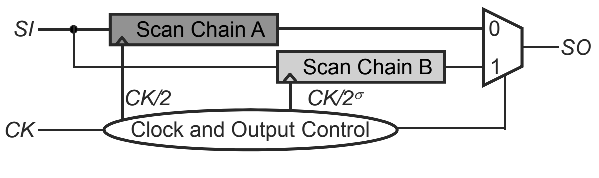
- Controllable and data-independent effect of shift power reduction
- No change to ATPG and no increase in test application time
- Presented (and used) by TI @ ITC 2000

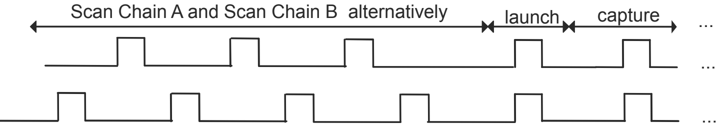
77

Design for Test Power Reduction



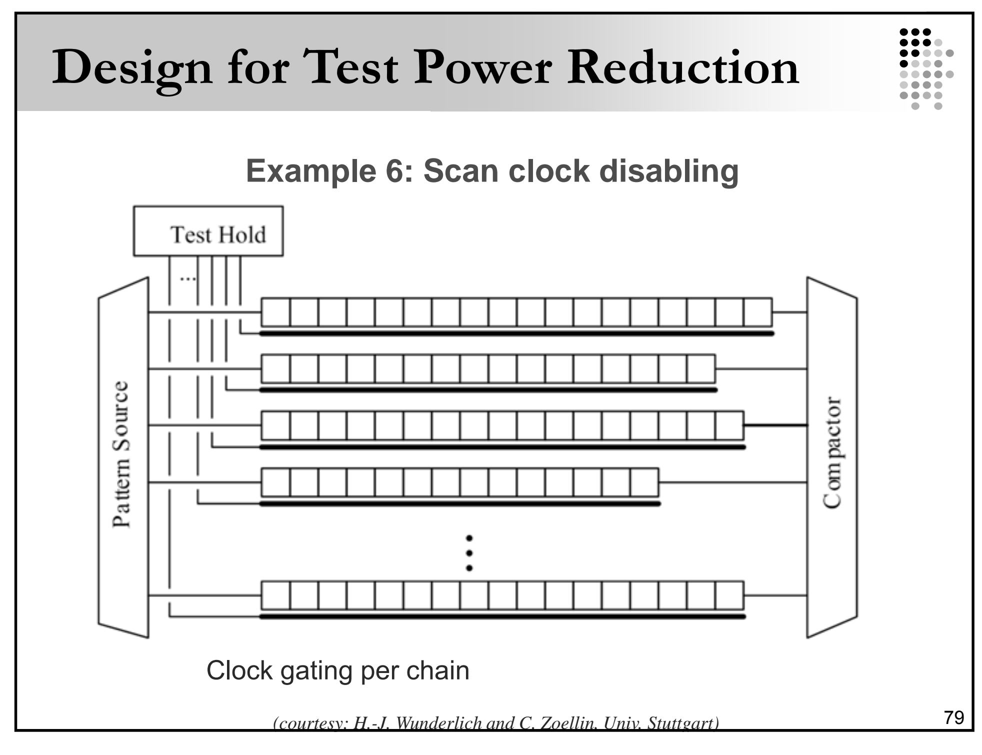
Example 5 (cont'd): Scan chain segmentation

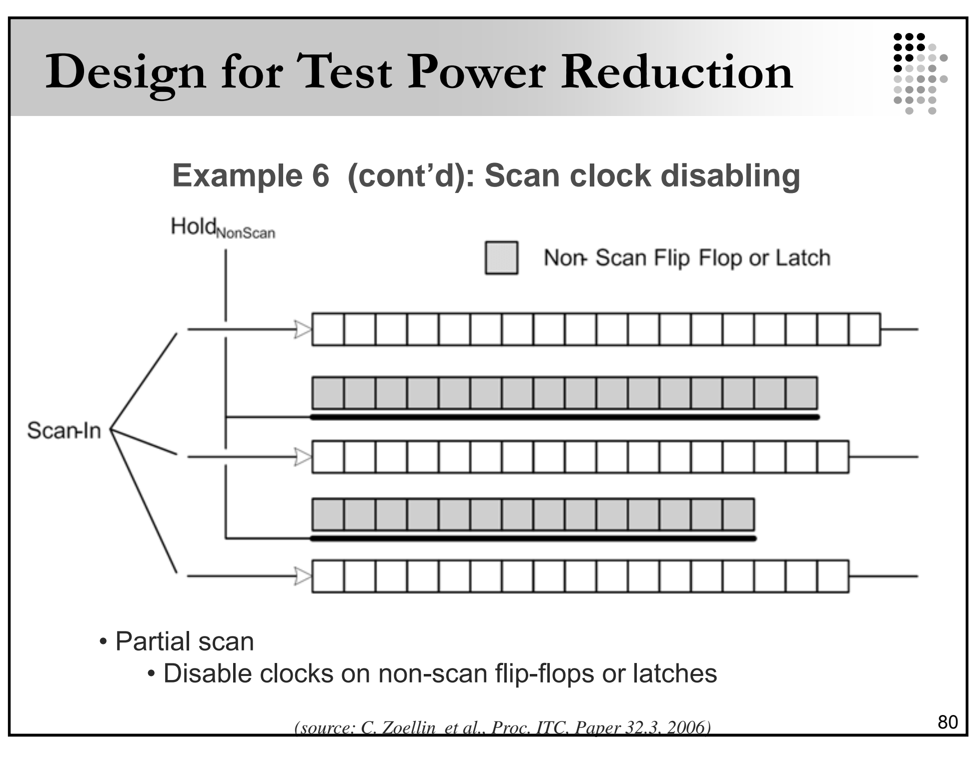


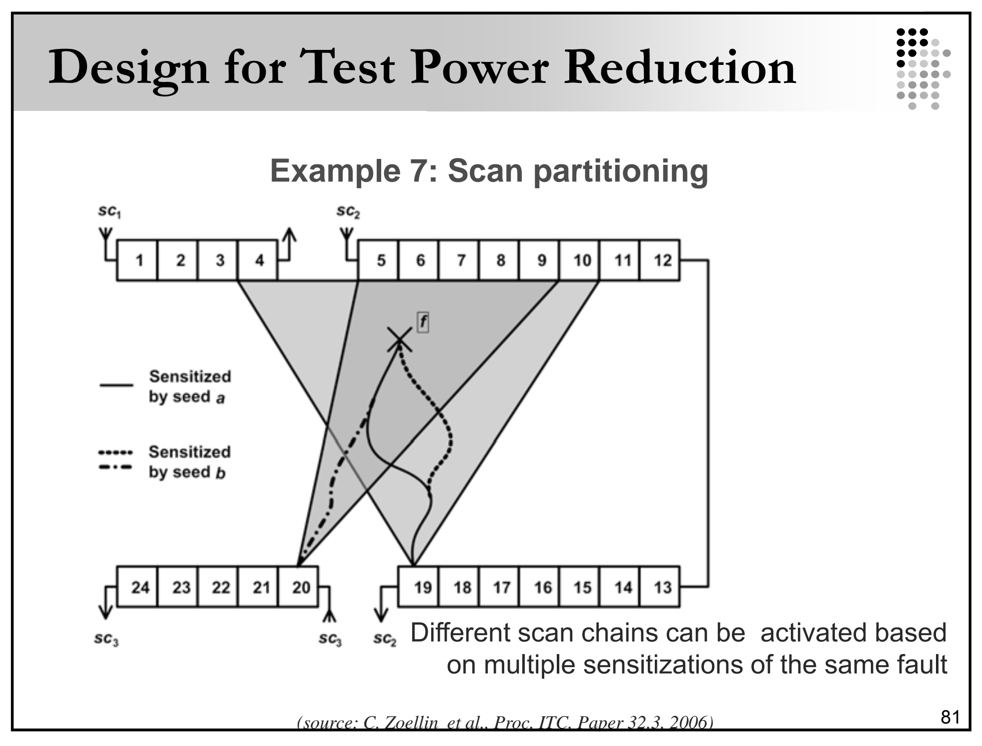


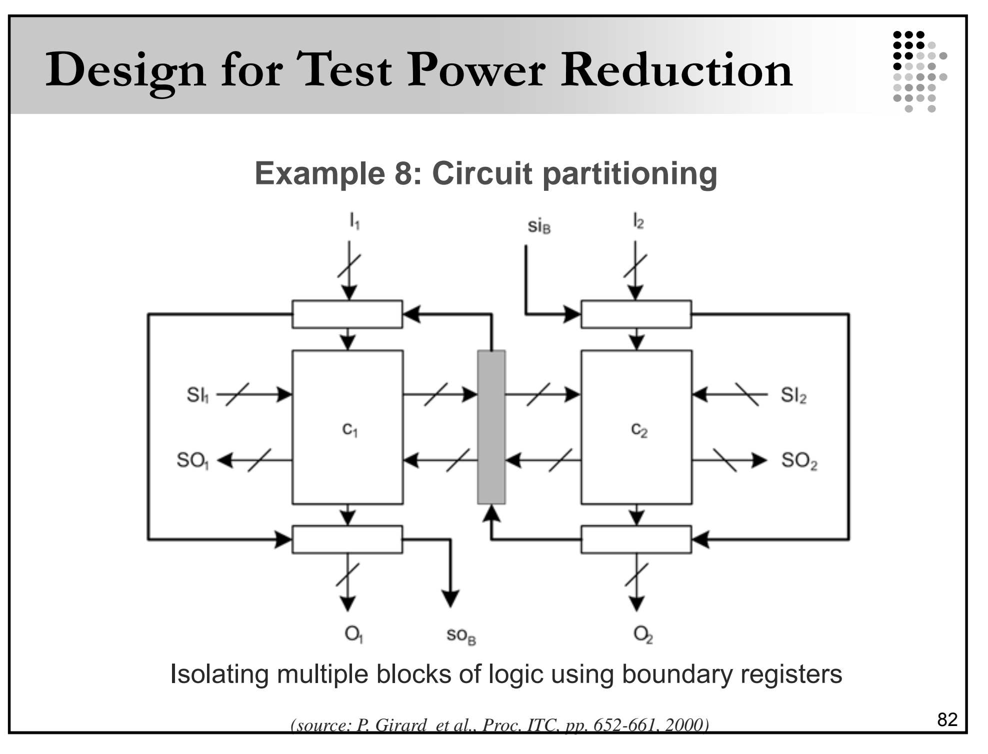
- The original scan chain is segmented into two scan chains
- Each scan chain is driven by a clock whose speed is half of the normal speed
- At each clock cycle, only half of the circuit inputs can switch

78

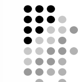

Design for Test Power Reduction
Example 6: Scan clock disabling
Test Hold
Pattern Source
Compactor
Clock gating per chain
(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)
79


Design for Test Power Reduction
Example 6 (cont'd): Scan clock disabling
Hold NonScan
Non-Scan Flip Flop or Latch
Scan-In
• Partial scan
• Disable clocks on non-scan flip-flops or latches
(source: C. Zoellin et al., Proc. ITC, Paper 32.3, 2006)
80


Design for Test Power Reduction
Example 7: Scan partitioning
sc1
sc2
1
2
3
4
5
6
7
8
9
10
11
12
f
Sensitized by seed a
Sensitized by seed b
24
23
22
21
20
19
18
17
16
15
14
13
sc3
sc3
sc2
Different scan chains can be activated based on multiple sensitizations of the same fault
(source: C. Zoellin et al., Proc. ITC, Paper 32.3, 2006)
81


Design for Test Power Reduction
Example 8: Circuit partitioning
I1
siB
I2
SI1
SO1
c1
c2
SI2
SO2
O1
soB
O2
Isolating multiple blocks of logic using boundary registers
(source: P. Girard et al., Proc. ITC, pp. 652-661, 2000)
82

Reducing Test Power



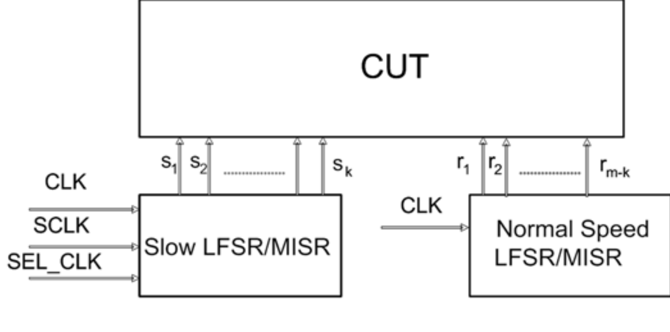
Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

83

Power-Aware BIST and Compression

Example 1: Dual-speed LFSR for BIST



Dual-speed LFSR - concept

(source: S. Wang and S. Gupta, Proc. ITC, pp. 848-857, 1997)

84

Power-Aware BIST and Compression

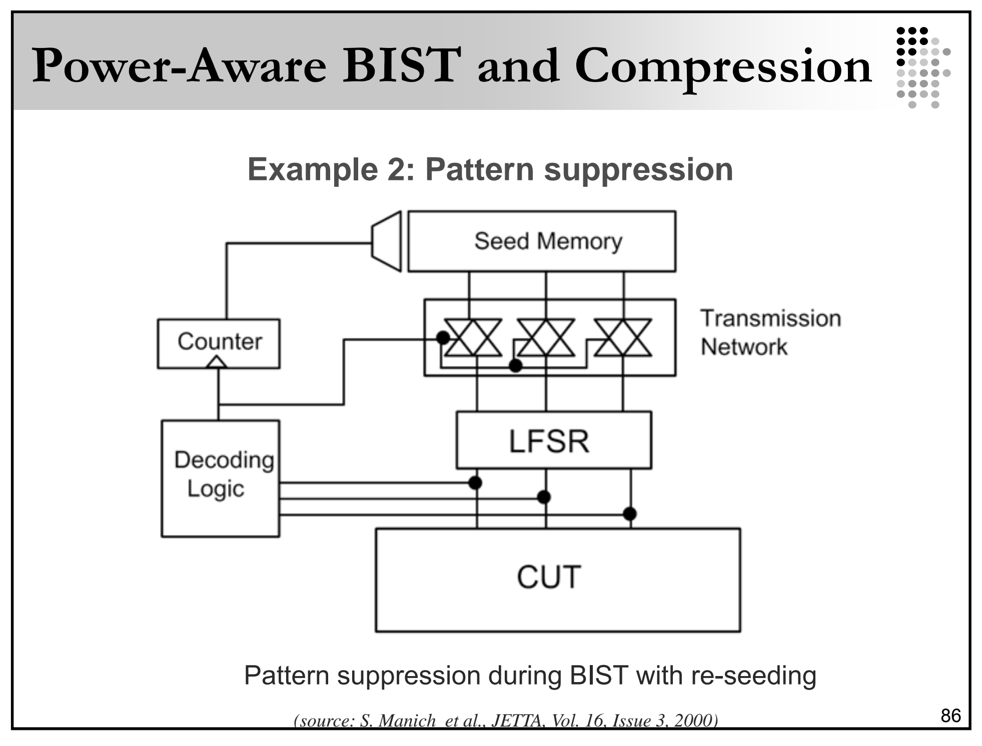
Example 1 (cont'd): Dual-speed LFSR for BIST

		Partitioned S	Partitioned N		Reordered S	Reordered N
0001		00	01		01	01
1000		10	00		01	10
0100		01	00		01	11
0010		00	10		01	00
1001	Partitioned →	10	01	Reordered →	10	01
1100		11	00		10	10
0110		01	10		10	11
1011		10	11		10	00
0101		01	01		11	01
1010		10	10		11	10
1101		11	01		11	11
1110		11	10		11	00
1111		11	11		00	01
0111		01	11		00	10
0011		00	11		00	11
0000		00	00		00	00

(source: S. Wang and S. Gupta, Proc. ITC, pp. 848-857, 1997)

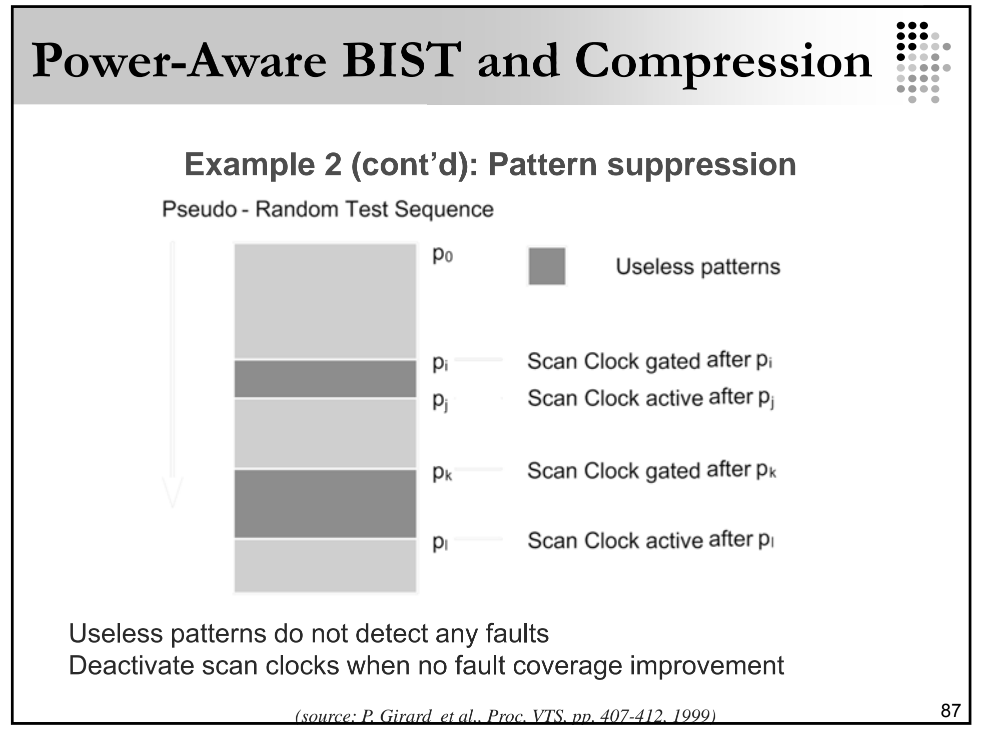
Power-Aware BIST and Compression

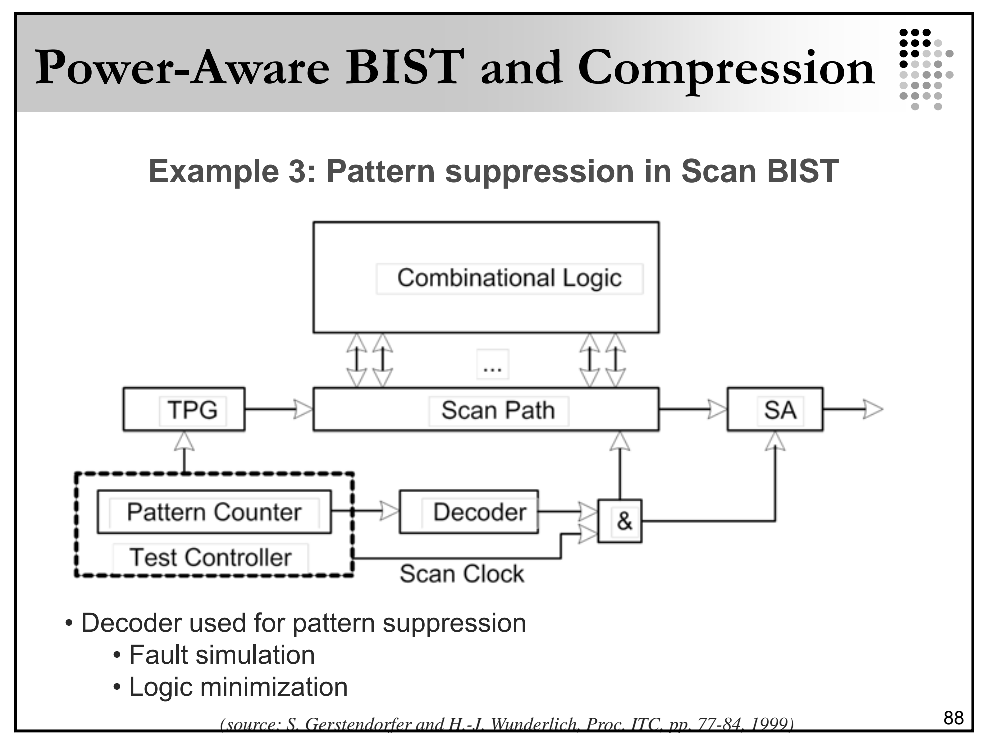
Example 2: Pattern suppression



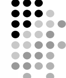
Pattern suppression during BIST with re-seeding

(source: S. Manich et al., JETTA, Vol. 16, Issue 3, 2000)


Power-Aware BIST and Compression
Example 2 (cont'd): Pattern suppression
Pseudo - Random Test Sequence
p0
Useless patterns
pi
Scan Clock gated after pi
pj
Scan Clock active after pj
pk
Scan Clock gated after pk
pl
Scan Clock active after pl
Useless patterns do not detect any faults
Deactivate scan clocks when no fault coverage improvement
(source: P. Girard et al., Proc. VTS, pp. 407-412, 1999)
87


Power-Aware BIST and Compression
Example 3: Pattern suppression in Scan BIST
Combinational Logic
...
TPG
Scan Path
SA
Pattern Counter
Test Controller
Decoder
&
Scan Clock
• Decoder used for pattern suppression
• Fault simulation
• Logic minimization
(source: S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999)
88

Power-Aware BIST and Compression



Example 3 (cont'd): Pattern suppression in Scan BIST

index	binary	# faults	index	binary	#faults
0	0000	17	8	1000	2
1	0001	9	9	1001	0
2	0010	4	10	1010	0
3	0011	0	11	1011	1
4	0100	5	12	1100	0
5	0101	2	13	1101	0
6	0110	3	14	1110	0
7	0111	0	15	1111	0

{0000 , 0001 , 0010 , 0100 , 0101, 0110 , 1000 , 1011 , 1100} **on-set**

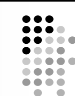
{0011 , 0111 , 1001 , 1010} **off-set**

{1101 , 1110 , 1111} **dc-set**

Implementing the pattern decoder

(source: S. Gerstendorfer and H.-J. Wunderlich, Proc. ITC, pp. 77-84, 1999)

Power-Aware BIST and Compression

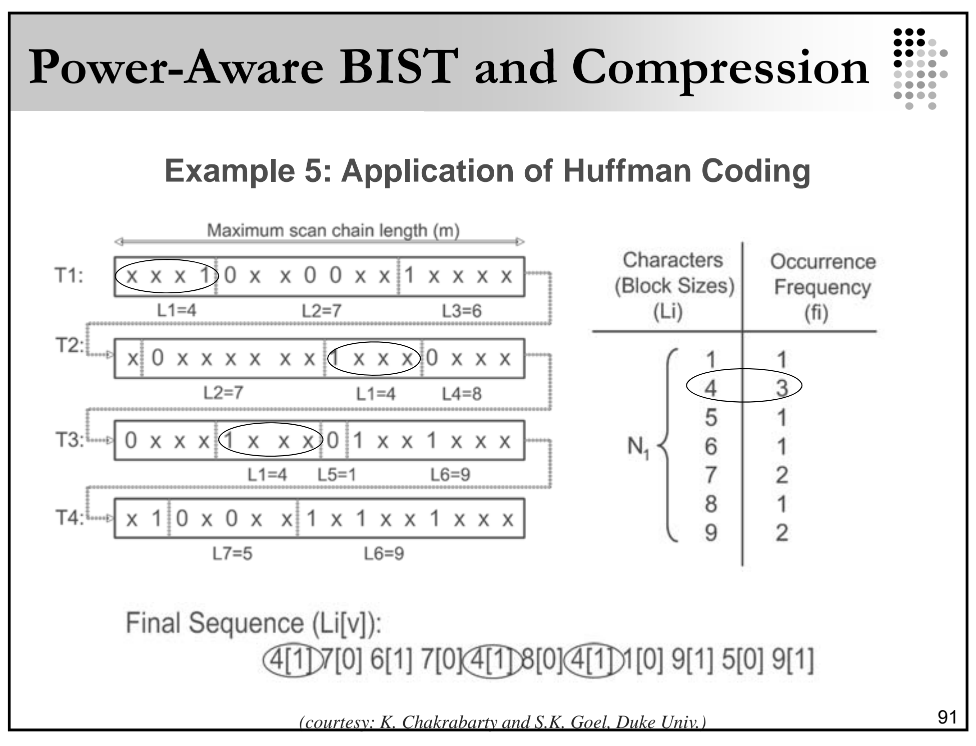


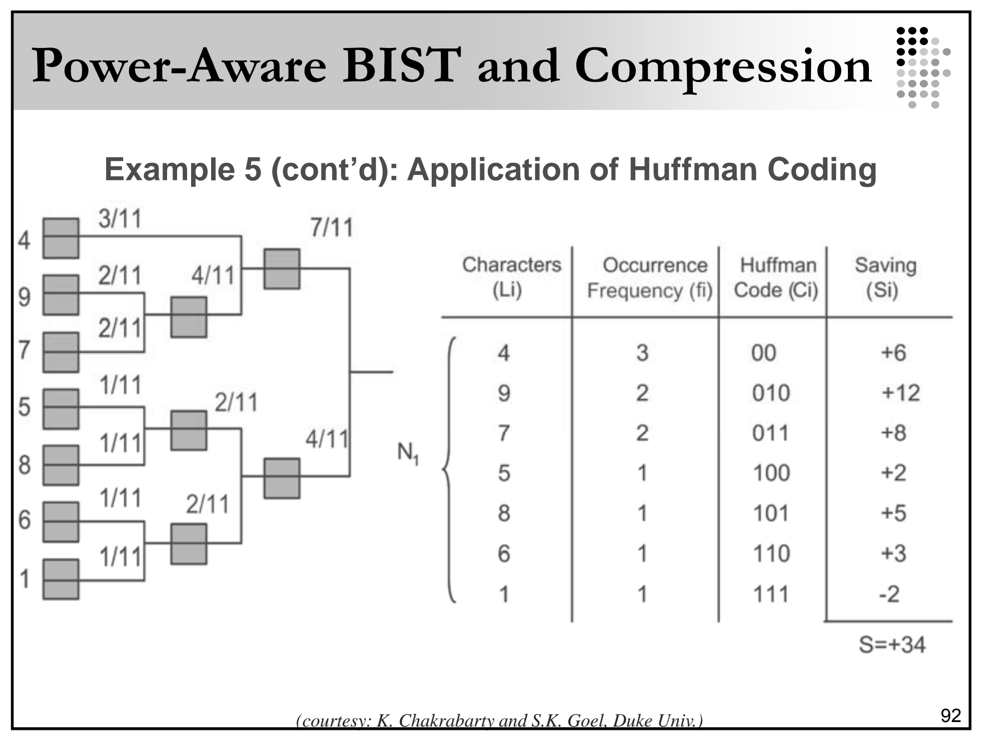
Example 4: Application of Run-Length Coding

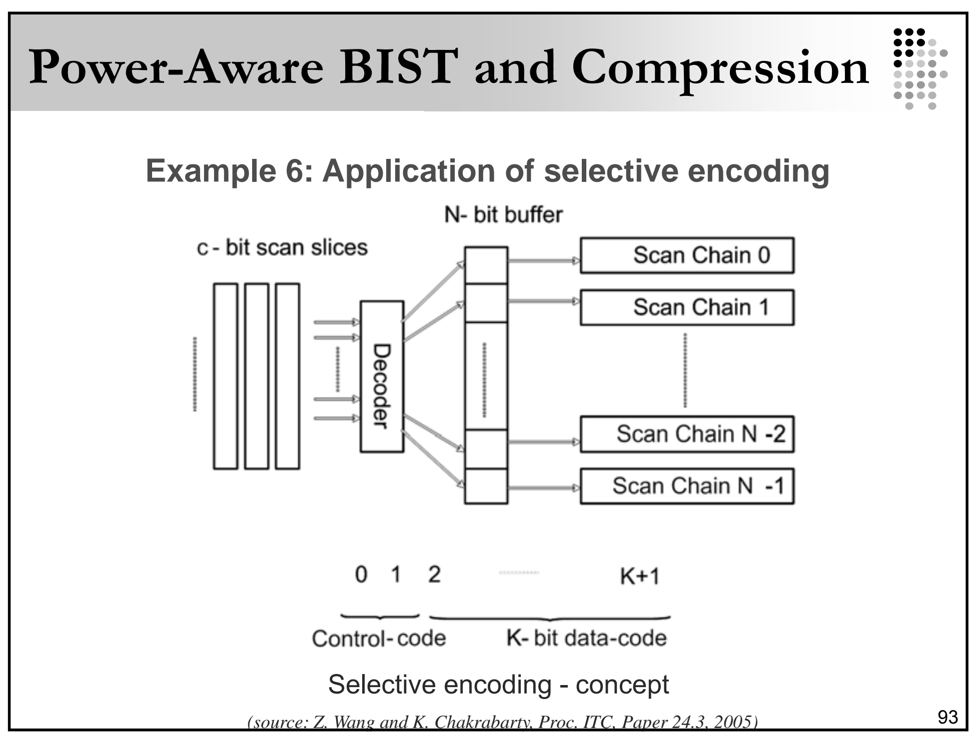
Group	Run-Length	Group Prefix	Tail	Codeword
A_1	0	0	00	000
	1		01	001
	2		10	010
	3		11	011
A_2	4	10	00	1000
	5		01	1001
	6		10	1010
	7		11	1011
A_3	8	110	00	11000
	9		01	11001
	10		10	11010
	11		11	11011

Golomb code

(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)


Power-Aware BIST and Compression
Example 5: Application of Huffman Coding
Maximum scan chain length (m)
T1:
x x x 1 0 x x 0 0 x x 1 x x x x
L1=4
L2=7
L3=6
T2:
x 0 x x x x x x 1 x x x 0 x x x
L2=7
L1=4
L4=8
T3:
0 x x x 1 x x x 0 1 x x 1 x x x
L1=4
L5=1
L6=9
T4:
x 1 0 x 0 x x 1 x 1 x x 1 x x x
L7=5
L6=9
Characters (Block Sizes) (Li)
Occurrence Frequency (fi)
N1
1 1
4 3
5 1
6 1
7 2
8 1
9 2
Final Sequence (Li[v]):
4[1] 7[0] 6[1] 7[0] 4[1] 8[0] 4[1] 1[0] 9[1] 5[0] 9[1]
(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)
91


Power-Aware BIST and Compression
Example 5 (cont'd): Application of Huffman Coding
4
9
7
5
8
6
1
3/11
2/11
2/11
1/11
1/11
1/11
1/11
4/11
2/11
2/11
7/11
4/11
N1
Characters (Li)
Occurrence Frequency (fi)
Huffman Code (Ci)
Saving (Si)
4 3 00 +6
9 2 010 +12
7 2 011 +8
5 1 100 +2
8 1 101 +5
6 1 110 +3
1 1 111 -2
S=+34
(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)
92



Power-Aware BIST and Compression

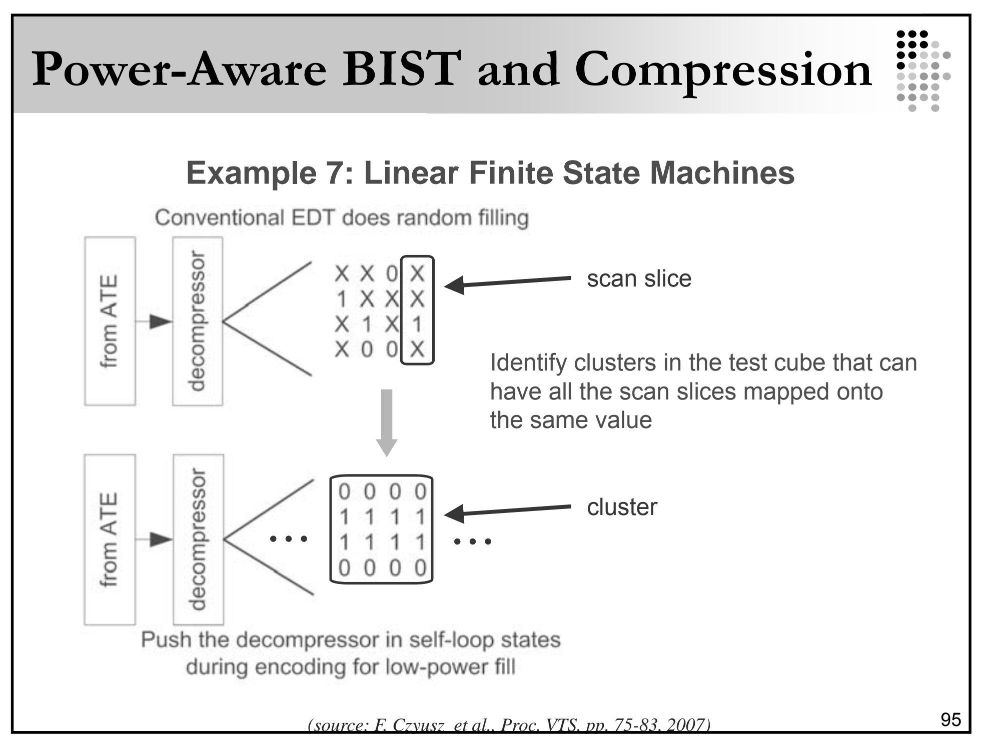
Example 6 (cont'd): Application of selective encoding

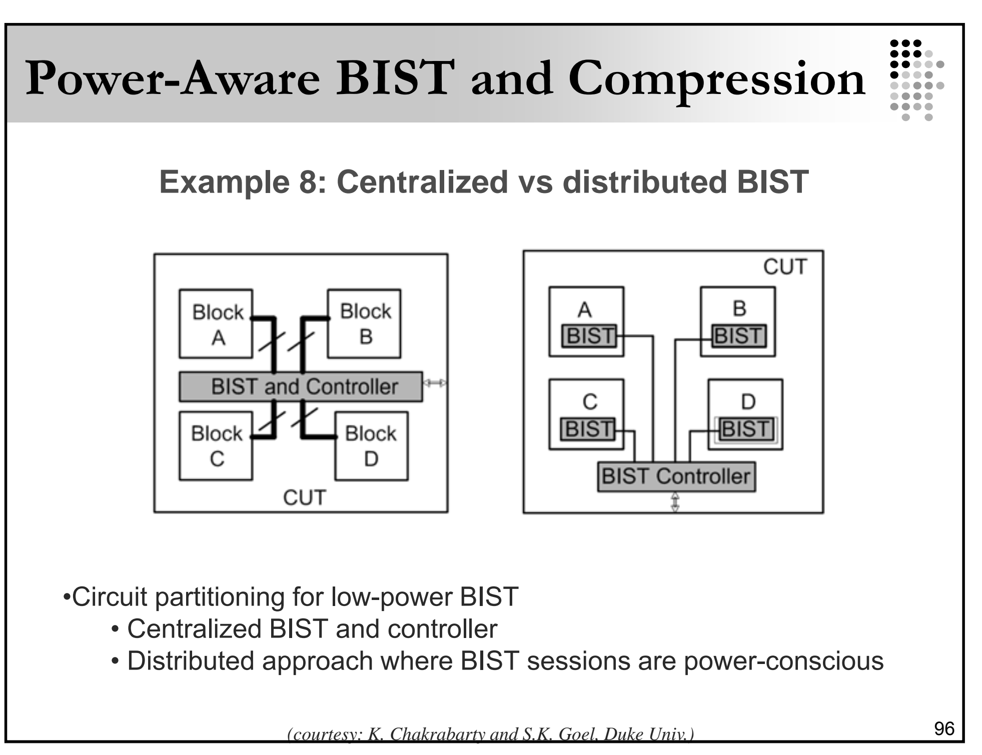
Slice	Slice code		Description
	Control code	Data code	
XX00 010X	00	0101	Start a new slice, map X to 0, set bit 5 to 1
1110 0001	00	0111	Start a new slice, map X to 0, set bit 7 to 1
	11	0000	Enter group-copy-mode, starting from bit 0 (i.e., group 0)
	11	1110	The data is 1110
XXXX XX11	01	1000	Start a new slice, map X to 1, no bits are set to 0

Selective encoding - example

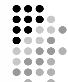
(source: Z. Wang and K. Chakrabarty, Proc. ITC, Paper 24.3, 2005)

94


Power-Aware BIST and Compression
Example 7: Linear Finite State Machines
Conventional EDT does random filling
from ATE
decompressor
X X 0 X
1 X X X
X 1 X 1
X 0 0 X
scan slice
Identify clusters in the test cube that can have all the scan slices mapped onto the same value
0 0 0 0
1 1 1 1
1 1 1 1
0 0 0 0
cluster
Push the decompressor in self-loop states during encoding for low-power fill
(source: F. Czyusz et al., Proc. VTS, pp. 75-83, 2007)
95


Power-Aware BIST and Compression
Example 8: Centralized vs distributed BIST
Block A
Block B
BIST and Controller
Block C
Block D
CUT
CUT
A
BIST
B
BIST
C
BIST
D
BIST
BIST Controller
•Circuit partitioning for low-power BIST
• Centralized BIST and controller
• Distributed approach where BIST sessions are power-conscious
(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)
96

Reducing Test Power



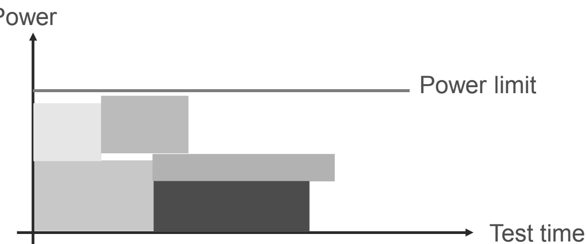
Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

97

System-Level Power-Aware Scheduling

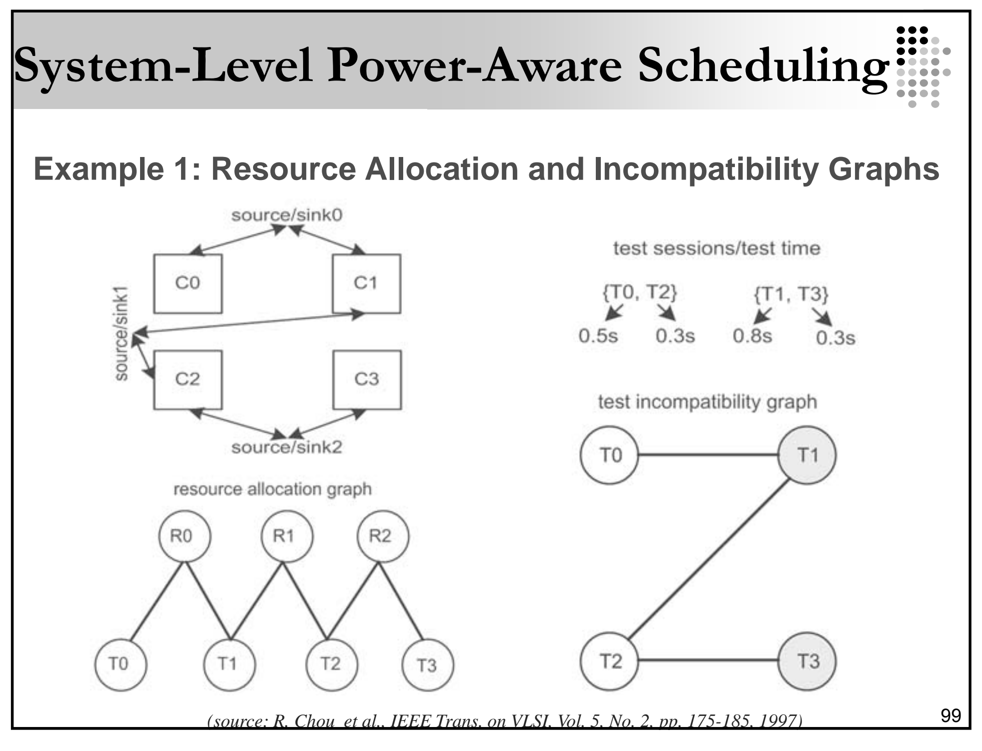
Improve Test Throughput by Exploiting Design Modularity

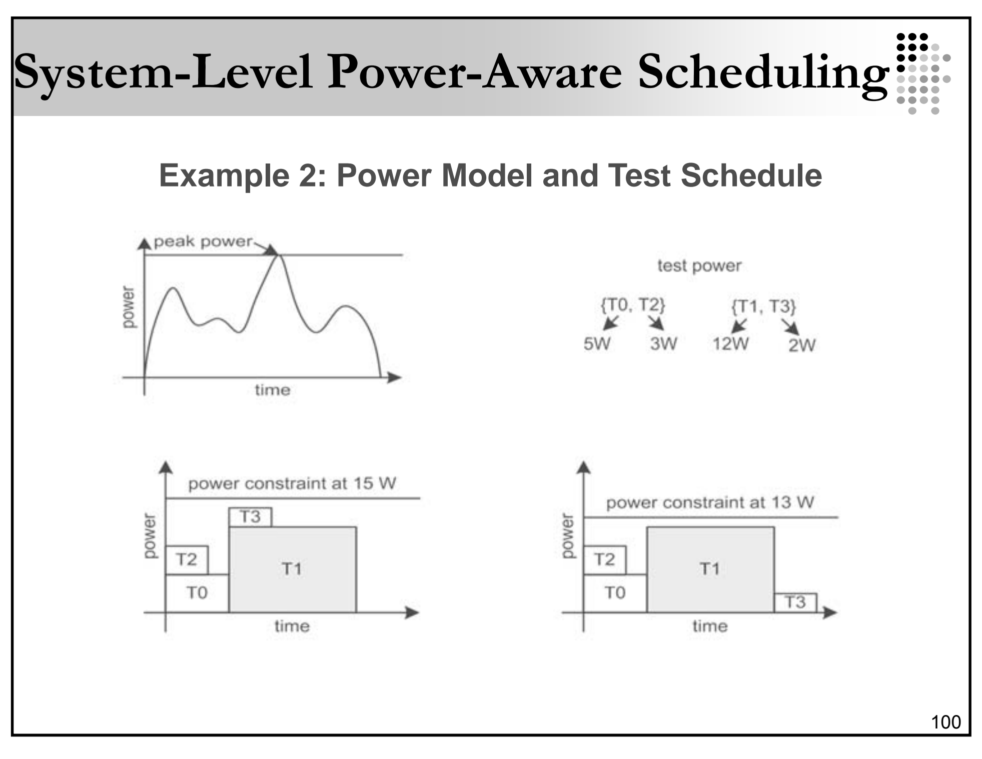


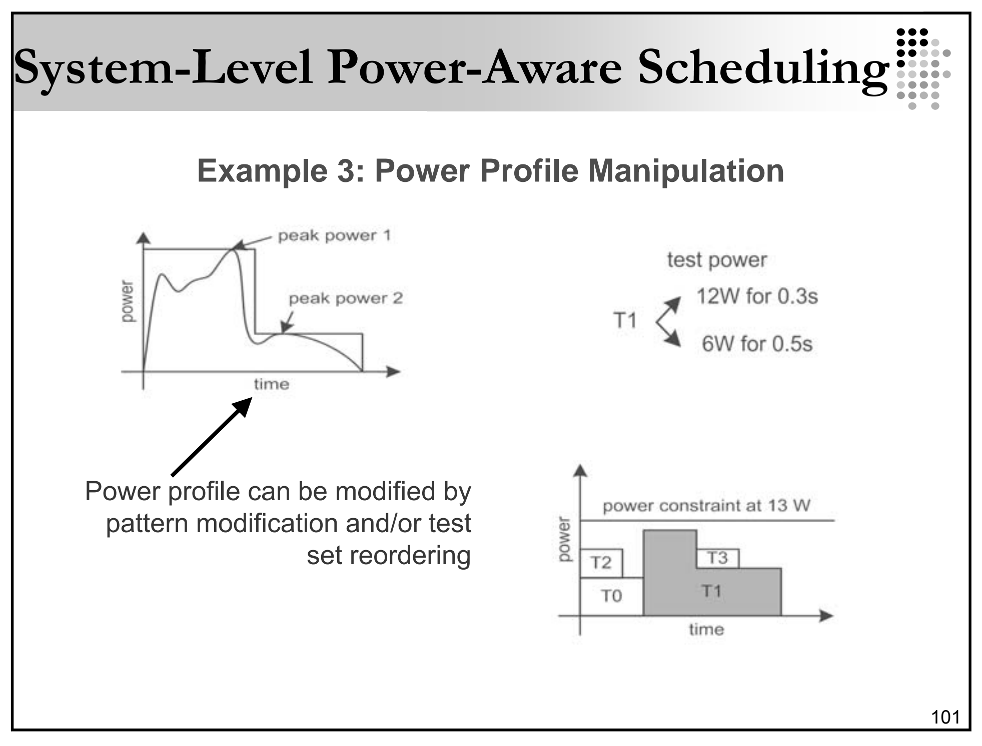
- The goal is to determine the blocks (memory, logic, analog, etc.) of an SOC to be tested in parallel at each stage of a test session in order to keep power dissipation under a specified limit while optimizing test time
- Some of the test resources (pattern generators and response analyzers) must be shared among the various blocks

(source: Y. Zorian, Proc. VTS, pp. 4-9, 1993)

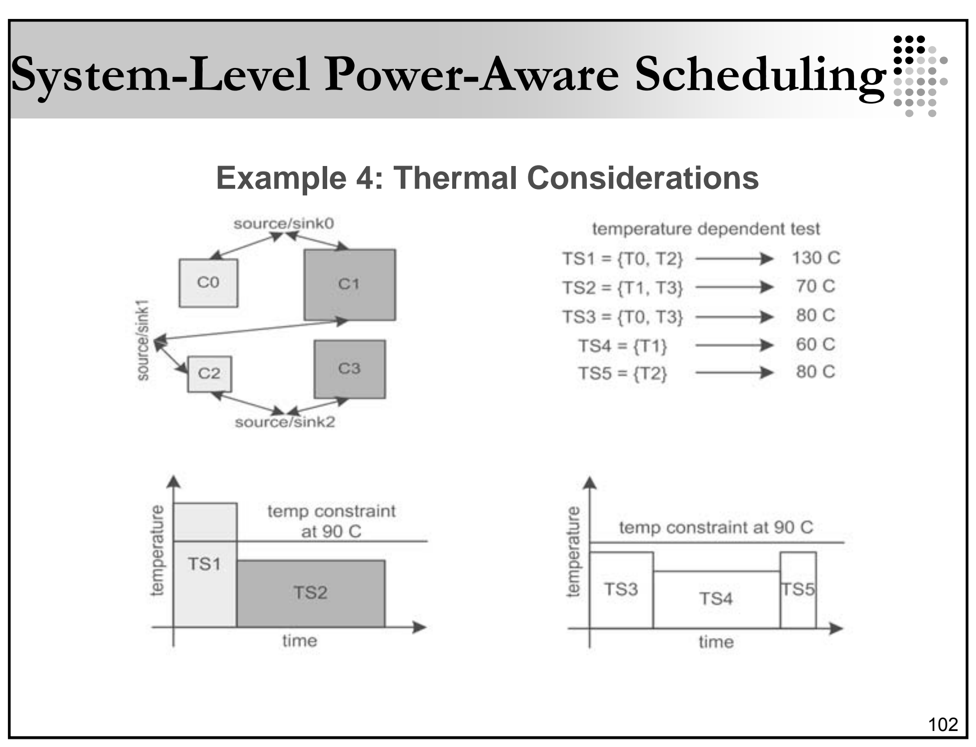
98


System-Level Power-Aware Scheduling
Example 1: Resource Allocation and Incompatibility Graphs
source/sink0
C0
C1
source/sink1
C2
C3
source/sink2
resource allocation graph
R0
R1
R2
T0
T1
T2
T3
test sessions/test time
{T0, T2}
{T1, T3}
0.5s
0.3s
0.8s
0.3s
test incompatibility graph
T0
T1
T2
T3
(source: R. Chou et al., IEEE Trans. on VLSI, Vol. 5, No. 2, pp. 175-185, 1997)
99

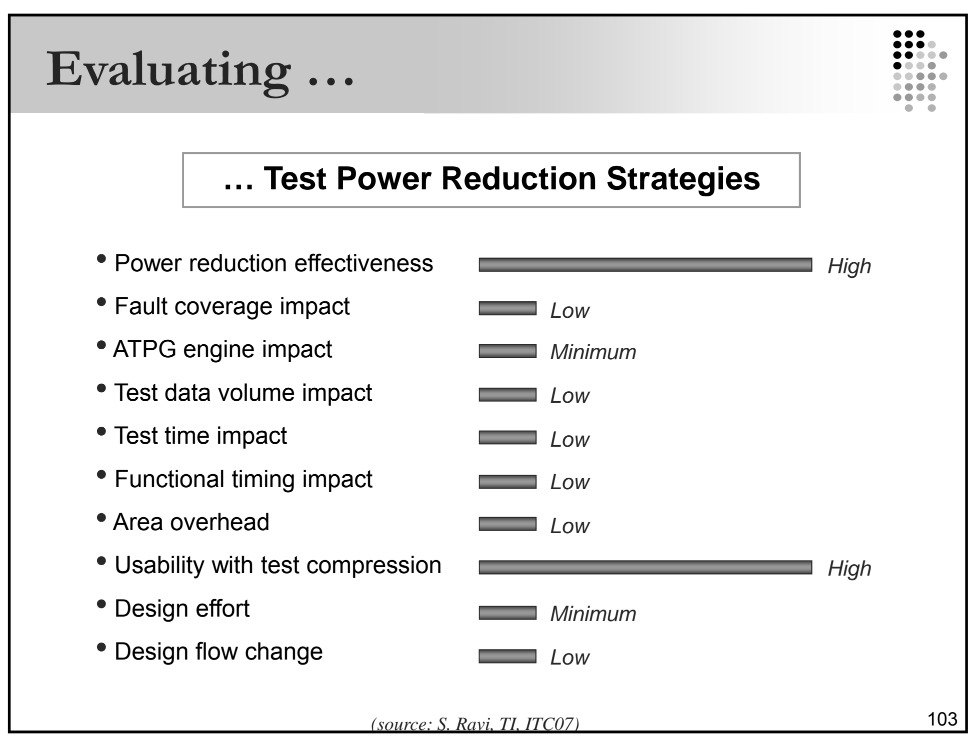

System-Level Power-Aware Scheduling
Example 2: Power Model and Test Schedule
peak power
power
time
test power
{T0, T2}
{T1, T3}
5W
3W
12W
2W
power constraint at 15 W
T3
T2
T1
T0
power constraint at 13 W
T2
T1
T0
T3
100



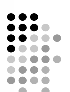
System-Level Power-Aware Scheduling
Example 3: Power Profile Manipulation
peak power 1
peak power 2
power
time
test power
T1
12W for 0.3s
6W for 0.5s
Power profile can be modified by pattern modification and/or test set reordering
power constraint at 13 W
T2
T3
T0
T1
101



System-Level Power-Aware Scheduling
Example 4: Thermal Considerations
source/sink0
C0
C1
source/sink1
C2
C3
source/sink2
temperature dependent test
TS1 = {T0, T2} → 130 C
TS2 = {T1, T3} → 70 C
TS3 = {T0, T3} → 80 C
TS4 = {T1} → 60 C
TS5 = {T2} → 80 C
temperature
temp constraint at 90 C
TS1
TS2
time
temp constraint at 90 C
TS3
TS4
TS5
102



Test Power Estimation



- Needed for test space exploration (DfT/ATPG) early in the design cycle
- Availability of scan enhanced design and ATPG patterns only at the gate level in today's design flows imposes the usage of gate-level estimators for test power
- Conventional flow adopted to perform estimation is simulation-based
- Estimation is performed at various PVT corners
- Challenges for multi-million gate SoCs
  - Time-consuming !!
  - Dump sizes can be very large !!
- The weighted transition metric (WSA) is quick but approximate

Faster and low cost solutions for test power estimation are needed !

104

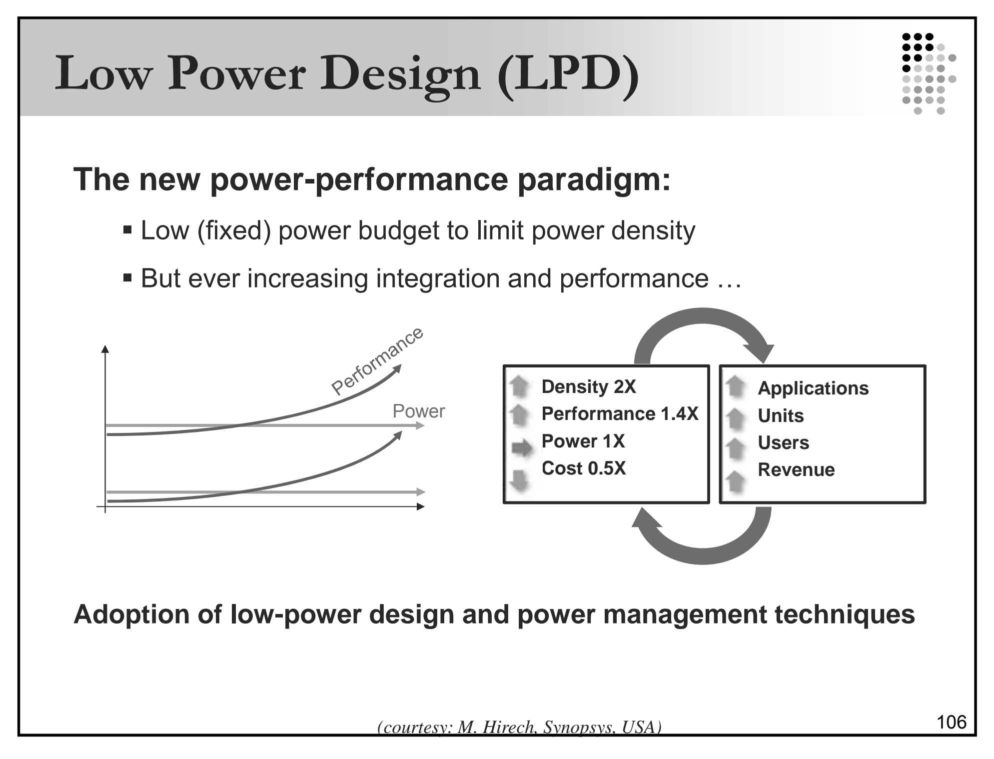
Low Power Design (LPD)

Power Consumption Trends

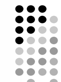
- Exponential growth in transistor density
  - More functionality
- But linear reduction in supply voltage
  - Not adequate to prevent power density to increase

(source: Tirimurti et al., DATE, 2004)

105



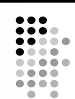
Low Power Design (LPD)



System & Architecture	IC Design & Implementation
▪ Voltage / Frequency Scaling ▪ Architecture (parallel, well managed pipeline, etc.) ▪ Others (H/S partitioning, instruction set, algorithms, etc.)	▪ Clock Gating ▪ Multiple Supply Voltage ▪ Multiple Threshold Voltage ▪ Substrate-Bias ▪ Power Gating ▪ Others
Circuit (Logic) Design	**Process Technology**
▪ Low Power Cell Library ▪ Gate sizing (to equalize paths) ▪ Buffer insertion to reduce slew ▪ Logic restructuring to avoid hazards ▪ Memory Bit Cell and Compiler ▪ Others	▪ Reduce Vdd ▪ Threshold Voltage Option ▪ Low Capacitance Dielectric ▪ New Gate Oxide Material ▪ Transistor Sizing ▪ Others

107

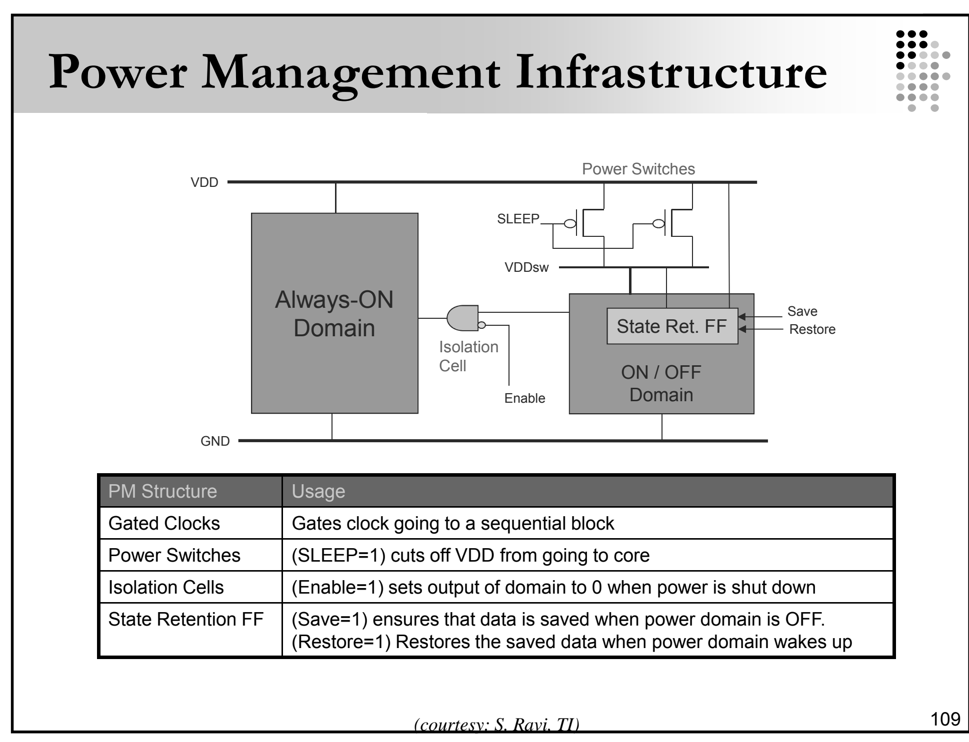
Low Power Design (LPD)



Main LPD techniques	Power reduction	
	Dynamic	Leakage
Clock gating	✓	
Power gating	✓	✓
Multi-Voltage domains	✓	
Multi-Threshold cells		✓

These techniques are often combined together to achieve the maximum power optimization value

108



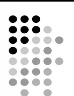
Power Management Infrastructure

PM Structure	Usage
Gated Clocks	Gates clock going to a sequential block
Power Switches	(SLEEP=1) cuts off VDD from going to core
Isolation Cells	(Enable=1) sets output of domain to 0 when power is shut down
State Retention FF	(Save=1) ensures that data is saved when power domain is OFF. (Restore=1) Restores the saved data when power domain wakes up

(courtesy: S. Ravi, TI)

109

Power Specification Formats



- Need of specifying properties of a circuit block w.r.t. power dissipation during design, verification and implementation
- Interpreted by designers and design automation tools
- To achieve a unified and efficient design flow, various EDA tools need to use a common format
    - *Common Power Format* (CPF) created by Cadence
    - *Unified Power Format* (UPF) supported Synopsys, Mentor and Magma and standardized by IEEE (P1801 std. working group)
- 90% same concepts, but different syntaxes
- Both formats are based on the *Tool Control Language* (TCL) embedded in most EDA tools

110

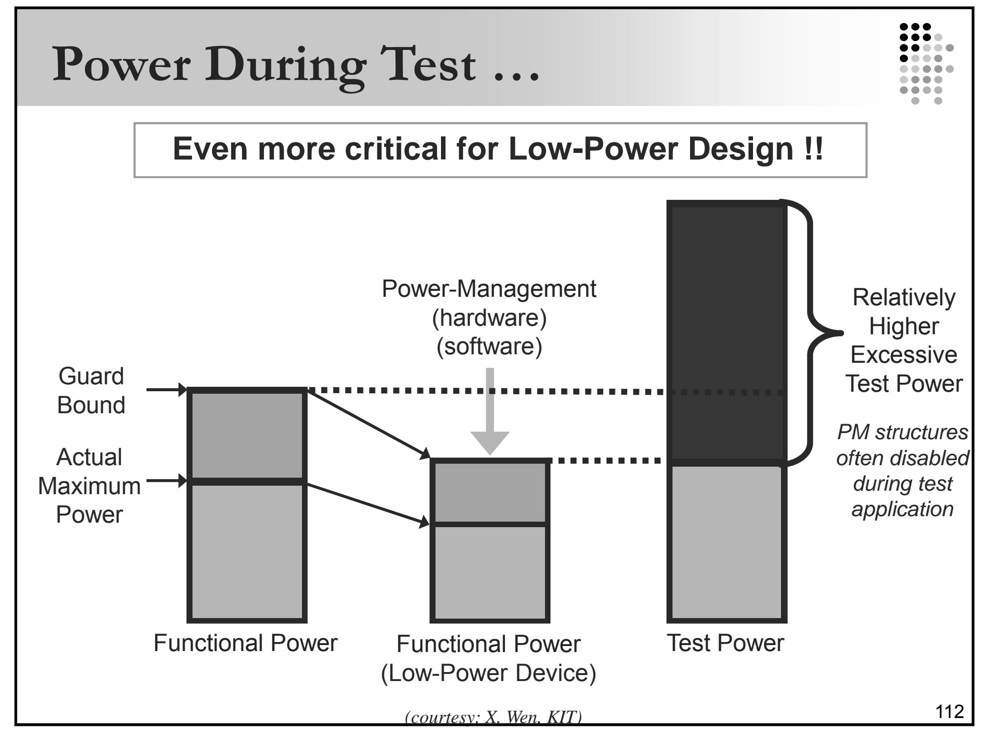
Power Specification Formats

- Used to describe the following specifications:
  - Voltage domains, Power domains, Isolation logic, Retention registers, Always-on cells, Power switches
  - The various power modes also need to be specified
  - Operating environment details (process, temperature, operating voltage data, and leakage calculation) are not part of UPF
  - UPF-based low power design flow →
- Example: creation of power domains

```
create_power_domain pdTOP
create_power_domain pd1 –elements U1
create_power_domain pd2 –elements U2
create_power_domain pd3 –elements U3
```

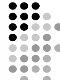

111

Power During Test …



112

Requirements for Test of LPD



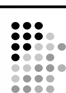
- Reduce (even more) test power by using the power management (PM) infrastructure (and/or applying the previous dedicated solutions)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures

And still target:

High fault coverage, short test application time, small test data volume, low area overhead, etc … while making test power dissipation (dynamic and leakage) comparable to functional power

113

Reducing Test Power of LPD



Main classes of dedicated solutions

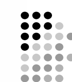
- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

Objective (again)

Make test power dissipation comparable to functional power

114

Reducing Test Power of LPD

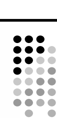


Main classes of dedicated solutions

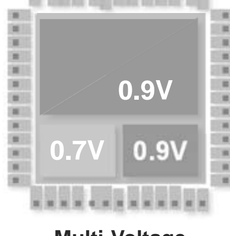
- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

115

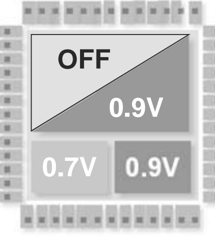
Test for Multi-Voltage Designs



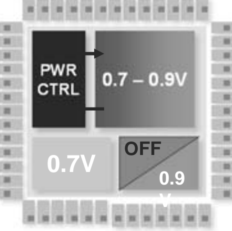
Multi-Voltage Design Styles



Multi-Voltage Multi-supply



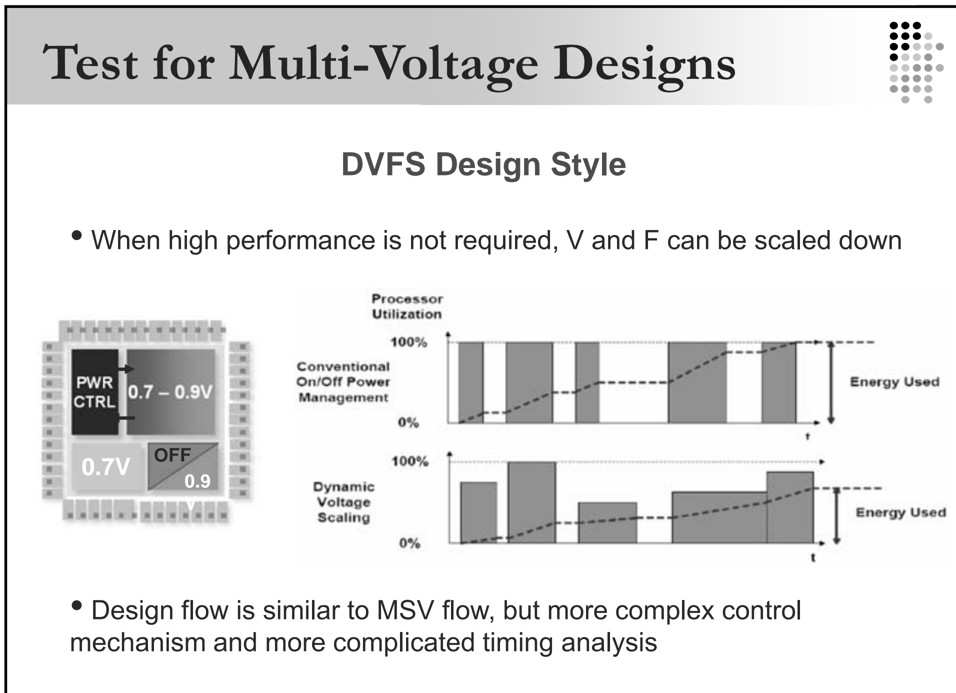
Multi-Voltage with power gating



Dynamic Voltage Frequency Scaling (DVFS)

- Creation of “power islands”
- Vdd scaling results in quadratic power reduction ($P=kCV^2f$)
- Level shifters to let signals cross power domain boundaries

116



Test for Multi-Voltage Designs

Example 1: Multi-Voltage Aware Scan Cell Ordering

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93%)

Design (1.2V)

Scan Cell

Block A 0.9V	Block B 1.2V	Block C 0.9V
A1, A2, A3	B1, B2, B3	C1, C2, C3

Scan chain assembly

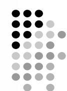
Position \ Ordering	Logical	Physical	Multi-Voltage
1	A1	A2	A2
2	A2	A1	A1
3	A3	A3	A3
4	B1	B3	C1
5	B2	B1	C2
6	B3	B2	C3
7	C1	C1	B2
8	C2	C2	B3
9	C3	C3	B1

Level shifter

- Presented by Synopsys in JOLPE vol.1 n° 1 April 2005 and implemented in Synopsys Galaxy™ Test

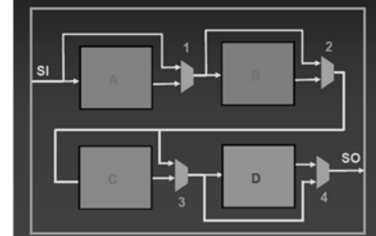
118

Test for Multi-Voltage Designs



Example 2: Power-Aware Scan Chain Assembly

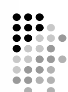
- Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints
- Bypass multiplexers allow testing of specific power domains in MSMV environment (switched-off power domains are bypassed)
- Preserve test functionality !



- Presented by Cadence @ ITC 2008
  and implemented in Cadence *Encounter*^{TM}

119

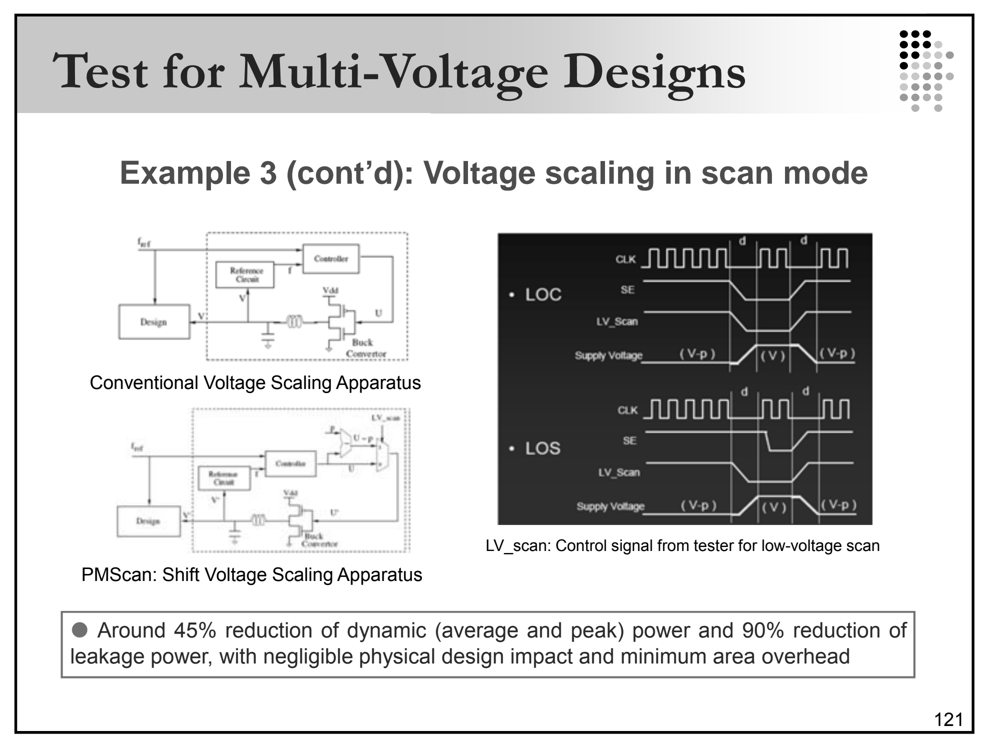
Test for Multi-Voltage Designs

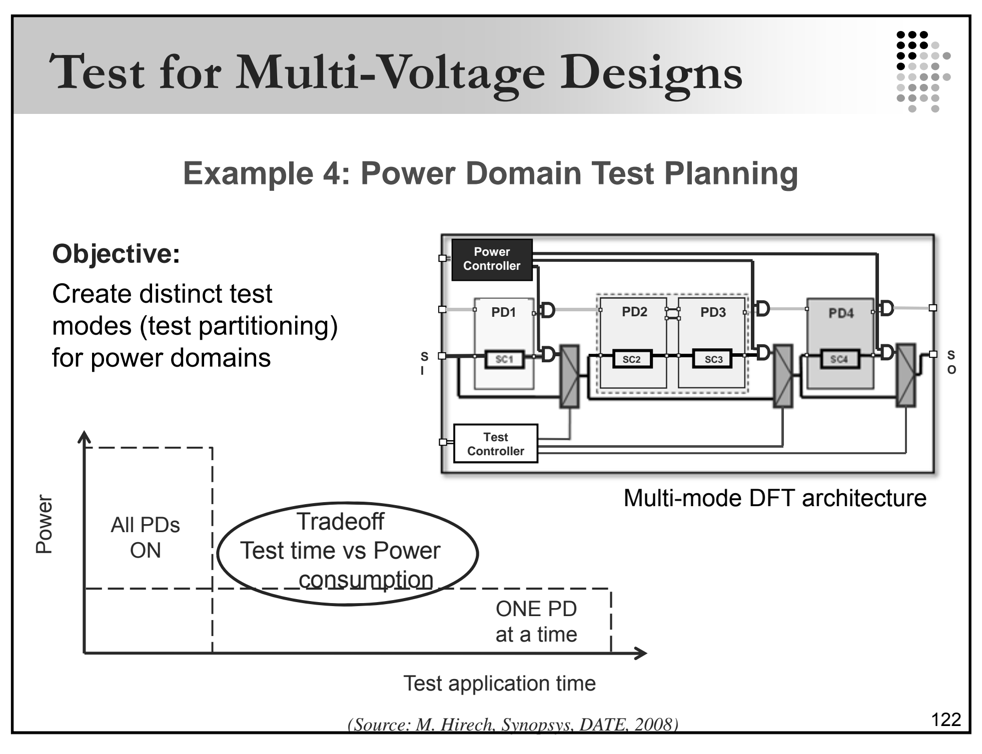


Example 3: Voltage scaling in scan mode

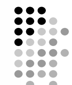
- During scan shifting, the combinational logic needs not meet timing
- Goal: re-use the DVS infrastructure in test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
- At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
  - Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan FFs (V_t) = 0.35 V
  - If shift frequency (F_{shift}) = 125 MHz → V_{shift} = 0.635 V is enough !
- Presented by TI @ ITC 2007

120


Test for Multi-Voltage Designs
Example 3 (cont'd): Voltage scaling in scan mode
Conventional Voltage Scaling Apparatus
PMScan: Shift Voltage Scaling Apparatus
LOC
LOS
CLK
SE
LV_Scan
Supply Voltage
(V-p)
(V)
LV_scan: Control signal from tester for low-voltage scan
Around 45% reduction of dynamic (average and peak) power and 90% reduction of leakage power, with negligible physical design impact and minimum area overhead
121

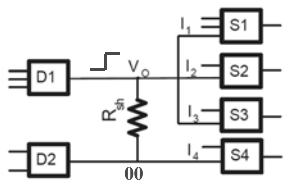

Test for Multi-Voltage Designs
Example 4: Power Domain Test Planning
Objective:
Create distinct test modes (test partitioning) for power domains
Power Controller
PD1
PD2
PD3
PD4
SC1
SC2
SC3
SC4
Test Controller
Multi-mode DFT architecture
Power
All PDs ON
Tradeoff
Test time vs Power consumption
ONE PD at a time
Test application time
(Source: M. Hirech, Synopsys, DATE, 2008)
122

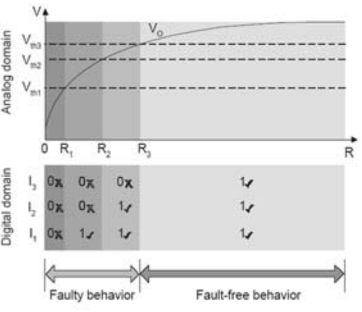
Test for Multi-Voltage Designs



Example 5: Test for MV Design – Bridge Defects

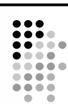
- **Bridge defects**
  - Most of them are resistive
  - Hard-shorts ~ stuck-at faults → detection is independent of Vdd
- **Resistive bridge defects**
  - A finite number of discrete intervals can be used to deal with all bridge R_{sh} values





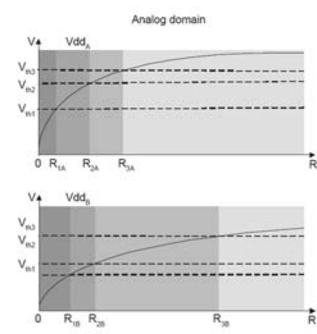
123

Test for Multi-Voltage Designs



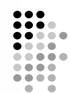
Example 5: Test for MV Design – Bridge Defects

- **Resistive bridge behavior at MV settings**
  - Voltage Vo does not scale linearly with the input threshold voltage of S1, S2 and S3 when changing Vdd
  - Resistance intervals differ from one voltage setting to another
  - Example: a bridge with $R_{sh} = R_{3B}$ will cause a logic fault at V_{ddB} but not at V_{ddA}
  - A test pattern targeting a particular logic fault will detect different ranges of defects at different MV settings



124

Test for Multi-Voltage Designs



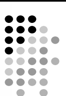
Example 5: Test for MV Design – Bridge Defects

- **Goal of test generation for MV settings**
  - Generate test patterns for MV settings to maximize coverage of Resistive Bridging Faults (RBF) while minimizing test sequence length
  - Identification of Vdd specific test patterns for a given fault f
  - Example*: for a given circuit, 621 test patterns are needed at three Vdd settings with a commercial tool (207 at each Vdd), while only 391 test patterns applied at two Vdd settings (0.8V and 1.2V) are needed with the proposed technique (to achieve 100% fault coverage)

(source: U. Ingelson et al., ATS, 2007)

125

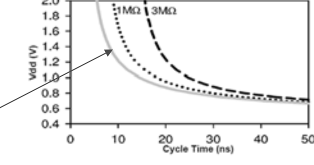
Test for Multi-Voltage Designs



Example 6: Test for MV Design – Open Defects

- **Open defects**
  - Due to unconnected nodes
  - Full opens → logic failures tested using static faults
- **Transmission gate opens**
  - Better detectability at low Vdd settings *(N. Zain Ali et al., ETS, 2006)*
- **Interconnect resistive opens**
  - Resistive opens → time-dependent → tested using delay tests
  - Better detectability at elevated Vdd settings *

(B. Kruseman et al., DATE, 2006)*



Longest path in the fault-free design

126

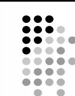
Reducing Test Power of LPD

Main classes of dedicated solutions

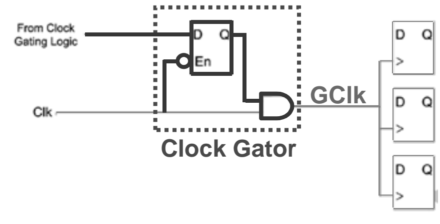
- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

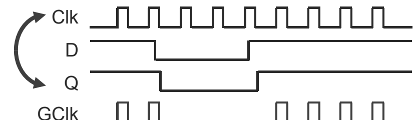
127

Test for Gated Clock Designs



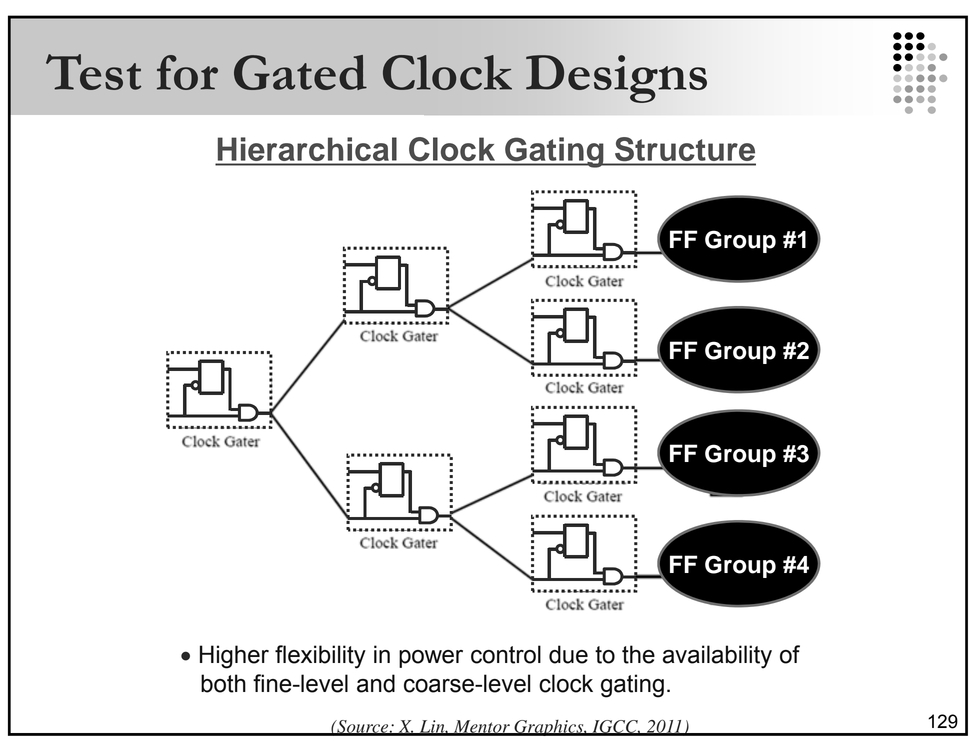
Basic Clock Gating Design

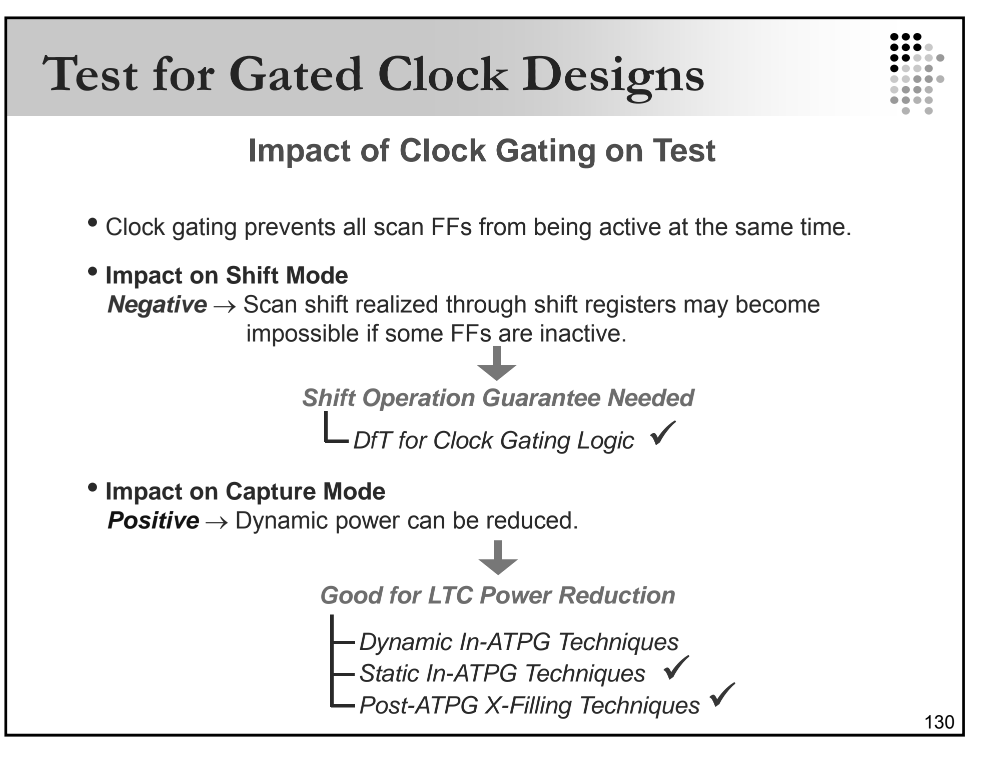




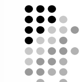
- Not all FFs need to be triggered to perform a function (e.g., the camera control logic in a mobile-phone SoC can be inactive during a call).
- Gating-off the clock to functionally-noncontributing FFs reduces dynamic power dissipation, *not only in logic portions but also in clock trees (> 50%)*.
- One of the major techniques for reducing functional power.
- Widely adopted and supported by existing EDA tools.

128


Test for Gated Clock Designs
Hierarchical Clock Gating Structure
Clock Gater
FF Group #1
FF Group #2
FF Group #3
FF Group #4
• Higher flexibility in power control due to the availability of both fine-level and coarse-level clock gating.
(Source: X. Lin, Mentor Graphics, IGCC, 2011)
129

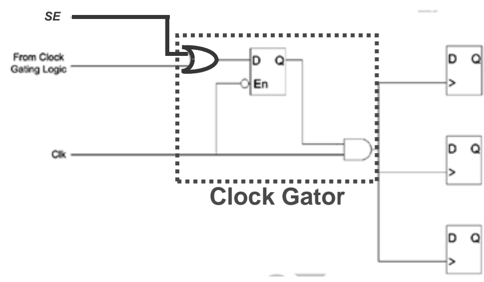

Test for Gated Clock Designs
Impact of Clock Gating on Test
• Clock gating prevents all scan FFs from being active at the same time.
• Impact on Shift Mode
Negative → Scan shift realized through shift registers may become impossible if some FFs are inactive.
Shift Operation Guarantee Needed
DfT for Clock Gating Logic ✓
• Impact on Capture Mode
Positive → Dynamic power can be reduced.
Good for LTC Power Reduction
Dynamic In-ATPG Techniques
Static In-ATPG Techniques ✓
Post-ATPG X-Filling Techniques ✓
130

Test for Gated Clock Designs



Example 1: DfT for Clock Gating Logic

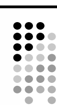
- **Shift Mode** (*SE* = 1): All scan FFs must be active to form one or more shift registers to shift-in test stimuli / shift-out test responses. Clock gating logic needs to be overridden (by *SE*) in shift mode.
- **Capture Mode** (*SE* = 0): Scan FFs are allowed to be controlled by clock gating logic. Nothing needs to be done.



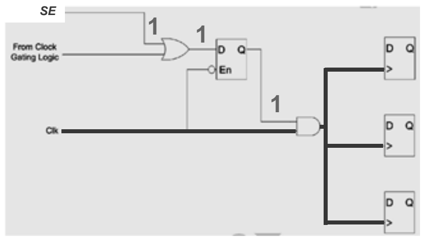
- Automatically implemented by commercial DfT tools.

131

Test for Gated Clock Designs



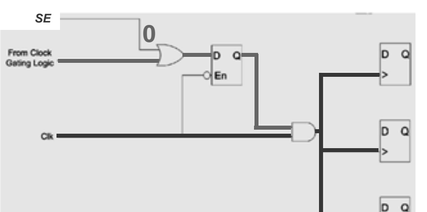
Example 1 (cont'd): DfT for Clock Gating Logic



- Disable clock gating in ***shift mode*** (*SE* = 1): Unconditionally-ON Clock

  ↓

  Shift Register Operation



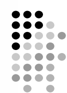
- Enable clock gating in ***capture mode*** (*SE* = 0): Conditionally-ON Clock

  ↓

  LTC Power Reduction

132

Test for Gated Clock Designs



Example 2: LTC Power Reduction by Clock Gating

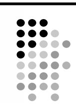
Static In-ATPG Technique 1

- A **default value** is a value to be assigned to an input in order to gate-off a clock.
  - ➔ *A preset value is to be used to fill an X-bit in a test cube.*
- Flow for obtaining default values for clock gating:
  - ➔ *Identify all clock gators.*
  - ➔ *For each clock gator, calculate a set of input settings that set the clock off.*
  - ➔ *The values in each input setting are default values.*
- Flow for using default values for clock gating:
  - ➔ *Generate a test cube for fault detection.*
  - ➔ *Assign default values to the X-bits in the test cube.*
    (*If there are multiple choices of default values, use the one that can turn-off more FFs.*)

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

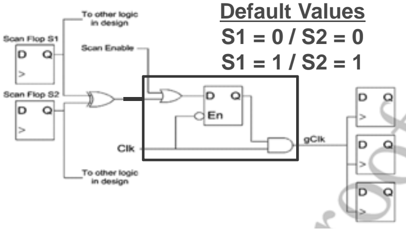
133

Test for Gated Clock Designs



Example 2 (cont'd): LTC Power Reduction by Clock Gating

Static In-ATPG Technique 1



Default Values
S1 = 0 / S2 = 0
S1 = 1 / S2 = 1

Test Cubes after ATPG

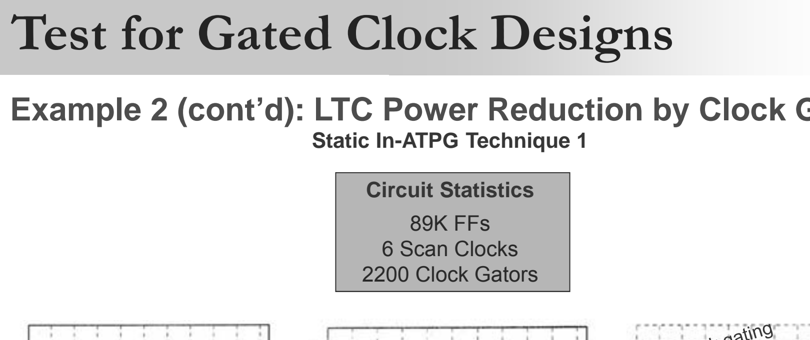
Test Cubes	Scan flops in design					
	S0	S1	S2	S3	S4	S5
T1	X	0	X	1	0	X
T2	0	1	X	X	X	0
T3	X	X	0	1	0	X

Test Cubes after Assigning Default Values
(S1=0 / S2=0)

Test Cubes	Scan flops in design						Merge "default values"?
	S0	S1	S2	S3	S4	S5	
T1	X	0	0	1	0	X	Yes
T2	0	1	X	X	X	0	Conflict
T3	X	0	0	1	0	X	Yes

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

134

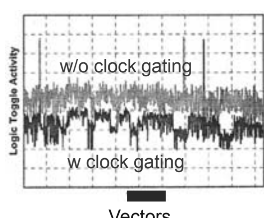


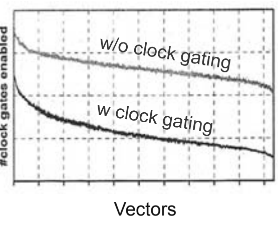
Test for Gated Clock Designs

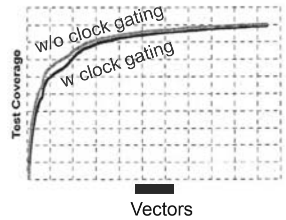
Example 2 (cont'd): LTC Power Reduction by Clock Gating

Static In-ATPG Technique 1

Circuit Statistics
89K FFs
6 Scan Clocks
2200 Clock Gators





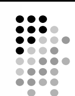


- The number of active clocks are reduced by more than 50%.
- LTC toggle activity is reduced by 35%.
- Fault coverage and test set size remain almost unchanged.

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

135

Test for Gated Clock Designs



Example 3: LTC Power Reduction by Clock Gating

Static In-ATPG Technique 2

Before Test Generation

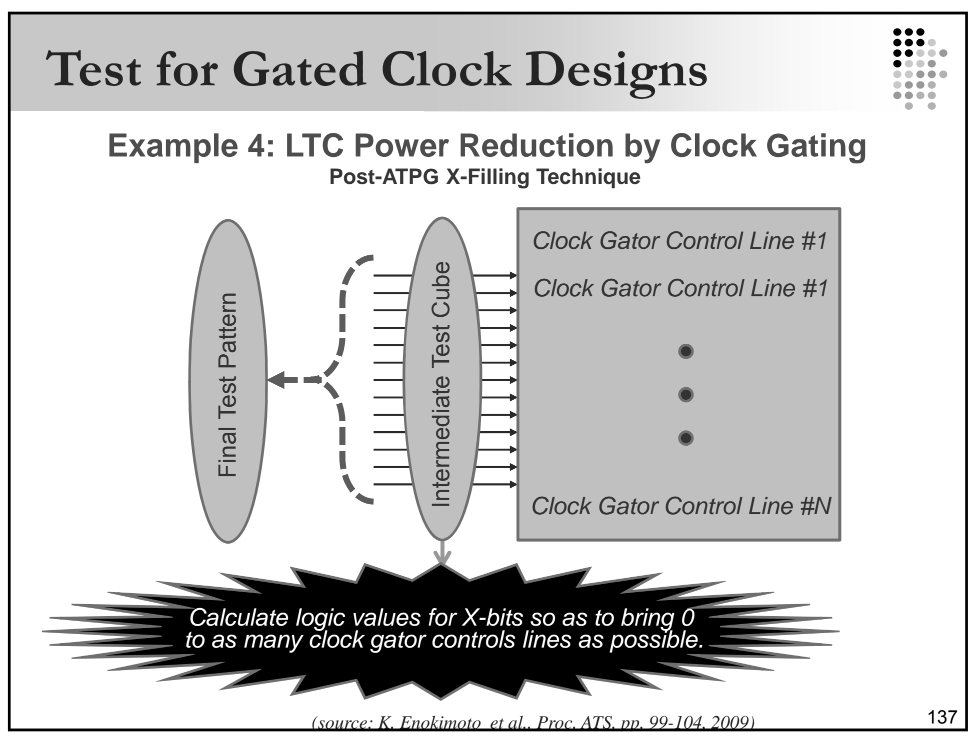
- Conduct structural analysis to identify all clock gators for each clock.
- Obtain ***clock control cubes*** (***CCCs***).
  - ➔ *A CCC is a combination of 0s, 1s, and Xs that disables one or more clock gators.*
- Order CCCs by the decreasing number of FFs that a CCC turns off.

During Test Generation

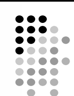
- Generate a test cube for detecting one or more faults.
- Merge the test cube with all compatible CCCs in the determined order.

(source: D. Czysz et al., Proc. ITC, Paper 13.2, 2008)

136



Test for Gated Clock Designs

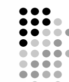


Summary

- Functional clock gating is indispensable in reducing dynamic power.
- Functional clock gating logic needs to be modified in order to guarantee correct operation in *shift mode*.
- Clock gating can be used in *capture mode* to reduce LTC power.
  - ➔ Static In-ATPG Techniques
    (*Assign pre-determined clock-gator disabling values to don't-care bits (X-bits) in a test cube initially generated for fault detection.*)
  - ➔ Post-ATPG X-Filling Techniques
    (*Find and assign proper logic values to don't-care (X-bits) in a test cube so as to disable as many clock gators as possible.*)

138

Reducing Test Power of LPD



Main classes of dedicated solutions

- Test for Multi-Voltage Designs
- Test for Gated Clock Designs
- Test for Power Management (PM) Structures

139

Test for Power Management Structures

Typical Power Management (PM) Structures

Power Control Logic ① Power Switch ② ✓ Isolation Cell ④ ✓

External Power Supply
On/Off VDD1 VDD1 VDD2
iso_enable
ack
req
Power Switch
PD1
ISO
PD2 Always ON
LS
Chip Level
Power Controller
stop_clock, save, restore
ack
RR
ELS
PD3 Always ON
PD_TOP Always ON domain
PD1, PD2, PD3, PD_TOP: power domains
ISO: Isolation cell; ELS: Enabled level shifter cell
LS: Level shifter cell; RR: Retention register

State Retention Register ③ ✓ Level Shifter ⑤ ✓

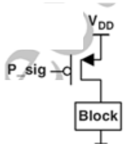
- Conditionally turning on or off power domains) to reduce dynamic and static power.
- Can be described in UPF (*Unified Power Format*) or CPF (*Common Power Format*).
- PM structures (①~⑤) require dedicated DfT methods and test patterns.

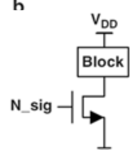
140

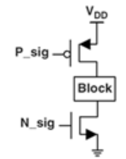
Test for Power Management Structures

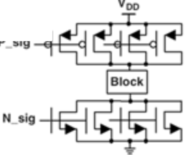
Example 1: Test for Power Switches

Header Switch | **Footer Switch** | **Symmetric Switch** | **Segmented Switch**









Header Switch / Footer Switch / Symmetric Switch

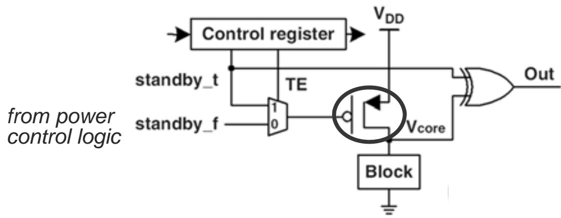
- Also called sleep transistors and used to shut down blocks (power domains) that are not in use (idle mode), hence reducing leakage power and dynamic power.
- Should be large enough to provide sufficient current to the circuit.

Segmented Switch

- Individual switch transistors can be small.
- Preferable in practice due to concerns about layout, design for manufacturability, and limiting inrush current when switching on a power domain.

Test for Power Management Structures

Example 1 (cont'd): Test for Power Switches

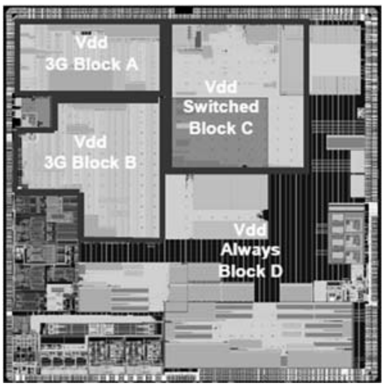


- Pattern 1 (*Test for Short*): *TE* = 1 / *standby_t* = 1
  ➔ Turn-off the power switch. After sufficient discharge, Vcore should be much lower than VDD, and thus *Out* (fault-free) = 1 / *Out* (faulty) = 0
- Pattern 2 (*Test for Open*): *TE* = 1 / *standby_t* = 0
  ➔ Turn-on the power switch. Vcore should be close to VDD, and thus *Out* (fault-free) = 1 / *Out* (faulty) = 0

(source: Goal et al., Proc. ETS, pp. 145-150, 2006)

Test for Power Management Structures

Example 2: Parametric Test of Micro Switches

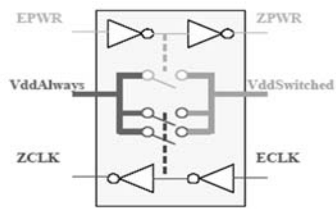


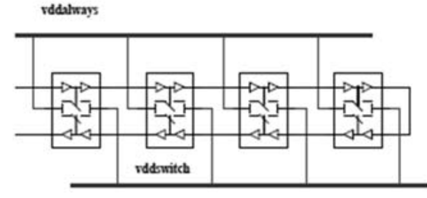
- Presented by ST-Ericson (Sophia) at International Test Conference 2008.
- Sigle-die 3G mobile phone base band Chip fabricated in 65nm technology.
- Includes multimedia features, such as video decoder, MP3 player, camera, games, and designed to be extremely low power.
- Rush current during power up → specific functional mode → test mode has to map functional mode !

143

Test for Power Management Structures

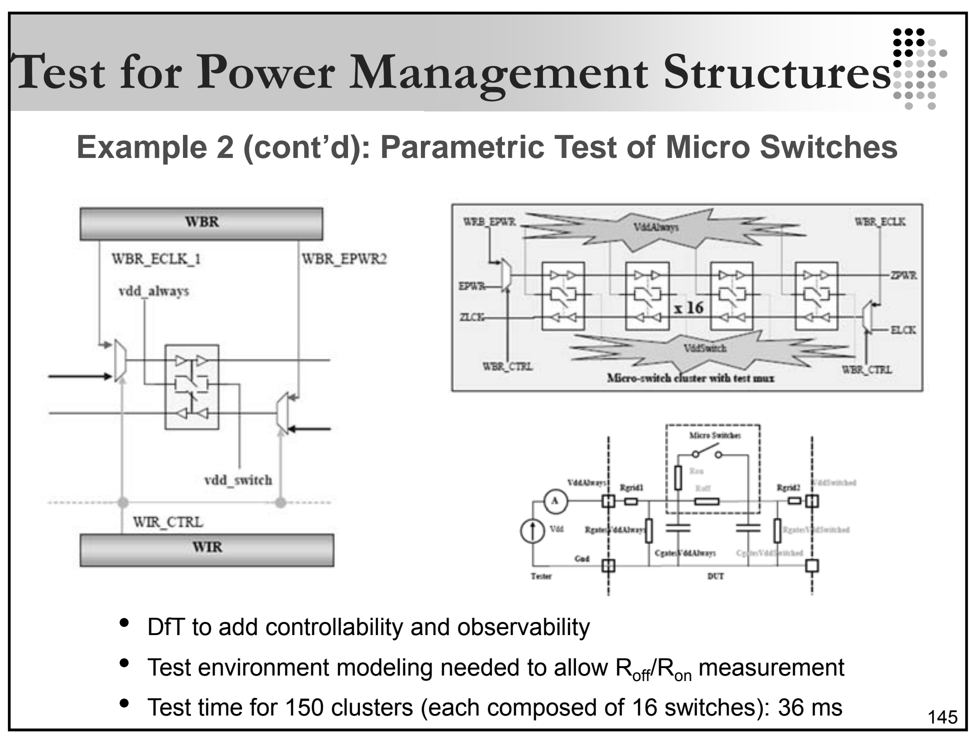
Example 2 (cont'd): Parametric Test of Micro Switches

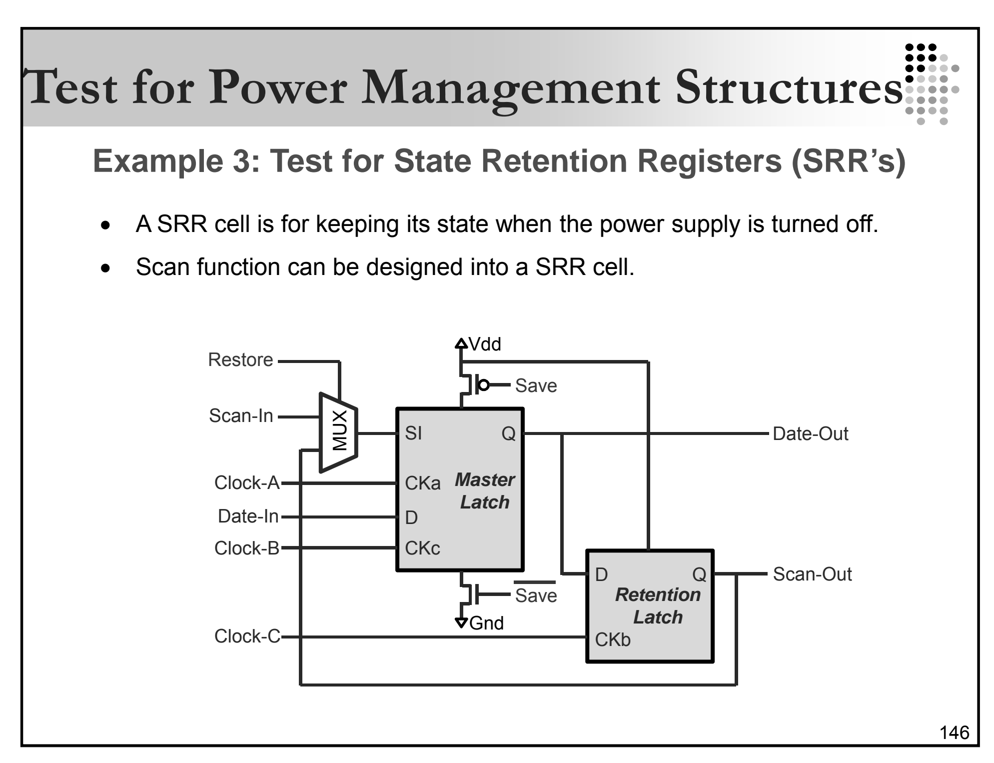




- The micro switches are daisy-chained. First, all the EPWR control signals are propagated in the chain. This gives a progressive ramp-up of the VddSwitched. Then, the ECLK control signal follows, turning 'on' all the transistors of the micro switches.
- Testing micro-switches individually is needed to detect resistive defects in each of them, and testing the micro switches' control chain is important to ensure the chain is not broken.

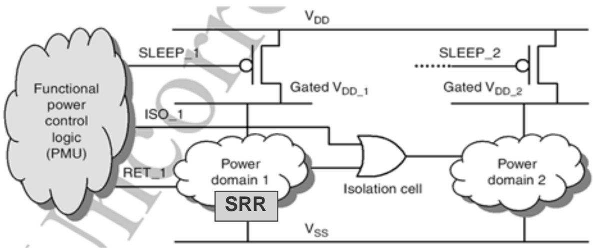
144


Test for Power Management Structures
Example 2 (cont'd): Parametric Test of Micro Switches
WBR
WBR_ECLK_1
WBR_EPWR2
vdd_always
vdd_switch
WIR_CTRL
WIR
x 16
Micro-switch cluster with test mux
• DfT to add controllability and observability
• Test environment modeling needed to allow R_{off}/R_{on} measurement
• Test time for 150 clusters (each composed of 16 switches): 36 ms
145


Test for Power Management Structures
Example 3: Test for State Retention Registers (SRR's)
• A SRR cell is for keeping its state when the power supply is turned off.
• Scan function can be designed into a SRR cell.
Vdd
Save
Restore
Scan-In
MUX
SI
Q
Date-Out
Clock-A
CKa
Master
Latch
Date-In
D
Clock-B
CKc
Save
Gnd
D
Q
Retention
Latch
CKb
Scan-Out
Clock-C
146

Test for Power Management Structures

Example 3 (cont'd): Test for State Retention Registers (SRR's)



Retention Capability Test

(1) Shift-in value *V* to SRR.
(2) Enable retention by setting *Save* to 1.
(3) Enable the isolation cell.
(4) Turn-off Power Domain 1.
(5) Turn-on Power Domain 1 after a few cycles.
(6) Disable the isolation cell.
(7) Disable retention by setting *Restore* to 1.
(8) Shift out the value of SRR and check if it is *V*.

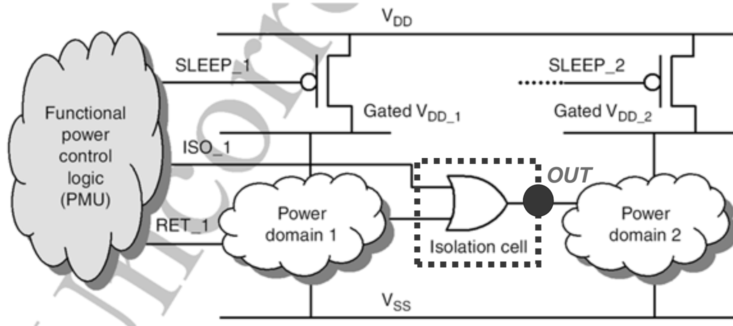
Repeat for V = 0 and V = 1

Other tests, such as test for retention robustness to the state element's clock, asynchronous set/reset, etc., may also need to be applied.

147

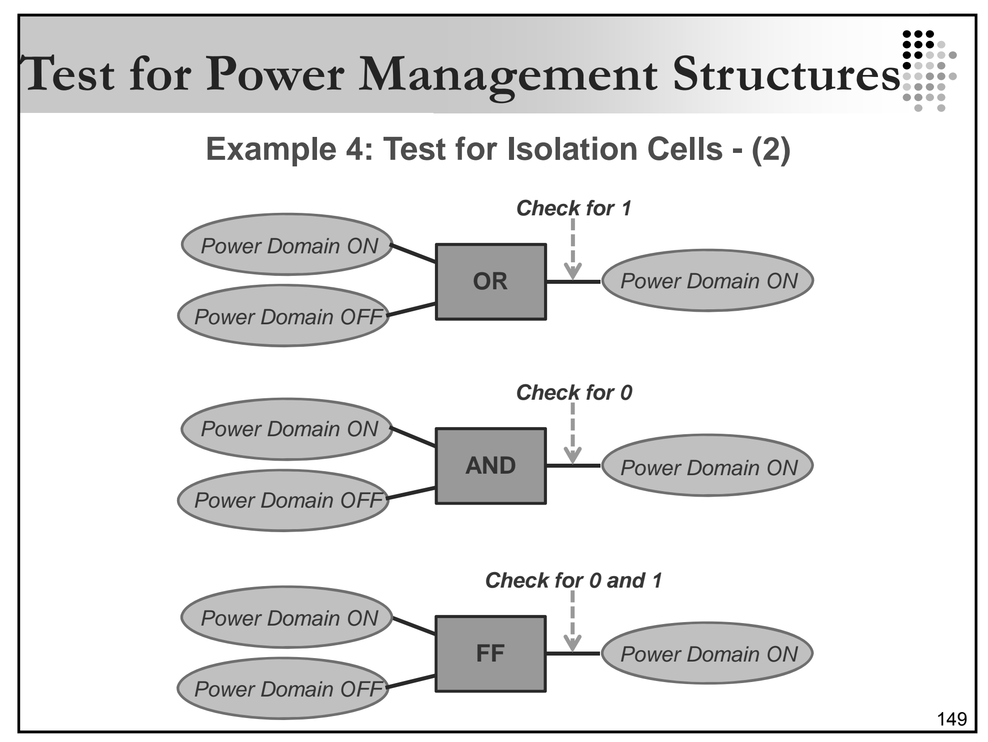
Test for Power Management Structures

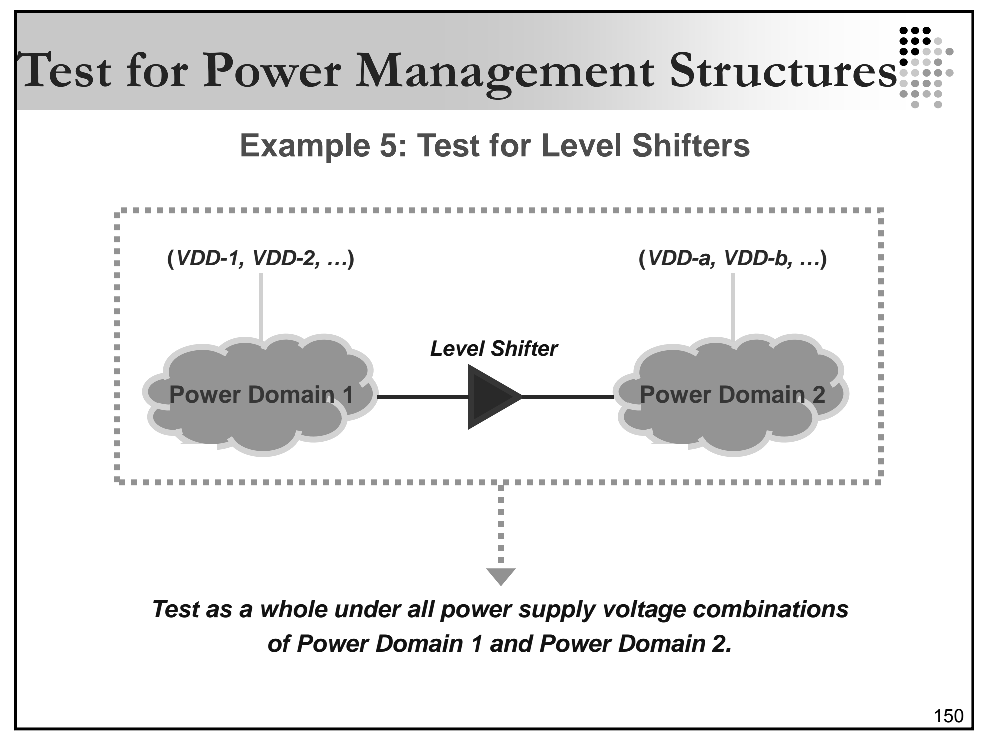
Example 4: Test for Isolation Cells - (1)

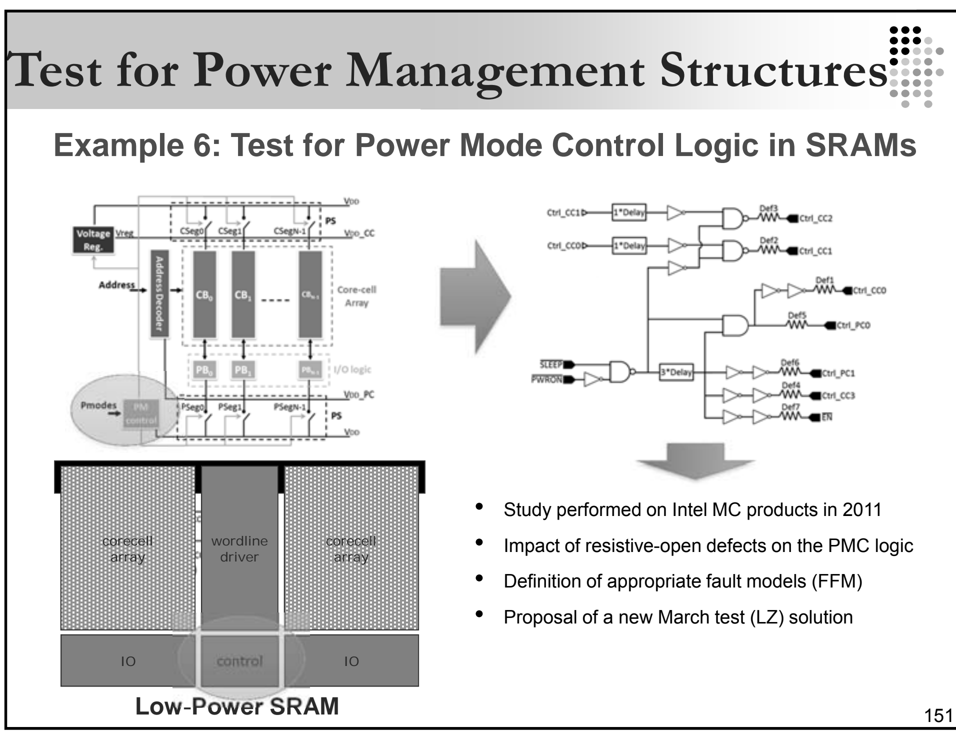


(1) Turn-off Power Domain 1 (*SLEEP_1* = 1).
(2) Turn-on Power Domain 2 (*SLEEP_2* = 0).
(3) Set 1 to *ISO_1* and check if the isolation cell output (*OUT*) is 1.

148


Test for Power Management Structures
Example 4: Test for Isolation Cells - (2)
Check for 1
Power Domain ON
Power Domain OFF
OR
Power Domain ON
Check for 0
Power Domain ON
Power Domain OFF
AND
Power Domain ON
Check for 0 and 1
Power Domain ON
Power Domain OFF
FF
Power Domain ON
149


Test for Power Management Structures
Example 5: Test for Level Shifters
(VDD-1, VDD-2, …)
(VDD-a, VDD-b, …)
Level Shifter
Power Domain 1
Power Domain 2
Test as a whole under all power supply voltage combinations
of Power Domain 1 and Power Domain 2.
150



Test for Power Management Structures

Summary

- More and more power management structures are used in various IC designs in order to reduce power (dynamic and static) dissipation.
- Conventional ATPG does not target power management structures, leading to potential quality problems.
- There is a strong need to fully understand the basics of various power management structures and their operation modes.
- Special considerations and even new algorithms are needed to fully test various power management structures.

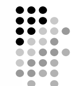
— Clock Gating Logic (Clock Gator, Control Logic)

— Power Gating Logic
- → PMU (Power Management Unit)
- → Power Switch
- → State Retention Register, Isolation Cell, Level Shifter

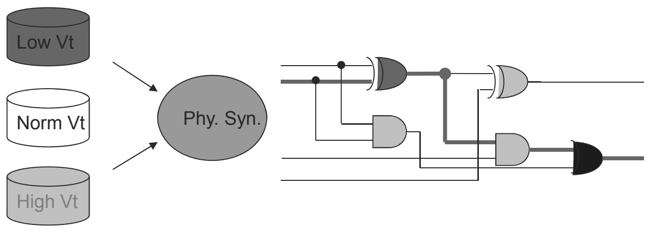
— Power Distribution Network

152

Impact of MTV Design on Test



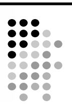
- Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction → speed cost to decrease leakage !!
- MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)
- Leakage power reduction while meeting timing and no area overhead
- Well established and supported by existing EDA tools



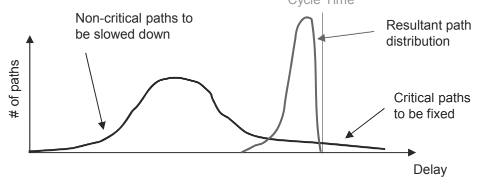
(source: CADENCE, 2007)

153

Impact of MTV Design on Test



- By using such power optimization techniques, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations
  - PDF selection more complex
  - More test data are needed
  - Sensitivity to variations

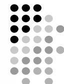


- PSN has a significant impact on the timing behavior
  - Need to integrate PSN effects in delay test pattern generation

Solutions for high quality at-speed fault coverage are needed !

154

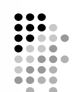
Power-Aware DFT Tools



- **Synopsys:**
  - Galaxy™ Test is a comprehensive test automation solution.
  - DFT Compiler and its low power features (for more details on this tools, see "Power and Design for Test: A Design Automation Perspective", A. De Colle et al, Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, April 2005)
  - DFT MAX and its low power features (for more details on this tools, see "DFT MAX and Power", R. Kapur et al, Journal of Low Power Electronics (JOLPE), Vol. 3, N° 2, August 2007)
  - TetraMAX® - power-aware test patterns for defect detection
  - Details http://www.synopsys.com/Tools/Implementation/RTLSynthesis/Test/Pages/default.aspx

155

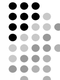
Power-Aware DFT Tools



- **Mentor:**
  - Tessent™ FastScan™ and Tessent™ TestKompress™ provide comprehensive low-power and power-aware test solutions.
  - Details at http://www.mentor.com/products/silicon-yield/logic_test/
- **Cadence:**
  - Encounter® Test, a key technology in the Cadence® Encounter digital IC design platform
  - To support manufacturing test of low-power devices, Encounter Test uses power intent information to create distinct test modes automatically for power domains and shut-off requirements.
  - Details http://www.cadence.com/products/ld/test_architect/pages/default.aspx

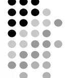
156

Conclusion



- Power consumption during Test is a real issue !!
- Not only during manufacturing test but also during on-line test
- Not only ATPG and DFT but also BIST, test compression, and test scheduling have been addressed
- No generic solution, but rather a combination of solutions. Example: power-aware DfT for reducing shift power and power-aware ATPG for reducing LTC power
- New test solutions for Low-Power Design that preserve test functionality are needed !!

157



Thank You !

158