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Power-Aware Testing and Test Strategies for Low Power Devices

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Power-Aware Testing and Test Strategies for Low Power Devices

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Outline



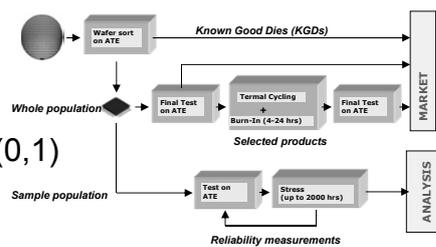
1. Basics on Test
2. Relevance of power during test
3. Main test power issues
4. Reducing test power by dedicated techniques
5. Low power design and its implications on test
6. Reducing test power of low power circuits
7. Conclusion

3

Context



- Manufacturing test
- Digital circuits and systems
- Test stimuli are logic values (0,1)
- Test is an experiment !
 - ✓ If responses meet expectations, chip may be good ... or stimuli are not sufficient (test escape)
 - ✓ If responses fail, chip may be faulty ... or measurement may be erroneous (yield loss)
- Test costs can now amount to 40% of overall product cost



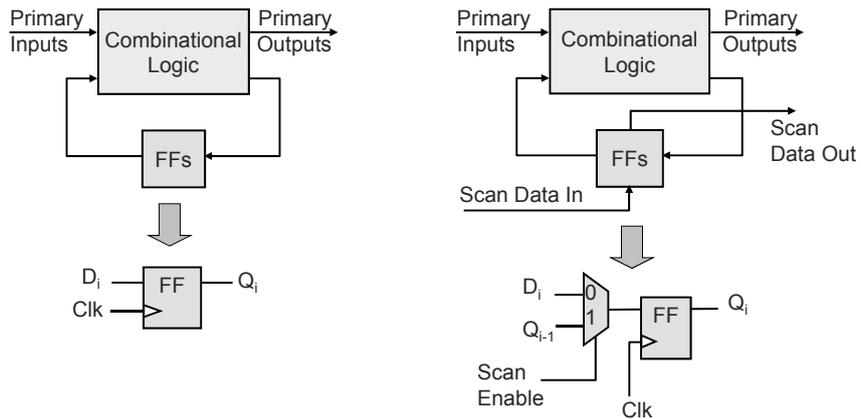
(courtesy: Bernardi et al., ETS, 2009)

4

Basics on Test - DfT

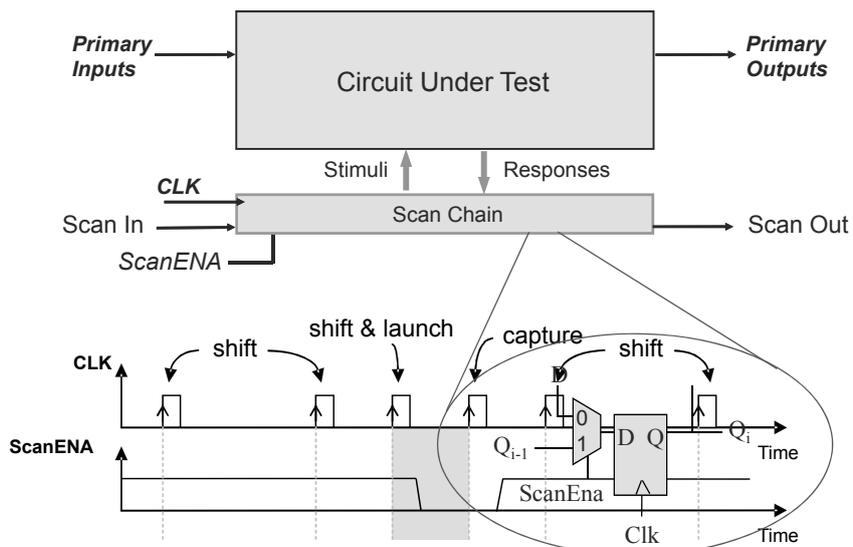


- Functional test is used ... but structural test is dominant !
- Use of fault models ... and DfT (Design-for-Test)



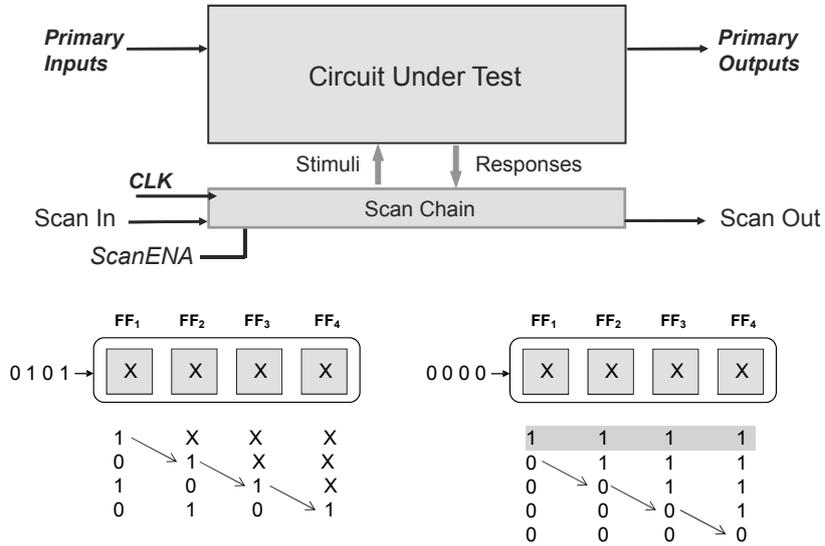
5

Basics on Test - DfT



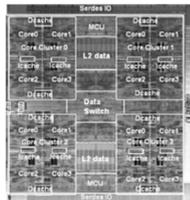
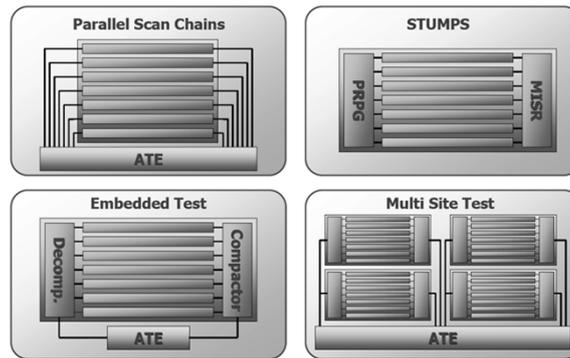
6

Basics on Test - DfT



7

Basics on Test - DfT



Example (presented @ ITC 2008):

- 16 core CMT microprocessor from Sun Microsystems
- 410 millions of transistors, 250W @ 2.3GHz, 1.2V
- 1.35 millions of flip-flops, all are scannable !!

8

Power Consumption in CMOS

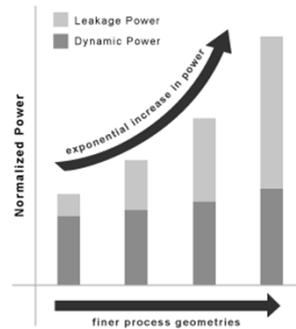


Switching (dynamic) Power

- Due to charge/discharge of load capacitance during switching
- $P_{DYN} \propto V_{DD}^2 \cdot F_{CLK}$

Leakage (static) Power

- Power consumed when the circuit is idle
- Mainly due to sub-threshold leakage
- $I_{SUB} \propto V_{DD} / V_{TH}$

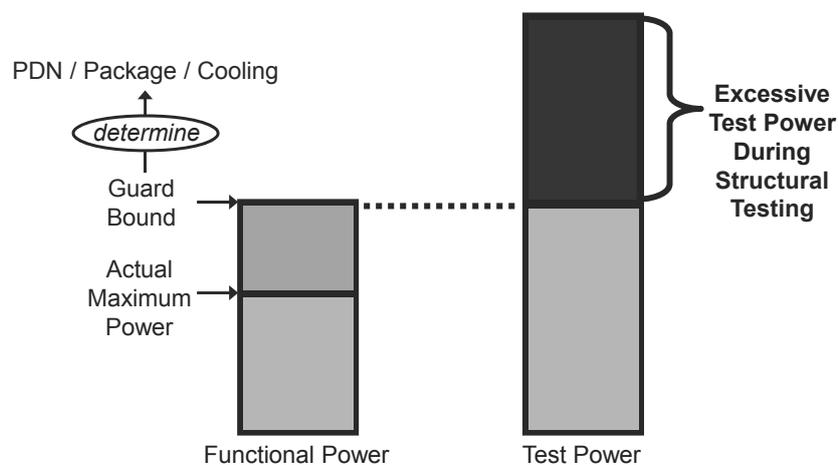


9

Power During Test ...



Much higher than during functional operations



10

Power During Test ...



Much higher than during functional operations

(presented by TI & Siemens AG @ ITC 2003)
ASIC (arithmetic) with Scan, 1M gates, 300kbits SRAM



Toggle activity under functional mode : 15%-20%
Toggle activity under test mode : 35%-40%

(Presented by Freescale @ ITC 2008)

Power under test mode up to 3.8X power during functional mode

And many other industrial experiences reported in the literature ...

11

Power During Test ...



Main reasons for excessive test power

- No correlation between consecutive test vectors
- Test vectors may ignore functional (especially power) constraints
- Non-functional clocking during test (e.g. LOC or LOS)
- DFT (e.g. scan) circuitry intensively used
- Concurrent testing often used for test time efficiency
- Compression and compaction used for test data volume reduction

For conventional (non low-power) designs, dynamic power is the main responsible for excessive test power !!

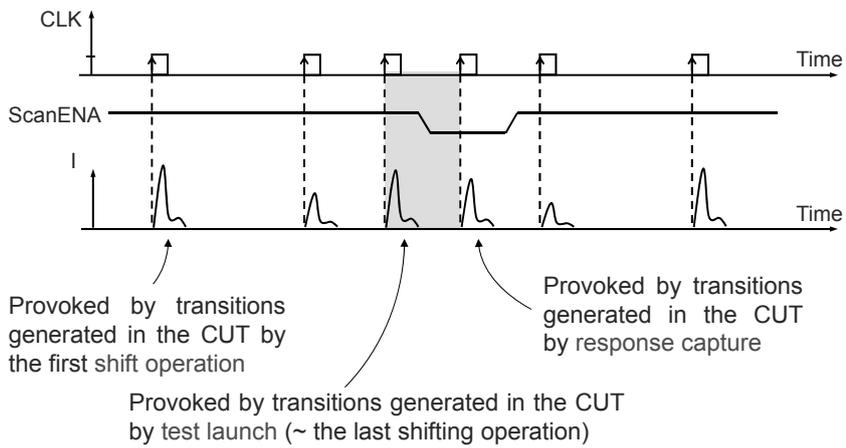
Leakage power is a real issue during IDDQ test (reduced sensitivity) and during burn-in test (can result in thermal runaway condition and yield loss)

12

Power During Test ...



Conventional (slow-speed) scan testing

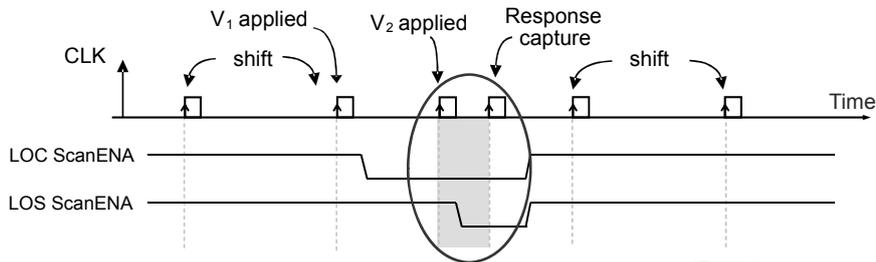


13

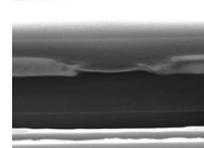
Power During Test ...



At-speed scan testing with a LOC/LOS scheme

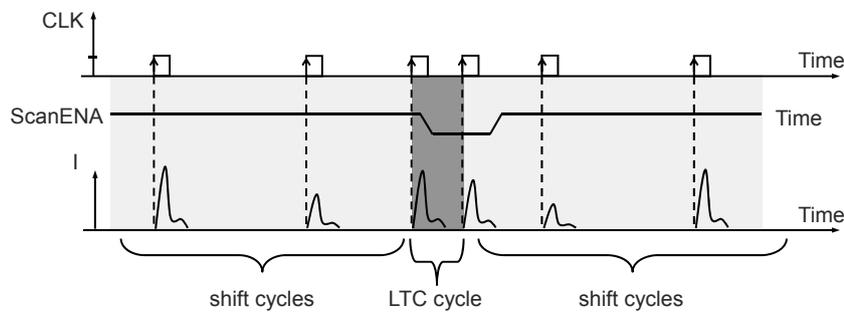


- Used to test for timing faults often caused by resistive defects
- Need of two-vector test patterns to provoke transitions
- Commonly used in microprocessor test
- **Example:** quad-core AMD Opteron processor (presented @ ITC 2008)



14

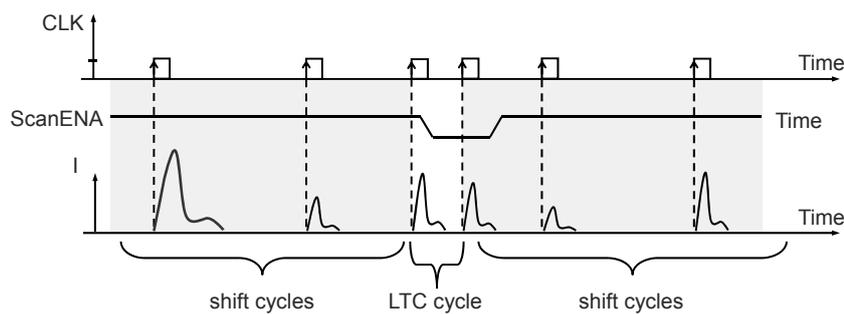
Power During Test ...



- The problem of excessive power during scan testing can be split into two sub-problems: excessive power during the shift cycles and excessive power during the Launch-To-Capture (LTC) cycle

15

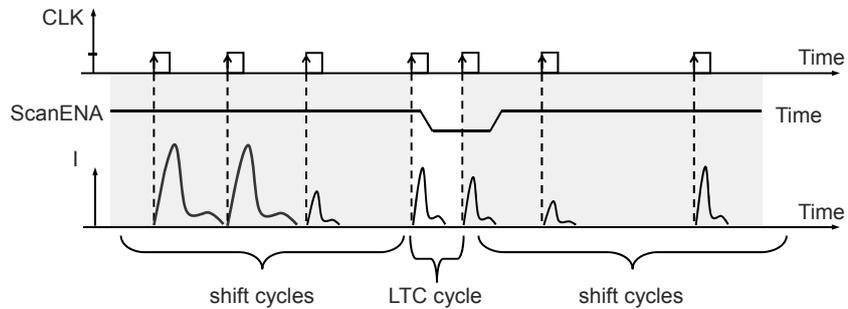
Power During Test ...



- Excessive power during the shift cycles:
 - ↳ no value has to be captured/stored
 - ↳ **one peak is not relevant**

16

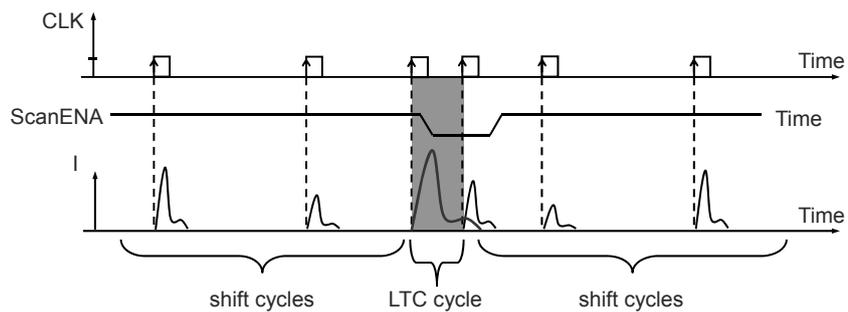
Power During Test ...



- Excessive power during the shift cycles:
 - ↪ more than one peak → relates to **high average power**
 - ↪ **problems may occur**

17

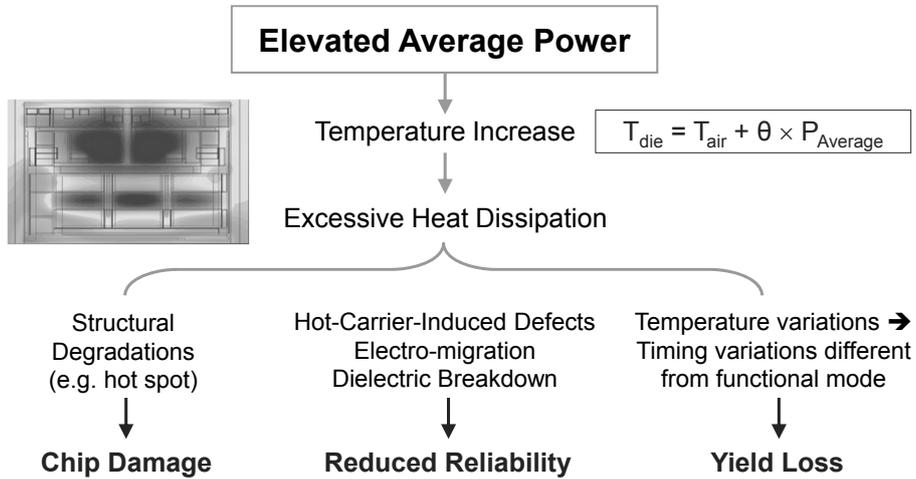
Power During Test ...



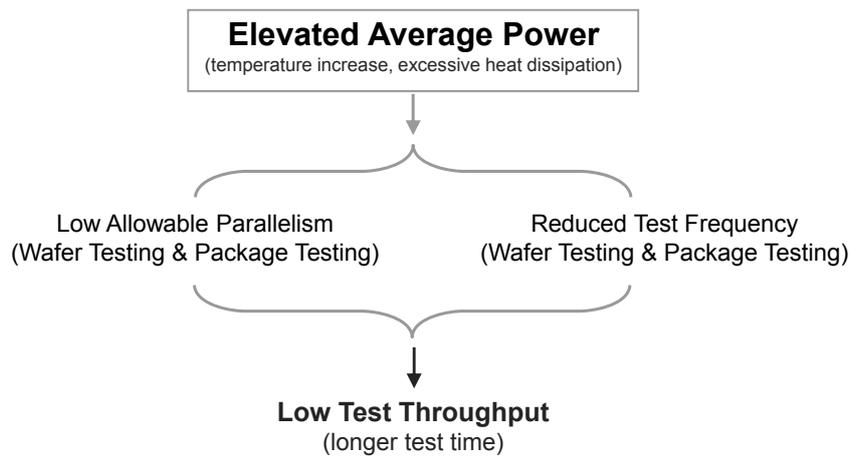
- Excessive power during the LTC cycle:
 - ↪ logic values have to be captured/stored
 - ↪ **one peak is highly relevant**

18

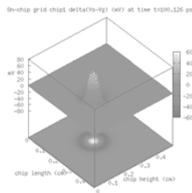
Main Test Power Issues



Main Test Power Issues



Main Test Power Issues



High Instantaneous Current

Elevated Peak Power

Power Supply Noise (IR-Drop, Ldi/dt)

Significant Delay Increase due to Excessive PSN

Erroneous Behavior Only During Testing (test fail)

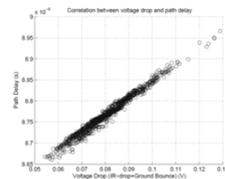
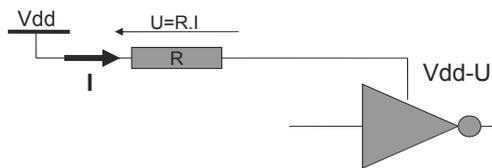
Manufacturing Yield Loss
(Over-Kill)

As huge designs can be manufactured today, most power-related test issues (during scan) are due to excessive peak power

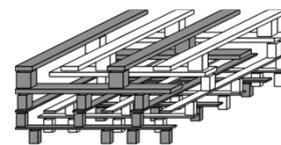
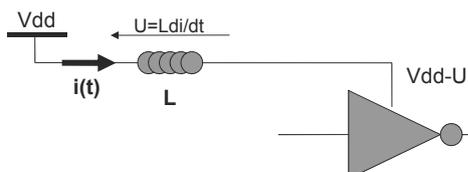
Main Test Power Issues



- **IR Drop** refers to the amount of decrease (increase) in the power (ground) rail voltage and is linked to the existence of a resistance between the PDN source and the Vdd (Gnd) node of the gate

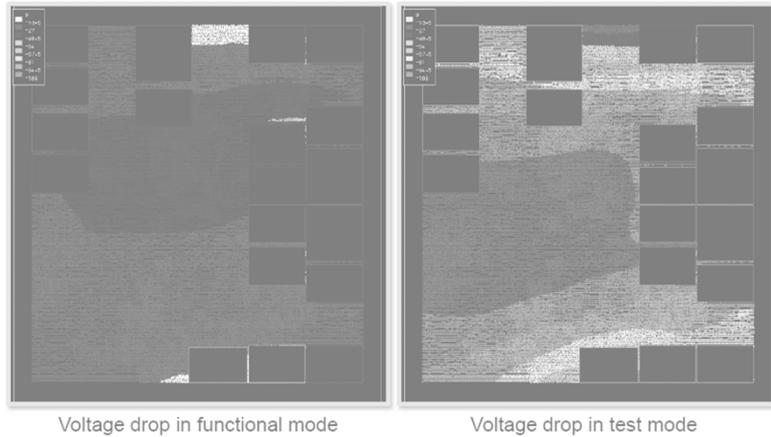


- **L(di/dt)** due to abrupt changes in current in short time (during switching) through inductive connections



(courtesy: O. Sentieys, IRISA, France)

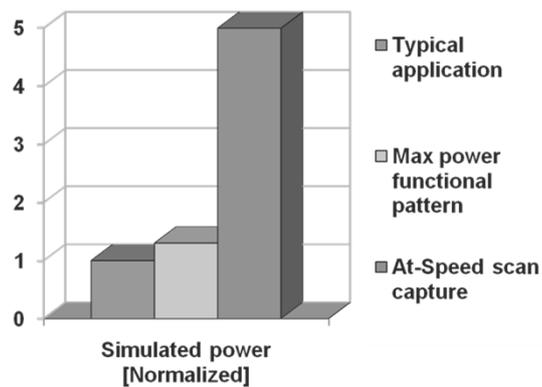
Main Test Power Issues



(courtesy: A. Domic, Synopsys, USA)

23

Main Test Power Issues



- Voltage drop: the main suspect for increased delay during capture
- Presented by Freescale @ ITC 2008

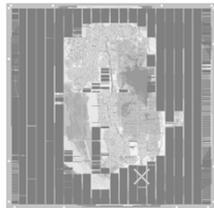
24

Main Test Power Issues



- Local IR-drop can be an issue even though total test power is reduced

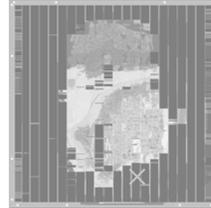
activate all modules



peak: 1.2V @ 1.026V
(176mV(14.5%) drop)



activate only one module



peak: 1.2V @ 1.029V
(171mV(14.3%) drop)

(courtesy: K. Hatayama, STARC, Japan)

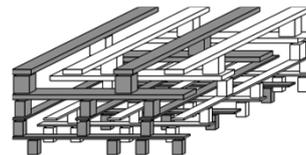
25

Reducing Test Power



Straightforward Solutions

- Test with lower clock frequency
- Partitioning and appropriate test planning
- Over sizing power distribution network (PDN)
 - Grid Sizing based on functional power requirements
- all parts not active at a time
 - Grid Sizing for test purpose too expensive !!



Costly or longer test time

26

Reducing Test Power



Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, ...

27

Reducing Test Power



Main classes of dedicated solutions

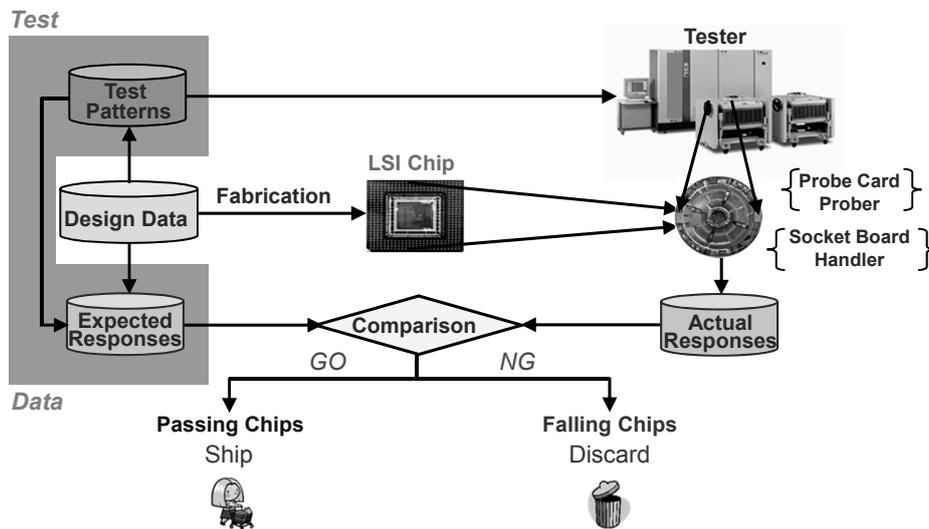
- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

28

Low-Power Test Pattern Generation



The Role of Test Data in Test Flow

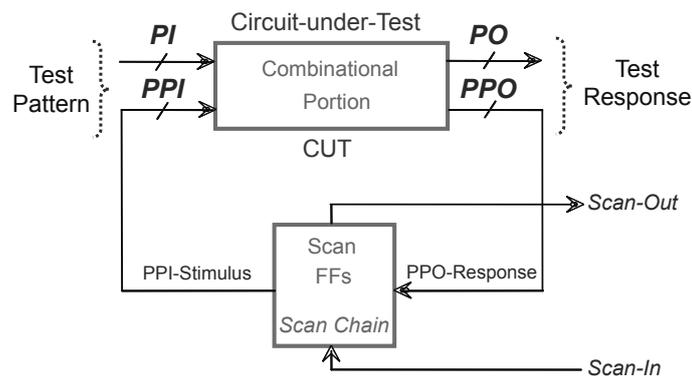


29

Low-Power Test Pattern Generation



Target of Scan Test Pattern Generation



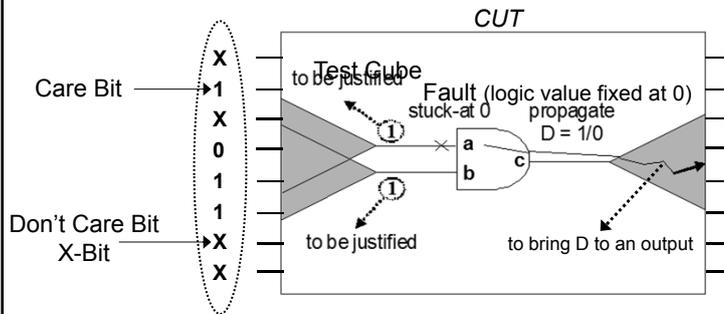
- **Scan Test Pattern Generation:** Assume a target fault in CUT, and find logic value assignments to some inputs (PI / PPI) so that the faulty (with the fault) and fault-free (without the fault) CUT create different responses on at least one output (PO / PPO).

30

Low-Power Test Pattern Generation



Automatic Test Pattern Generation (ATPG)



- ATPG is based on complex algorithms and is used to determine logic values for input bits in order to detect a fault in the given CUT.
- Not all input bits need to be assigned with logic values in order to detect a fault.
- The immediate result of ATPG is a test cube, which contains both specified bits (care bits) and unspecified bits (don't care bits or X-bits).

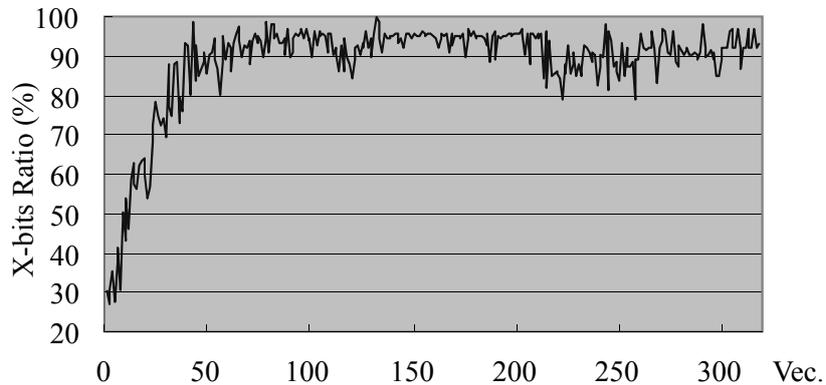
31

Low-Power Test Pattern Generation



X-Bits in Test Cubes

(Block in an Industry Chip: 90nm-Process / 1.2V / 50K-Gate / 2.5% VDD IR-Drop Allowance)



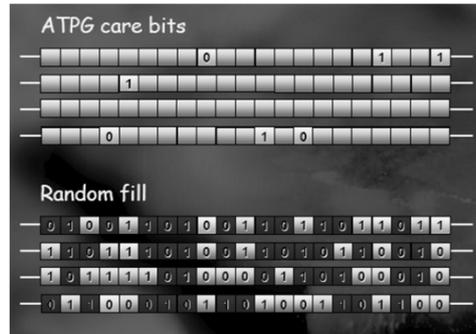
- A large percentage of input bits in a test cube are don't care bits (X-bits).
- Need X-filling (i.e., assigning logic values to X-bits) to create a complete test pattern.

32

Low-Power Test Pattern Generation



Conventional X-Filling Technique: *Random-Fill*



- Conventionally, X-bits in a test cube are filled with random logic values.
- Advantages → *Small test pattern count due to “fortuitous detection”*
- Disadvantage → *High test (shift and LTC) power*

33

Low-Power Test Pattern Generation



Various Low-Power X-Filling Techniques

Low-Shift-Power X-Filling ✓		
Shift-In Power Reduction	Shift-Out Power Reduction	Total Shift Power Reduction
<i>0-fill</i> <i>1-fill</i> <i>MT-fill</i> <i>adjacent fill / repeat fill</i>	<i>output-justification-based X-filling</i>	<i>MTR-fill</i>
Low-LTC-Power X-Filling ✓		
FF-Oriented	Node-Oriented	Critical-Area-Oriented
<i>PMF-fill</i> <i>LCP-fill</i> <i>preferred fill</i> <i>JP-fill</i> <i>CTX-fill</i>	<i>PWT-fill</i> <i>state-sensitive X-filling</i>	<i>CCT-fill</i> <i>CAT-fill</i>
Low-Shift-and-LTC-Power X-Filling ✓		
<i>impact-oriented X-filling</i>	<i>hybrid X-filling</i>	<i>bounded adjacent fill</i>
Low-Power X-Filling for Compressed Scan Testing		
<i>0-fill</i>	<i>PHS-fill</i>	<i>CJP-fill</i>

(source: X. Wen and S. Wang, *Low-Power Test Generation*, Chapter 3 in *Power-Aware Testing and Test Strategies for Low-Power Devices*, edited by P. Girard, N. Nicolici & X. Wen, Springer, 2009)

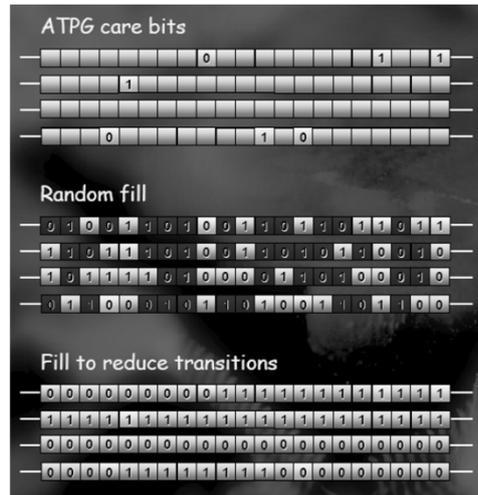
34

Low-Power Test Pattern Generation



Example 1: Low-Shift-Power X-filling

- **Goal:** To assign proper logic values to don't care bits (X-bits) in a test cube so as to reduce transitions in scan chains (and thus also in the combinational logic).
- Popular techniques include **0-fill**, **1-fill**, **MT-fill**, and **adjacent-fill**.
- Mostly shift-in power is reduced. Occasionally, shift-out power and LTC power are also reduced, especially by **0-fill**.
- Reported by TI at ITC 2003.
- No area overhead but may increase test pattern count.

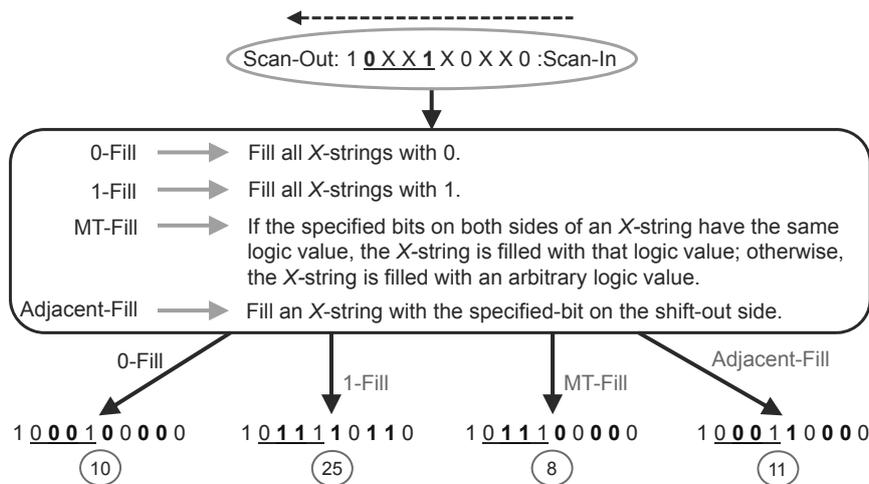


35

Low-Power Test Pattern Generation



Example 1 (cont'd): Low-Shift-Power X-filling



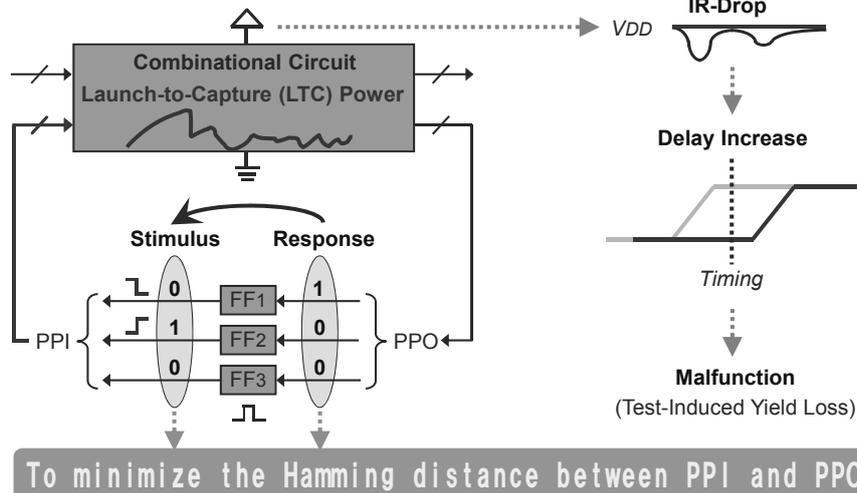
• Available from most commercial ATPG tools.

36

Low-Power Test Pattern Generation



Example 2: Low-LTC-Power X-Filling



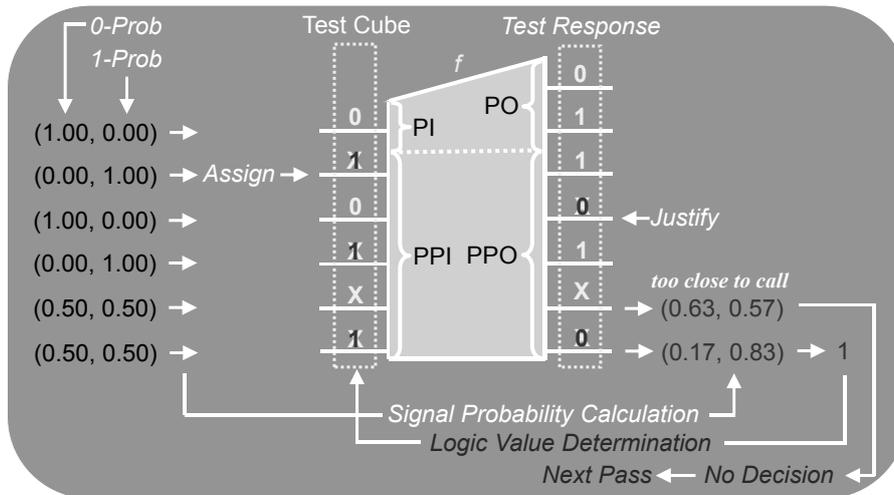
37

Low-Power Test Pattern Generation



Example 2 (cont'd): Low-LTC-Power X-Filling

JP-Fill



(source: X. Wen et al., Proc. ITC, Paper 25.1, 2007)

38

Low-Power Test Pattern Generation



Summary - (1)

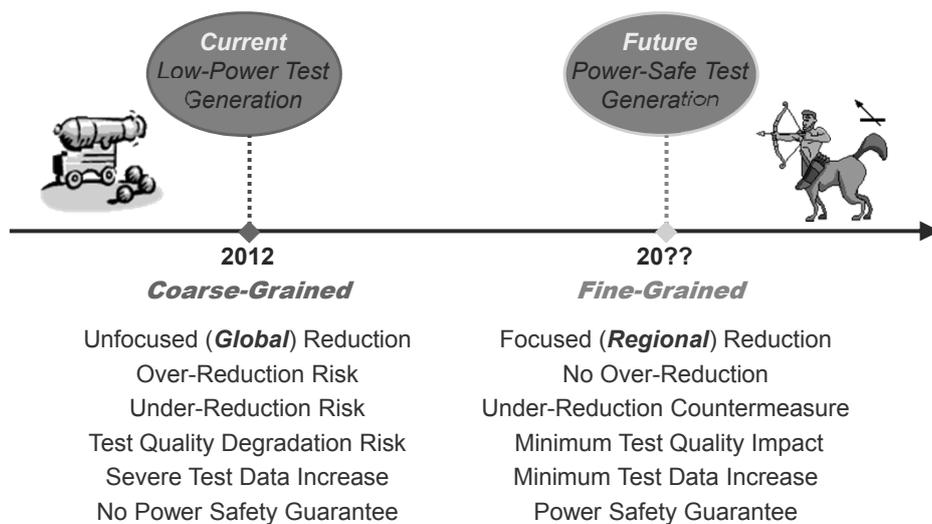
- A large portion of input bits in test cubes are don't care bits (X-bits) even after aggressive test compaction in ATPG.
- X-bits can be used for reducing various shift and/or LTC power. Especially, 0-fill can reduce shift-in, shift-out, and LTC power to some extent.
- X-filling-based low-power test generation causes neither area overhead nor performance degradation.
- Most commercial ATPG tools now support low-power X-filling.
- Test pattern count may increase due to low-power X-filling. This problem can be solved by
 - (1: *Vector-Pinpoint*) identifying high-test-power test patterns and conducting X-filling only for those patterns, or
 - (2: *Area-Pinpoint*) identifying high-test-power areas and conducting X-filling only to reduce test power in those areas.

41

Low-Power Test Pattern Generation



Summary - (2)



(source: X. Wen, ETS, Invited Talk, 2012)

42

Reducing Test Power



Main classes of dedicated solutions

- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

Objective

Make test power dissipation comparable to functional power

While achieving high fault coverage, short test application time, small test data volume, low test development efforts, low area overhead, ...

43

Design for Test Power Reduction



During scan testing (standard or at-speed):

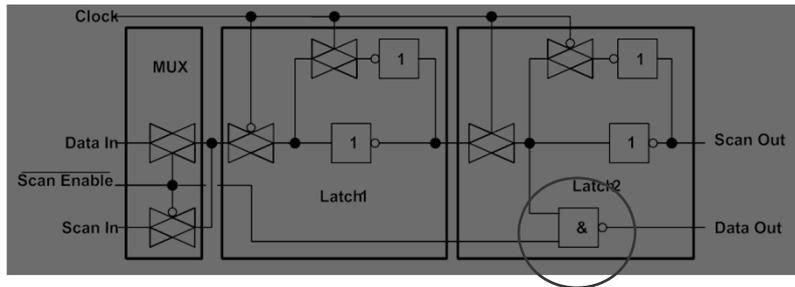
Shift Power Reduction	LTC Power Reduction
<ul style="list-style-type: none">● Shift Impact Blocking<ul style="list-style-type: none">- blocking gate, special scan cell- first-level power supply gating● Scan Chain Modification<ul style="list-style-type: none">- scan cell reordering- scan chain segmentation- scan chain disable● Scan Clock Manipulation<ul style="list-style-type: none">- splitting, staggering- multi-duty clocking	<ul style="list-style-type: none">● Partial Capture<ul style="list-style-type: none">- circuit modification- scan chain disable- one-hot clocking- capture-clock staggering

44

Design for Test Power Reduction



Example 1: Low power scan cell



- Master-slave structure of a mux-D flip-flop is modified
- Gate the data output during shift
- Toggle suppression during shift
- But modification of all flip-flops → impact on area and performance

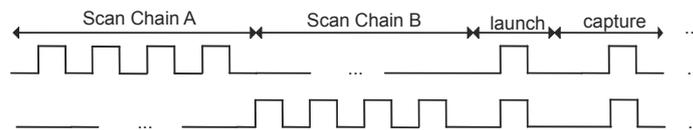
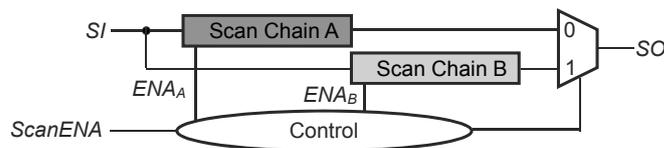
(source: A. Hertwig and H.-J. Wunderlich, Proc. ETW, pp. 49-53, 1998)

45

Design for Test Power Reduction



Example 2: Scan chain segmentation



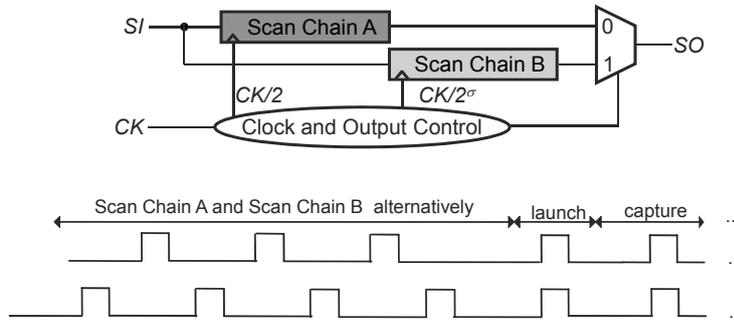
- Controllable and data-independent effect of shift power reduction
- No change to ATPG and no increase in test application time
- Presented (and used) by TI @ ITC 2000

46

Design for Test Power Reduction



Example 3: Staggered clocking



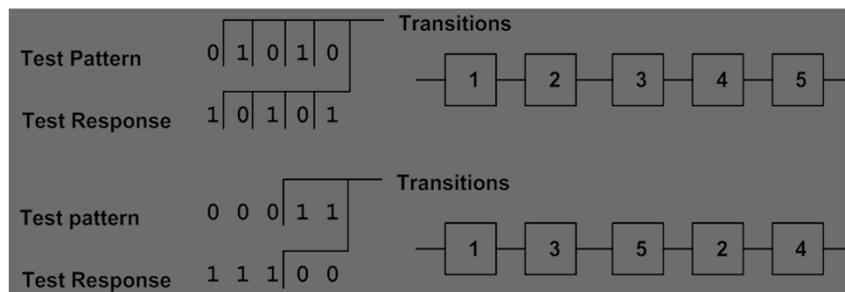
- The original scan chain is segmented into two new scan chains
- Each scan chain is driven by a clock whose speed is half of the normal speed
- At each clock cycle, only half of the circuit inputs can switch

47

Design for Test Power Reduction



Example 4: Scan cell reordering



- Scan cell order influences the number of transitions
- Need to change the order of bits in each vector during test application
- No overhead, FC and test time unchanged, low impact on design flow
- May lead to routing congestion problems ...

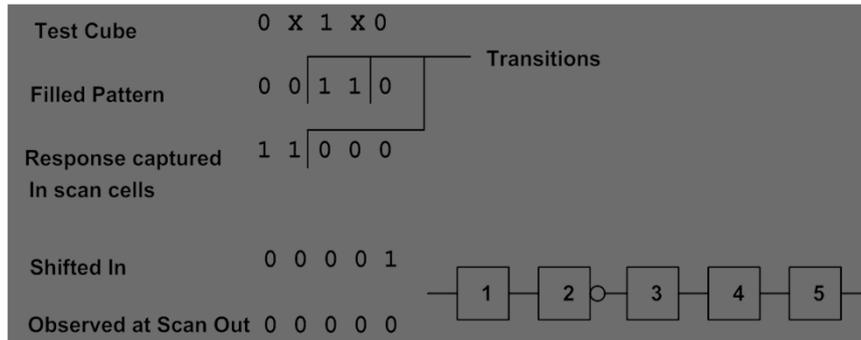
(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

48

Design for Test Power Reduction



Example 5: Inserting logic into scan chains



- The goal is to modify the transition count during shift

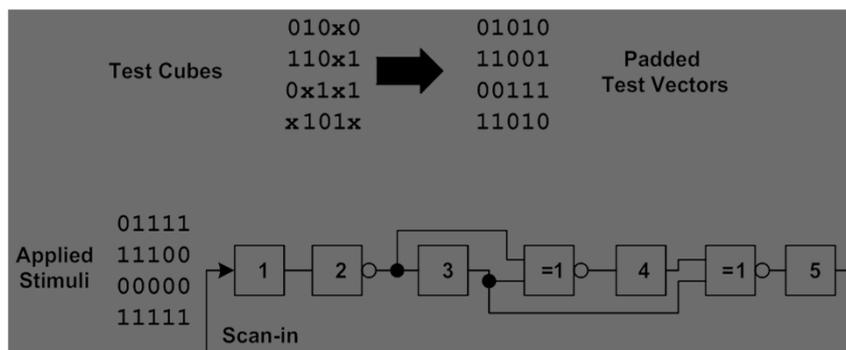
(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

49

Design for Test Power Reduction



Example 6: Scan segment inversion



- This is done by embedding a linear function in the scan path
- Reduces the transition count in the scan chain

(courtesy: H.-J. Wunderlich and C. Zoellin, Univ. Stuttgart)

50

Reducing Test Power



Main classes of dedicated solutions

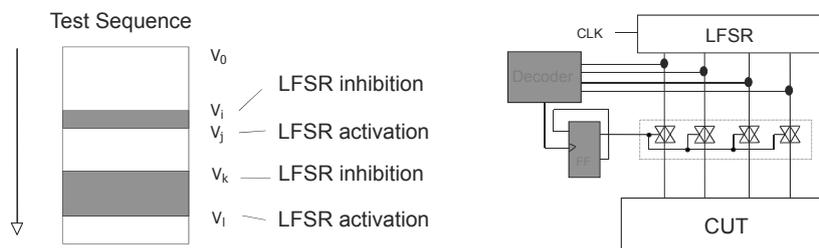
- Low-Power Test Pattern Generation
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51

Power-Aware BIST and Compression



Example 1: Masking logic insertion during BIST



Prevent application of non-detecting (but consuming) vectors to the CUT. A decoder is used to store the first and last vectors of each sub-sequence of consecutive non-detecting vectors to be filtered.

Minimizes average power without reducing fault coverage

(source: P. Girard et. al., Proc. VTS, pp. 407-412, 1999)

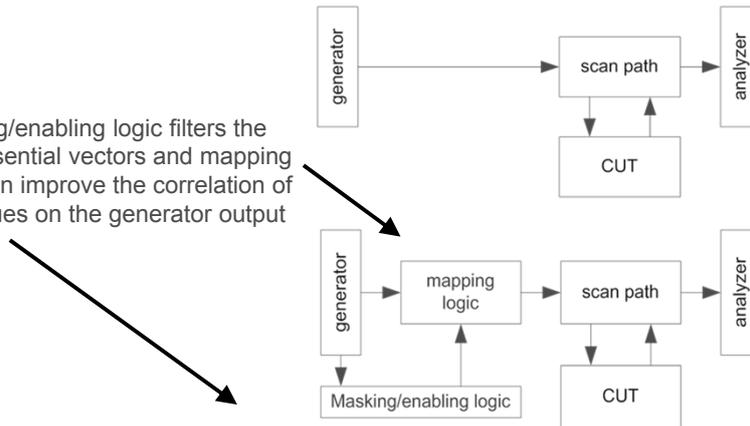
52

Power-Aware BIST and Compression



Example 2: Adaptation to Scan-Based BIST

Masking/enabling logic filters the non-essential vectors and mapping logic can improve the correlation of the values on the generator output



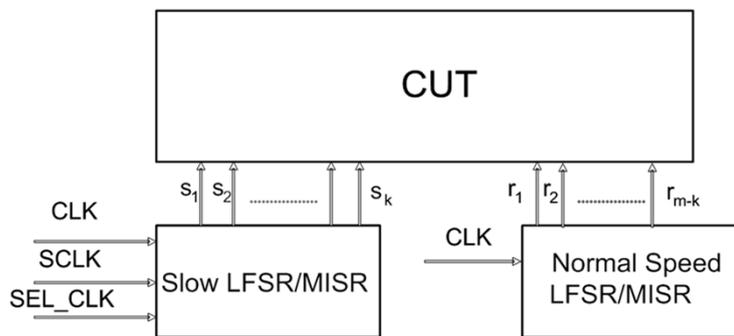
(source: F. Corno et al., Proc. DFT, pp. 219-226, 1999)

53

Power-Aware BIST and Compression



Example 3: Dual-speed LFSR for BIST



Dual-speed LFSR - concept

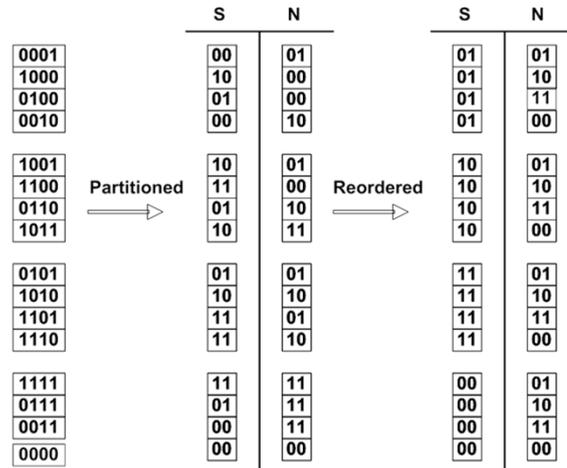
(source: S. Wang and S. Gupta, Proc. ITC, pp. 848-857, 1997)

54

Power-Aware BIST and Compression



Example 3 (cont'd): Dual-speed LFSR for BIST



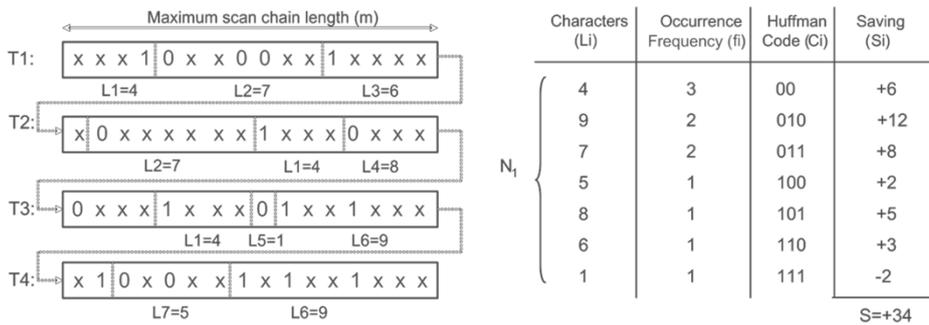
(source: S. Wang and S. Gupta, Proc. ITC, pp. 848-857, 1997)

55

Power-Aware BIST and Compression



Example 4: Coding for compression and test power



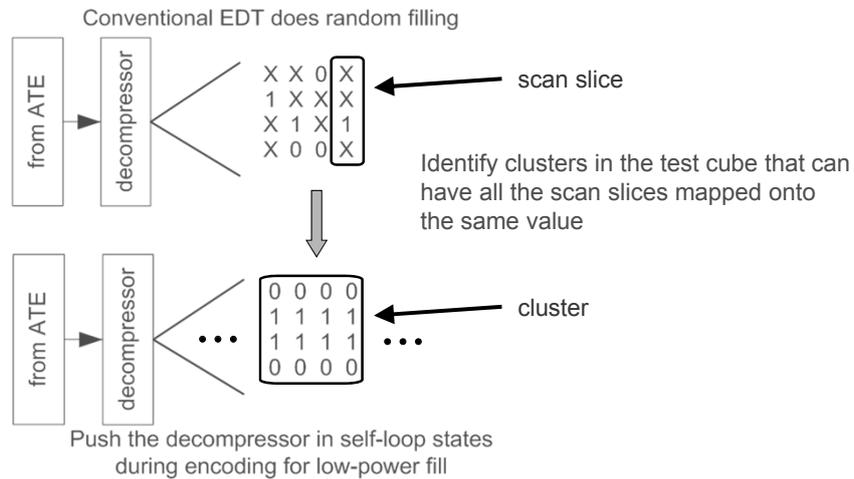
(courtesy: K. Chakrabarty and S.K. Goel, Duke Univ.)

56

Power-Aware BIST and Compression



Example 5: Linear Finite State Machines



(source: F. Czyrusz et al., Proc. VTS, pp. 75-83, 2007)

57

Reducing Test Power



Main classes of dedicated solutions

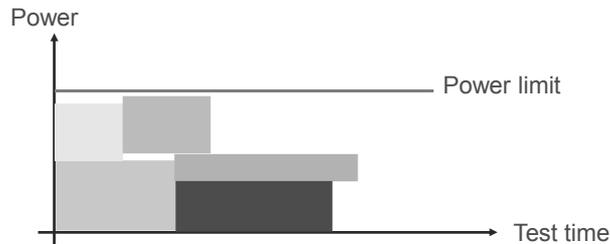
- Low-Power Test Pattern Generation
- Design for Test Power Reduction
- Power-Aware BIST and Test Data Compression
- System-Level Power-Aware Test Scheduling

58

System-Level Power-Aware Scheduling



Improve Test Throughput by Exploiting Design Modularity



- The goal is to determine the blocks (memory, logic, analog, etc.) of an SOC to be tested in parallel at each stage of a test session in order to keep power dissipation under a specified limit while optimizing test time
- Some of the test resources (pattern generators and response analyzers) must be shared among the various blocks

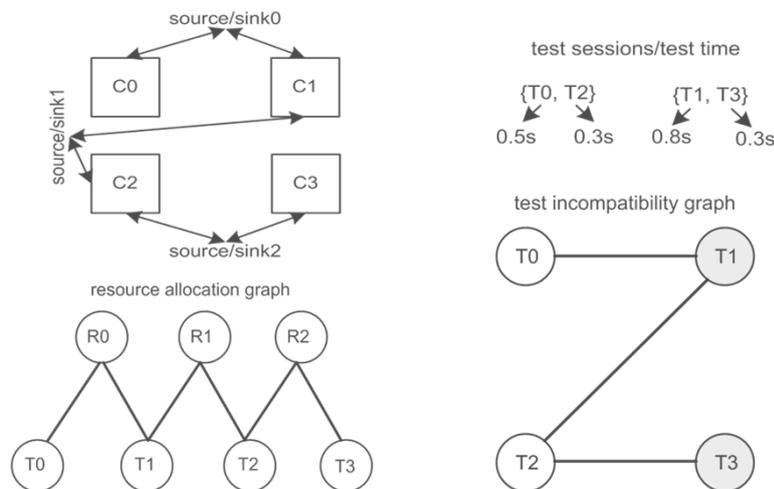
(source: Y. Zorian, Proc. VTS, pp. 4-9, 1993)

59

System-Level Power-Aware Scheduling



Example 1: Resource Allocation and Incompatibility Graphs



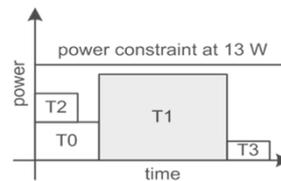
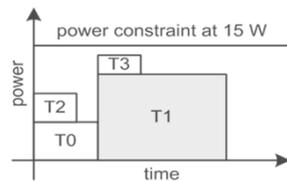
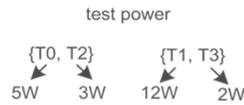
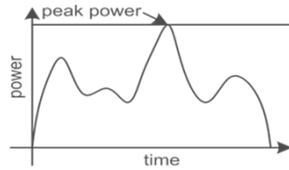
(source: R. Chou et al., IEEE Trans. on VLSI, Vol. 5, No. 2, pp. 175-185, 1997)

60

System-Level Power-Aware Scheduling



Example 1 (cont'd): Power Model and Test Schedule



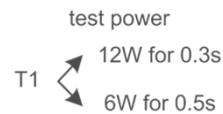
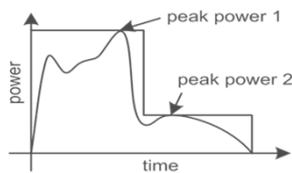
(source: R. Chou et al., IEEE Trans. on VLSI, Vol. 5, No. 2, pp. 175-185, 1997)

61

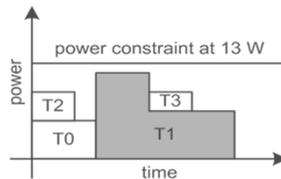
System-Level Power-Aware Scheduling



Example 2: Power Profile Manipulation



Power profile can be modified by pattern modification and/or test set reordering

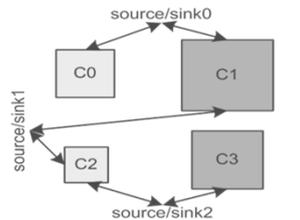


62

System-Level Power-Aware Scheduling

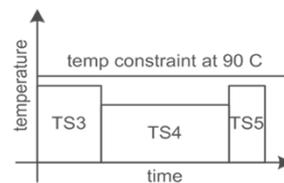
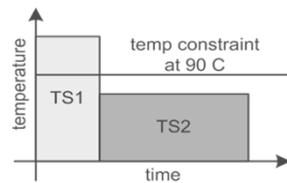


Example 3: Thermal Considerations



temperature dependent test

TS1 = {T0, T2}	→	130 C
TS2 = {T1, T3}	→	70 C
TS3 = {T0, T3}	→	80 C
TS4 = {T1}	→	60 C
TS5 = {T2}	→	80 C



63

Evaluating ...



Test Power Reduction Strategies

- Power reduction effectiveness *High*
- Fault coverage impact *Low*
- ATPG engine impact *Minimum*
- Test data volume impact *Low*
- Test time impact *Low*
- Functional timing impact *Low*
- Area overhead *Low*
- Usability with test compression *High*
- Design effort *Minimum*
- Design flow change *Low*

(source: S. Ravi, TI, ITC07)

64

Test Power Estimation



- Needed for test space exploration (DfT/ATPG) early in the design cycle
- Availability of scan enhanced design and ATPG patterns only at the gate level in today's design flows imposes the usage of gate-level estimators for test power
- Conventional flow adopted to perform estimation is simulation-based
- Estimation is performed at various PVT corners
- Challenges for multi-million gate SoCs
 - Time-consuming !!
 - Dump sizes can be very large !!
- The weighted transition metric (WSA) is quick but approximate

Faster and low cost solutions for test power estimation are needed !

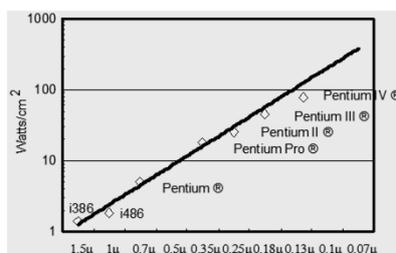
65

Low Power Design (LPD)



Power Consumption Trends

- Exponential growth in transistor density
 - More functionality
- But linear reduction in supply voltage
 - Not adequate to prevent power density to increase



(source: Tirumurti et al., DATE, 2004)

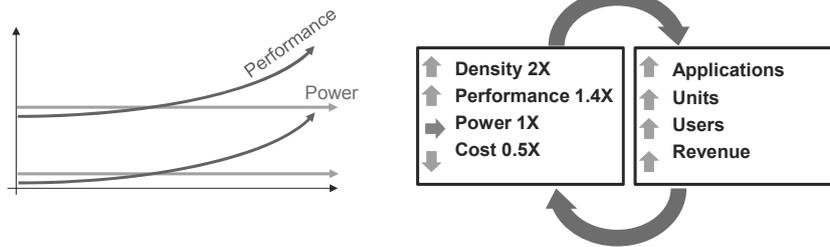
66

Low Power Design (LPD)



The new power-performance paradigm:

- Low (fixed) power budget to limit power density
- But ever increasing integration and performance ...



Adoption of low-power design and power management techniques

(courtesy: M. Hirech, Synopsys, USA)

67

Low Power Design (LPD)



System & Architecture <ul style="list-style-type: none"> ▪ Voltage / Frequency Scaling ▪ Architecture (parallel, well managed pipeline, etc.) ▪ Others (H/S partitioning, instruction set, algorithms, etc.) 	IC Design & Implementation <ul style="list-style-type: none"> ▪ Clock Gating ▪ Multiple Supply Voltage ▪ Multiple Threshold Voltage ▪ Substrate-Bias ▪ Power Gating ▪ Others
Circuit (Logic) Design <ul style="list-style-type: none"> ▪ Low Power Cell Library ▪ Gate sizing (to equalize paths) ▪ Buffer insertion to reduce slew ▪ Logic restructuring to avoid hazards ▪ Memory Bit Cell and Compiler ▪ Others 	Process Technology <ul style="list-style-type: none"> ▪ Reduce Vdd ▪ Threshold Voltage Option ▪ Low Capacitance Dielectric ▪ New Gate Oxide Material ▪ Transistor Sizing ▪ Others

68

Low Power Design (LPD)



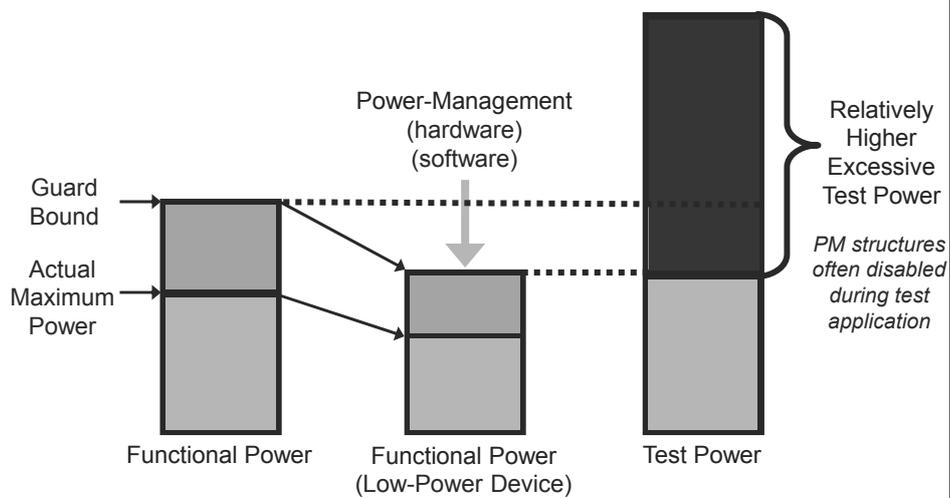
Main LPD techniques	Power reduction	
	Dynamic	Leakage
Clock gating	✓	
Power gating	✓	✓
Multi-Voltage domains	✓	
Multi-Threshold cells		✓

These techniques are often combined together to achieve the maximum power optimization value

Power During Test ...



Even more critical for Low-Power Design !!



(courtesy: X. Wen, KIT)

Requirements for Test of LPD



- Reduce (even more) test power by using the power management (PM) infrastructure (and/or applying the previous dedicated solutions)
- Preserve the functionality of the test infrastructure
- Test the power management (PM) structures

And still target:

High fault coverage, short test application time, small test data volume, low area overhead, etc ... while making test power dissipation (dynamic and leakage) comparable to functional power

71

Reducing Test Power of LPD



Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

Objective (again)

Make test power dissipation comparable to functional power

72

Reducing Test Power of LPD



Main classes of dedicated solutions

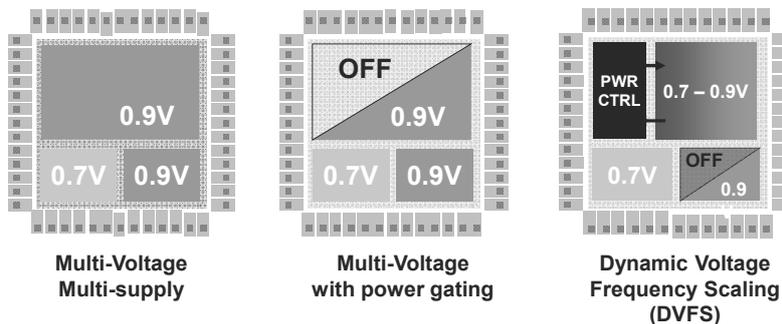
- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

73

Test for Multi-Voltage Designs



Multi-Voltage Design Styles



- Creation of “power islands”
- Vdd scaling results in quadratic power reduction ($P=kCV^2f$)
- Level shifters to let signals cross power domain boundaries

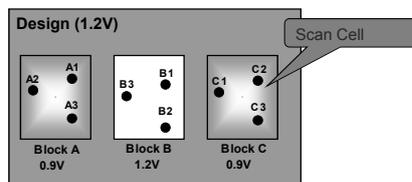
74

Test for Multi-Voltage Designs



Example 1: Multi-Voltage Aware Scan Cell Ordering

- Multi-voltage aware scan chain assembly considers the voltage domains of scan cells during scan cell ordering so as to minimize the occurrence of chains that cross voltage domains
- Minimize number (area overhead) of level shifters (by 93%)



Scan chain assembly

Ordering / Position	Logical	Physical	Multi-Voltage
1	A1	A2	A2
2	A2	A1	A1
3	A3	A3	A3
4	B1	B3	C1
5	B2	B1	C2
6	B3	B2	C3
7	C1	C1	B2
8	C2	C2	B3
9	C3	C3	B1

- Presented by Synopsys in JOLPE vol.1 n° 1 April 2005 and implemented in Synopsys Galaxy™ Test

Level shifter

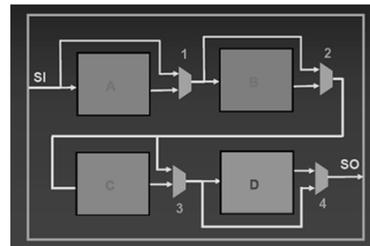
75

Test for Multi-Voltage Designs



Example 2: Power-Aware Scan Chain Assembly

- Test infrastructures like scan chain or TAM may cross several power domains and can be broken if some of these domains are temporarily powered-down for low-power constraints
- Bypass multiplexers allow testing of specific power domains in MSMV environment (switched-off power domains are bypassed)
- Preserve test functionality !



- Presented by Cadence @ ITC 2008 and implemented in Cadence Encounter™

76

Test for Multi-Voltage Designs



Example 3: Voltage scaling in scan mode

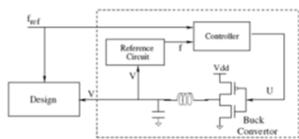
- During scan shifting, the combinational logic needs not meet timing
- Goal: re-use the DVS infrastructure in test mode to propose a scaled-voltage scan test scheme. The goal is to reduce dynamic and leakage power dissipation by using a lower supply voltage during scan shifting
- At-speed testing with a LOC or a LOS test scheme is assumed, as well as the fact that the scan shift speed is usually lower than the functional (capture) speed
 - Example: functional supply voltage (V_{max}) = 1.1 V, functional frequency (F_{max}) = 500 MHz, threshold voltage of scan FFs (V_t) = 0.35 V, shift Frequency (F_{shift}) = 125 MHz $\rightarrow V_{shift} = 0.635$ V
- Presented by TI @ ITC 2007

77

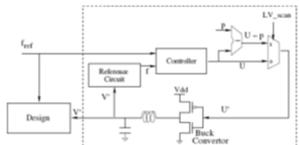
Test for Multi-Voltage Designs



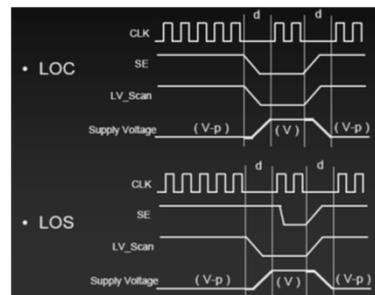
Example 3 (cont'd): Voltage scaling in scan mode



Conventional Voltage Scaling Apparatus



PMScan: Shift Voltage Scaling Apparatus



LV_scan: Control signal from tester for low-voltage scan

- Around 45% reduction of dynamic (average and peak) power and 90% reduction of leakage power, with negligible physical design impact and minimum area overhead

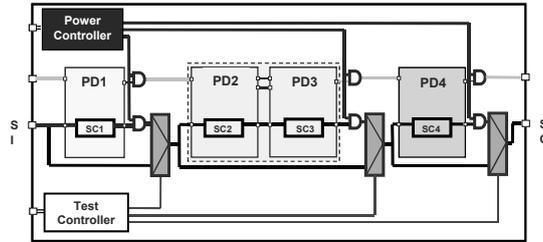
78

Test for Multi-Voltage Designs

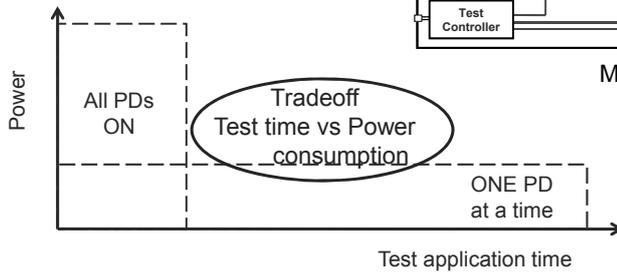


Example 4: Power Domain Test Planning

Objective:
Create distinct test modes (test partitioning) for power domains



Multi-mode DFT architecture



(Source: M. Hirech, Synopsys, DATE, 2008)

Reducing Test Power of LPD



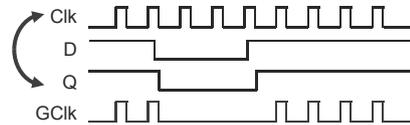
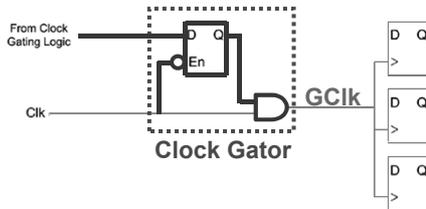
Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

Test for Gated Clock Designs



Basic Clock Gating Design



- Not all FFs need to be triggered to perform a function (e.g., the camera control logic in a mobile-phone SoC can be inactive during a call).
- Gating-off the clock to functionally-noncontributing FFs reduces dynamic power dissipation, *not only in logic portions but also in clock trees (> 50%)*.
- One of the major techniques for reducing functional power.
- Widely adopted and supported by existing EDA tools.

81

Test for Gated Clock Designs



Impact of Clock Gating on Test

- Clock gating prevents all scan FFs from being active at the same time.

- **Impact on Shift Mode**

Negative → Scan shift realized through shift registers may become impossible if some FFs are inactive.



Shift Operation Guarantee Needed

└─ *DfT for Clock Gating Logic* ✓

- **Impact on Capture Mode**

Positive → Dynamic power can be reduced.



Good for LTC Power Reduction

└─ *Dynamic In-ATPG Techniques*
└─ *Static In-ATPG Techniques* ✓
└─ *Post-ATPG X-Filling Techniques* ✓

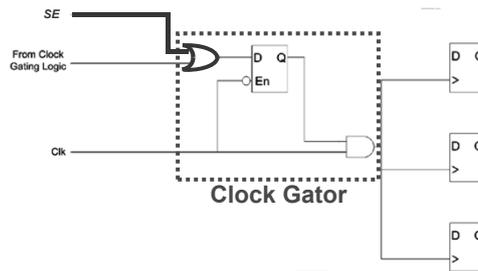
82

Test for Gated Clock Designs



Example 1: DfT for Clock Gating Logic

- **Shift Mode** ($SE = 1$): All scan FFs must be active to form one or more scan chains to shift-in test stimulus / shift-out test response. Clock gating logic needs to be overridden (by SE) in shift mode.
- **Capture Mode** ($SE = 0$): Scan FFs are allowed to be controlled by clock gating logic. Nothing needs to be done.



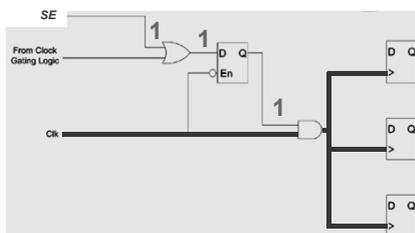
- Automatically implemented by Cadence and Synopsys DfT tools.

83

Test for Gated Clock Designs



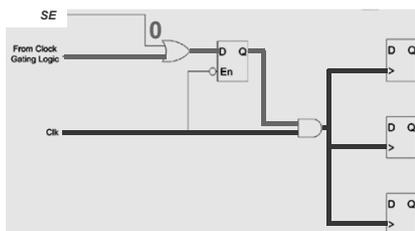
Example 1 (cont'd): DfT for Clock Gating Logic



- Disable clock gating in **shift mode** ($SE = 1$): Unconditionally-ON Clock



Shift Register Operation



- Enable clock gating in **capture mode** ($SE = 0$): Conditionally-ON Clock



LTC Power Reduction

84

Test for Gated Clock Designs



Example 2: LTC Power Reduction by Clock Gating

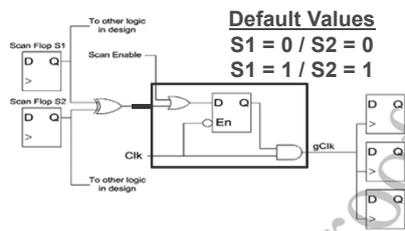
- A **default value** is a value to be assigned to an input in order to gate-off a clock.
 - A *preset value* is to be used to fill an X-bit in a test cube.
- Flow for obtaining default values for clock gating:
 - Identify all clock gators.
 - For each clock gator, calculate a set of input settings that set the clock off.
 - The values in each input setting are default values.
- Flow for using default values for clock gating:
 - Generate a test cube for fault detection.
 - Assign default values to the X-bits in the test cube.
 - (If there are multiple choices of default values, use the one that can turn-off more FFs.)

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

Test for Gated Clock Designs



Example 2 (cont'd): LTC Power Reduction by Clock Gating



Default Values
 $S1 = 0 / S2 = 0$
 $S1 = 1 / S2 = 1$

Test Cubes after ATPG

Test Cubes	Scan flops in design					
	S0	S1	S2	S3	S4	S5
T1	X	0	X	1	0	X
T2	0	1	X	X	X	0
T3	X	X	0	1	0	X

Test Cubes after Assigning Default Values
 (S1=0 / S2=0)

Test Cubes	Scan flops in design						Merge "default values"?
	S0	S1	S2	S3	S4	S5	
T1	X	0	0	1	0	X	Yes
T2	0	0	X	X	X	0	Conflict
T3	X	0	0	1	0	X	Yes

(source: R. Illman et al., Proc. LPonTR, pp. 45-46, 2008)

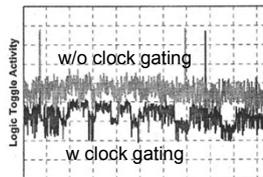
Test for Gated Clock Designs



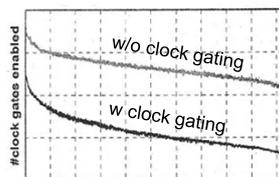
Example 2 (cont'd): LTC Power Reduction by Clock Gating

Circuit Statistics

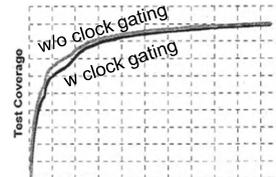
89K FFs
6 Scan Clocks
2200 Clock Gators



Vectors



Vectors



Vectors

- The number of active clocks are reduced by more than 50%.
- LTC toggle activity is reduced by 35%.
- Fault coverage and test set size remain almost unchanged.

(source: R. Illman, et al., Proc. LPonTR, pp. 45-46, 2008)

87

Test for Gated Clock Designs



Summary

- Functional clock gating is indispensable in reducing dynamic power.
- Functional clock gating logic needs to be modified in order to guarantee correct operation in *shift mode*.
- Clock gating can be used in *capture mode* to reduce LTC power.
 - Static In-ATPG Techniques
(Assign pre-determined clock-gator disabling values to don't-care bits (X-bits) in a test cube initially generated for fault detection.)
 - Post-ATPG X-Filling Techniques
(Find and assign proper logic values to don't-care (X-bits) in a test cube so as to disable as many clock gators as possible.)

88

Reducing Test Power of LPD



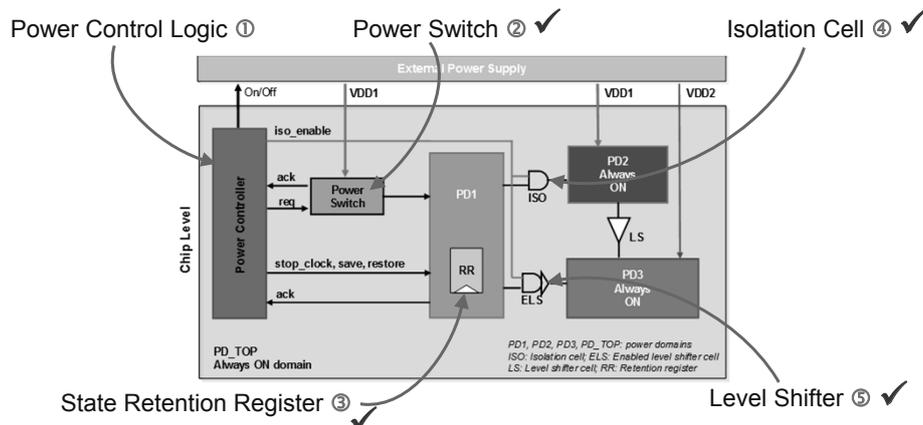
Main classes of dedicated solutions

- Test Strategies for Multi-Voltage Designs
- Test Strategies for Gated Clock Designs
- Test of Power Management (PM) Structures

Test for Power Management Structures



Typical Power Management (PM) Structures

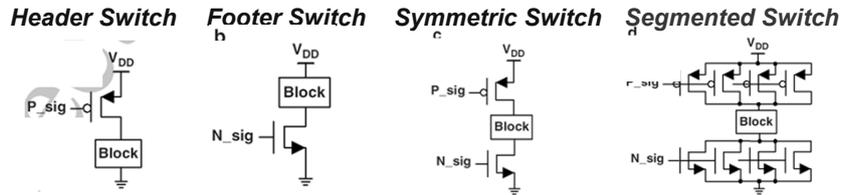


- Conditionally turning on or off power domains) to reduce dynamic and static power.
- Can be described in UPE (Unified Power Format) or CPF (Common Power Format).
- PM structures (①~⑤) require dedicated DfT methods and test patterns.

Test for Power Management Structures



Example 1: Test for Power Switches



Header Switch / Footer Switch / Symmetric Switch

- Also called sleep transistors and used to shut down blocks (power domains) that are not in use (idle mode), hence reducing leakage power and dynamic power.
- Should be large enough to provide sufficient current to the circuit.

Segmented Switch

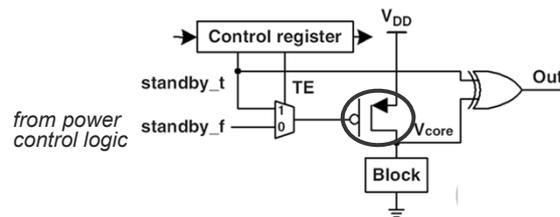
- Individual switch transistors can be small.
- Preferable in practice due to concerns about layout, design for manufacturability, and limiting inrush current when switching on a power domain.

91

Test for Power Management Structures



Example 1 (cont'd): Test for Power Switches



- Pattern 1 (*Test for Short*): $TE = 1 / standby_t = 1$
 → Turn-off the power switch. After sufficient discharge, V_{core} should be much lower than V_{DD} , and thus $Out (fault-free) = 1 / Out (faulty) = 0$
- Pattern 2 (*Test for Open*): $TE = 1 / standby_t = 0$
 → Turn-on the power switch. V_{core} should be close to V_{DD} , and thus $Out (fault-free) = 1 / Out (faulty) = 0$

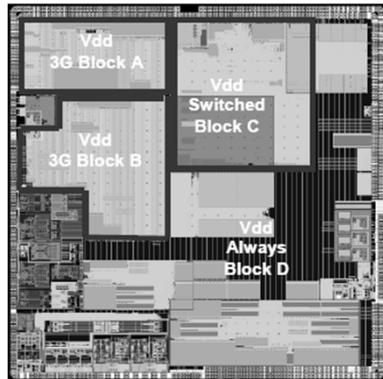
(source: Goal (NXP) et al., Proc. ETS, pp. 145-150, 2006)

92

Test for Power Management Structures



Example 2: Parametric Test of Micro Switches



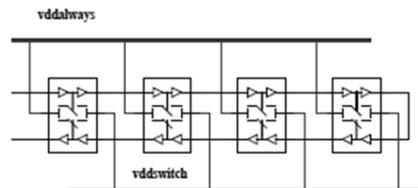
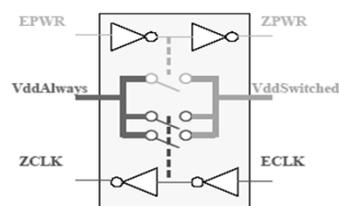
- Presented by ST-Ericson (Sophia) at International Test Conference 2008.
- Single-die 3G mobile phone base band Chip made in 65nm technology
- Includes multimedia features, such as video decoder, MP3 player, camera, games, and designed to be extremely low power.
- Rush current during power up → specific functional mode → test mode has to map functional mode !

93

Test for Power Management Structures



Example 2 (cont'd): Parametric Test of Micro Switches

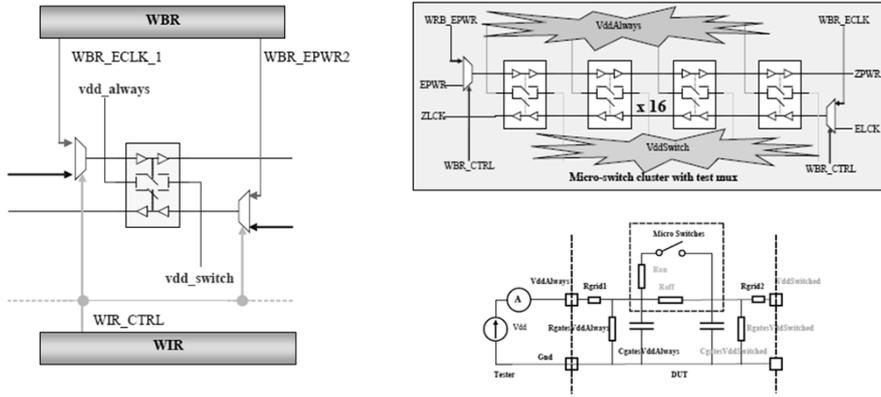


- The micro switches are daisy-chained. First, all the EPWR control signals are propagated in the chain. This gives a progressive ramp-up of the VddSwitched. Then, the ECLK control signal follows, turning 'on' all the transistors of the micro switches.
- Testing micro-switches individually is needed to detect resistive defects in each of them, and testing the micro switches' control chain is important to ensure the chain is not broken.

94

Test for Power Management Structures

Example 2 (cont'd): Parametric Test of Micro Switches



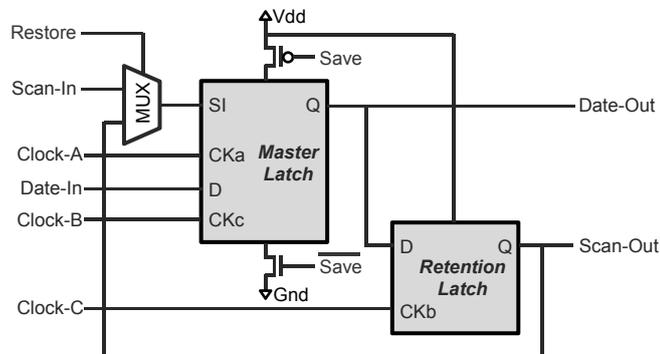
- DFT to add controllability and observability
- Test environment modeling needed to allow R_{off}/R_{on} measurement
- Test time for 150 clusters (each composed of 16 switches): 36 ms

95

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Example 3: Test for State Retention Registers (SRR's)

- A SRR cell is for keeping its state when the power supply is turned off.
- Scan function can be designed into a SRR cell.

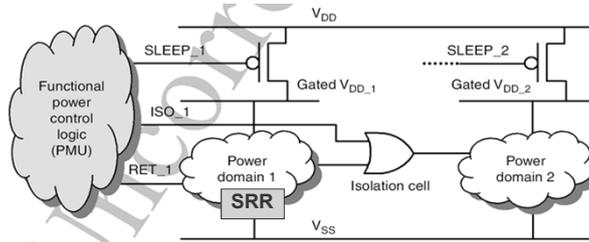


96

Test for Power Management Structures



Example 3 (cont'd): Test for State Retention Registers (SRR's)



Retention Capability Test

- (1) Shift-in value V to SRR.
- (2) Enable retention by setting *Save* to 1.
- (3) Enable the isolation cell.
- (4) Turn-off Power Domain 1.
- (5) Turn-on Power Domain 1 after a few cycles.
- (6) Disable the isolation cell.
- (7) Disable retention by setting *Restore* to 1.
- (8) Shift out the value of SRR and check if it is V .

Repeat for $V = 0$ and $V = 1$

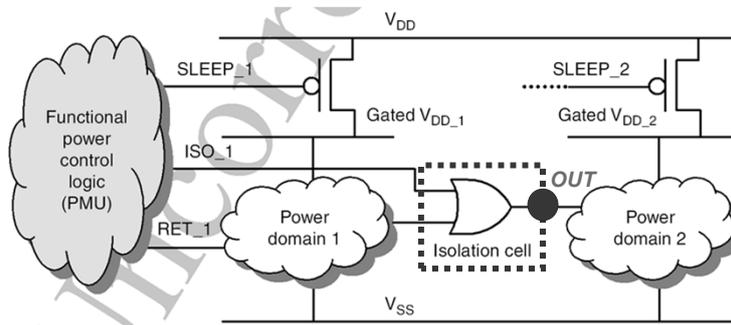
Other tests, such as test for retention robustness to the state element's clock, asynchronous set/reset, etc., may also need to be applied.

97

Test for Power Management Structures



Example 4: Test for Isolation Cells - (1)



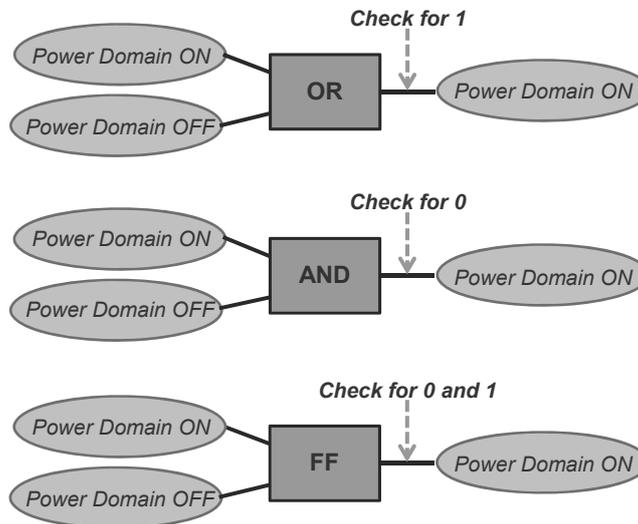
- (1) Turn-off Power Domain 1 ($SLEEP_1 = 1$).
- (2) Turn-on Power Domain 2 ($SLEEP_2 = 0$).
- (3) Set 1 to ISO_1 and check if the isolation cell output (OUT) is 1.

98

Test for Power Management Structures



Example 4: Test for Isolation Cells - (2)

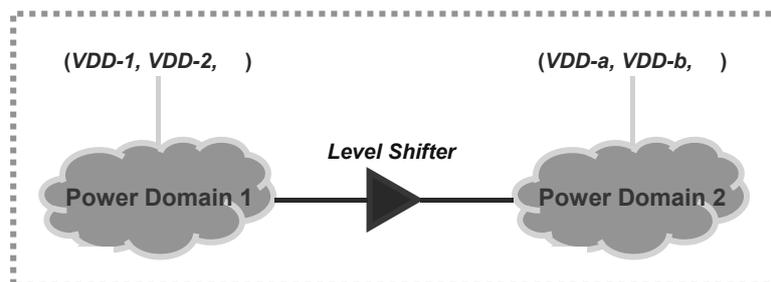


99

Test for Power Management Structures



Example 5: Test for Level Shifters

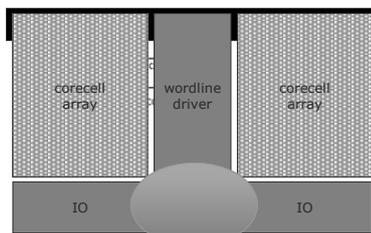
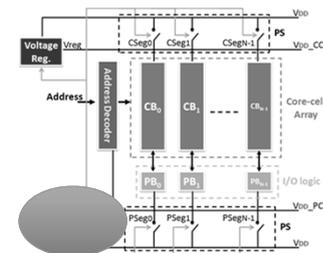


Test as a whole under all power supply voltage combinations of Power Domain 1 and Power Domain 2.

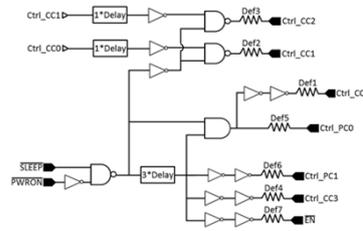
100

Test for Power Management Structures

Example 6: Test for Power Mode Control Logic in SRAMs



Low-Power SRAM



- Study performed on Intel MC products in 2011
- Impact of resistive-open defects on the PMC logic
- Definition of appropriate fault models (FFM)
- Proposal of a new March test (LZ) solution

101

Test for Power Management Structures

Summary

- More and more power management structures are used in various IC designs in order to reduce power (dynamic and static) dissipation.
- Conventional ATPG does not target power management structures, leading to potential quality problems.
- There is a strong need to fully understand the basics of various power management structures and their operation modes.
- Special considerations and even new algorithms are needed to fully test various power management structures.

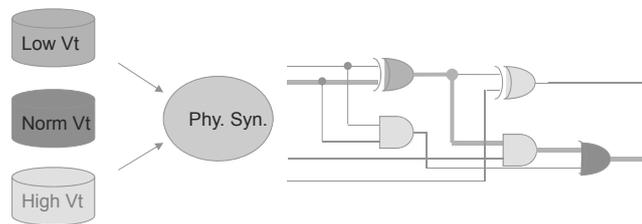
- Clock Gating Logic (Clock Gator, Control Logic)
- Power Gating Logic
 - PMU (Power Management Unit)
 - Power Switch
 - State Retention Register, Isolation Cell, Level Shifter
- Power Distribution Network

102

Impact of MTV Design on Test



- Threshold voltage scales down (with supply voltage) to deliver circuit performance, but leakage power increases exponentially with threshold voltage reduction → speed cost to decrease leakage !!
- MTV designs use high-Vt cells to decrease leakage current where performance is not critical (transistors on non-critical paths)
- Leakage power reduction while meeting timing and no area overhead
- Well established and supported by existing EDA tools



(source: CADENCE, 2007)

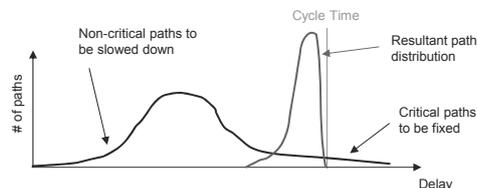
103

Impact of MTV Design on Test



- By using such power optimization techniques, more paths become clustered in a narrow region around the cycle time, resulting in a large population of paths which are sensitive to small delay perturbations

- PDF selection more complex
- More test data are needed
- Sensitivity to variations



- PSN has a significant impact on the timing behavior
- Need to integrate PSN effects in delay test pattern generation

Solutions for high quality at-speed fault coverage are needed !

104

Power-Aware DFT Tools



• Synopsys:

- Galaxy™ Test is a comprehensive test automation solution.
- DFT Compiler and its low power features (for more details on this tools, see “Power and Design for Test: A Design Automation Perspective”, A. De Colle et al, Journal of Low Power Electronics (JOLPE), Vol. 1, N° 1, April 2005)
- DFT MAX and its low power features (for more details on this tools, see “DFT MAX and Power”, R. Kapur et al, Journal of Low Power Electronics (JOLPE), Vol. 3, N° 2, August 2007)
- TetraMAX® - power-aware test patterns for defect detection
- Details
<http://www.synopsys.com/Tools/Implementation/RTLSynthesis/Test/Pages/default.aspx>

105

Power-Aware DFT Tools



• Mentor:

- Tessent™ FastScan™ and Tessent™ TestKompress™ provide comprehensive low-power and power-aware test solutions.
- Details at http://www.mentor.com/products/silicon-yield/logic_test/

• Cadence:

- Encounter® Test, a key technology in the Cadence® Encounter digital IC design platform
- To support manufacturing test of low-power devices, Encounter Test uses power intent information to create distinct test modes automatically for power domains and shut-off requirements.
- Details
http://www.cadence.com/products/ld/test_architect/pages/default.aspx

106

Conclusion



- Power consumption during Test is a real issue !!
- Not only during manufacturing test but also during on-line test
- Not only ATPG and DFT but also BIST, test compression, and test scheduling have been addressed
- No generic solution, but rather a combination of solutions. Example: power-aware DfT for reducing shift power and power-aware ATPG for reducing LTC power
- New test solutions for Low-Power Design that preserve test functionality are needed !!

107



Thank You !

108