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Low-noise and Low-power Front-end for True-tripolar ENG Amplifier

Mariam Abdallah^{1,2}, Fabien Soulier^{1,2}, Serge Bernard^{1,3}, Lionel Gouyet⁴, and Guy Cathébras^{1,2}

Abstract— Electroneurogram acquisition systems are usually based on tripolar cuff electrodes that are known to decrease noise from external sources, such as muscular fibers (EMG) or stimulation artifacts. This paper presents a preamplifier associated with this kind of electrode in a true-tripole configuration. It is designed at the transistor level to lower the number of transistors while still rejecting parasitical signals. This integration at the transistor level reduces the size, power consumption and noise of the preamplifier compared to classical true-tripolar structures.

I. INTRODUCTION

In the context of incurable neurological diseases, such as epilepsy, Parkinson's disease, stroke or spinal cord injury, surgical or pharmacological solutions are not always satisfactory restoration of sensory-motor functions affected. A workaround is then to interface the nervous system with a stimulating prosthesis by measuring electroneurogram (ENG). We are particularly interested in the acquisition of ENG signals at the peripheral nervous system which presents the opportunity to improve the functional electrical stimulation (FES) [1] [8]. Cuff electrodes which had been developed and most used in the last twenty years [2, 3] are established as a safe and reliable method of chronically recording the ENG comparing to intra-fascicular and sieve electrode [4, 5]. Typically, the neural activity measured by these electrodes is only microvolt's (1-5 μV in the 1Hz-3 kHz [6]). Moreover, the electromyogram (EMG) generated by active muscle activity which has signal amplitude in the order of 1mV presents one of the main noise sources and causes the interference with the recorded ENG. So minimizing these kinds of interferences is a main objective to be able to exploit neural signals.

There exist two amplifier configurations associated with the tripolar electrode (figure 1). First, the quasi-tripole proposed by R.Stein et al. [9] and J.Hoffer [10] is shown in figure 2 (a). This configuration is based on a screening effect achieved by shorting the outer poles. Secondly, the true-tripole configuration consists of linear combination of signals coming from the three poles (V_{in1} , V_{in2} , V_{in3}).

$$V_{out} = A (V_{in1} - (V_{in2} + V_{in3})/2) \quad (1)$$

This combination is usually realized thanks to differential amplifiers as shown in the figure 2 (b). The true-tripole has several advantages over the quasi-tripole such as: less

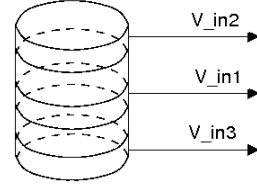


Figure 1. Tripolar cuff electrode.

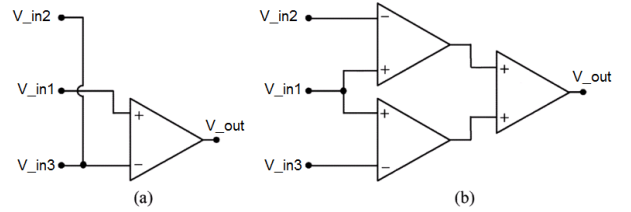


Figure 2. Tripolar ENG amplifier configurations (adapted from [11]). (a) quasi-tripole, (b) true-tripole.

sensitivity to interface impedance, better signal-to-noise ratio (SNR) and EMG rejection [11]. The drawback is that true-tripole needs three differential amplifiers where the quasi-tripole requires only one.

In this paper, we present true-tripolar preamplifier followed by a variable-gain instrumentation amplifier (IA). This preamplifier is designed at a transistor level in order to reduce the size, power consumption and noise by limiting the number of transistors. First, we present the overall structure of the acquisition channel and the detailed design of the preamplifier. The third section gives the electrical performances of the designed amplifier. A brief discussion is then interpreted and finally, the last section gives some concluding points and perspectives.

II. MATERIAL AND METHOD

The acquisition system is designed as an application specific integrated circuit (ASIC) and contains several channels. Each channel is composed of an IA associated with a preamplifier as shown in the figure 3.

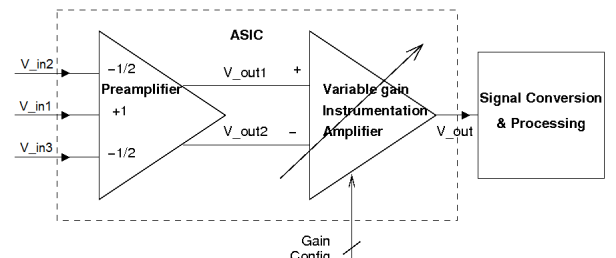


Figure 3. Overview of the true-tripolar acquisition system

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A. Overview of the structure

The circuit is designed with the AMS CMOS 0.35 μ m technology, with 3.3V supply. The preamplifier provides three functions which are:

- to combine the input signals as shown in the equation (1),
- to barely amplify the neural signal to an acceptable SNR,
- and to present a differential output to the IA.

Nevertheless, in the aim to increase and adjust the total gain of the structure this first stage is followed by an IA with variable gain. The latter is numerically controlled by a configurable network of switches and resistors in order to obtain a range of gain going from 6 dB to 80 dB for the second stage. We will use a Nexys2 FPGA card for this purpose. The SNR optimization of the IA is less critical than the preamplifier one thus it's realized with operational amplifiers from the AMS standard library.

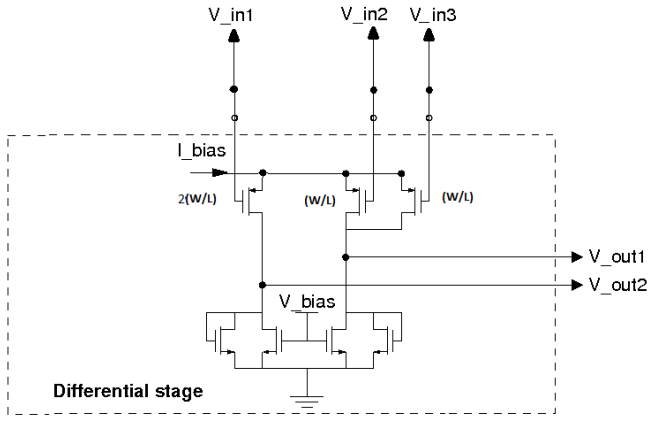


Figure 4. Three input preamplifier schematic.

B. Preamplifier

The preamplifier is designed like a differential pair whose negative input transistor is split into only two transistors (two times smaller than the positive input, figure 4). This way, it provides the same functionality as the classical true-tripolar structure with a single (3-input) differential amplifier instead of three, and with a size similar to a quasi-tripole amplifier. To improve the noise performances, we chose to use the PMOS transistors for the pair and we have optimized the size to (W/L= 150/7.5 μ m). The active load is made with NMOS transistors. Two diodes were added in parallel to bias the output voltage to 1.65V approximately. The gain of the differential pair is given by:

$$A = gm_p / gm_n \quad (2)$$

Where gm_p represents the transconductance of the P-MOS transistors connected to the inputs V_{in2} and V_{in3} while gm_n is the transconductance of the diode connected to NMOS transistors at the bottom of the schematic. To achieve the gain of 100 with consumption of $I_{bias} = 12 \mu$ A we have to chose an active load transistor size (W/L= 55/40) and diode of size (W/L=2/164.3).

III. RESULTS

A. Gains AND Rejection

Triantis et al. have shown that the EMG bio-potential has a linear spatial variation inside an insulated cuff [7]. Therefore, to suppress this parasitical signal the preamplifier needs to reject:

-the common mode

$$V_{in1} = V_{in2} = V_{in3} \quad (3)$$

-the differential parasitic mode

$$V_{in1} = 0, V_{in2} = -V_{in3} \quad (4)$$

To characterize the preamplifier, we have to simulate the output with these two modes and compare it to the main mode which is orthogonal to both.

$$V_{in1} = -2 V_{in2} = -2 V_{in3} \quad (5)$$

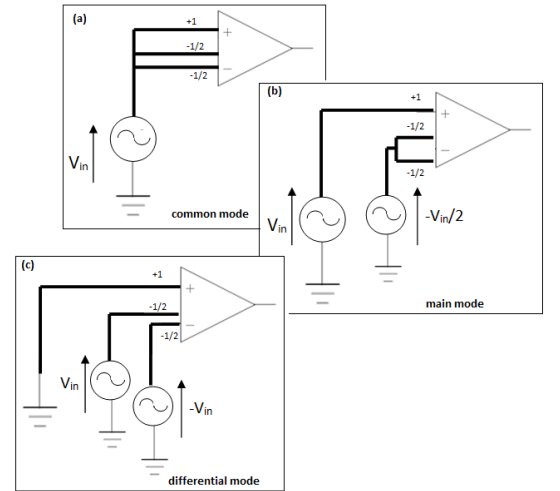


Figure 5. The three simulated modes used for preamplifier characterization: (a) comon mode, (b) differential parasitic mode, (c) main mode.

DC and AC simulations were performed for these three modes (figure 5). The results are presented in the figures 6 and 7. The main results of these simulations are:

- more than 150dB rejection ratio for the common and differential modes compared to main one.
- dynamic range of about ± 5 mV.

B. Bandwidth and noise

Fig. 7 shows 200 kHz bandwidth that is far above the needs for ENG acquisition (tenths of kHz). The estimated flicker noise due to input and load transistors is below the μ V on the required bandwidth.

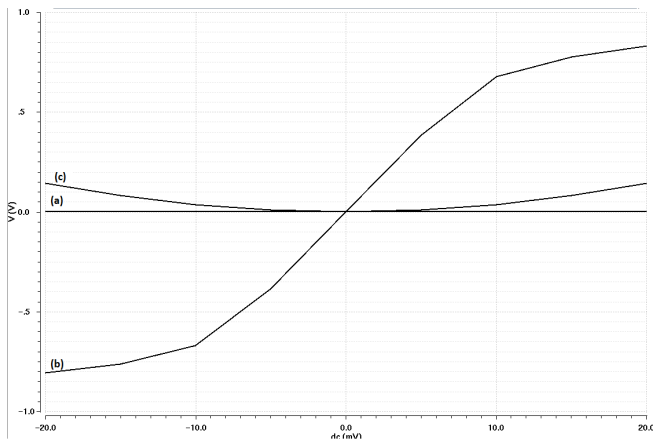


Figure 6. DC simulation result for main (b), common (a) and differential modes (c).

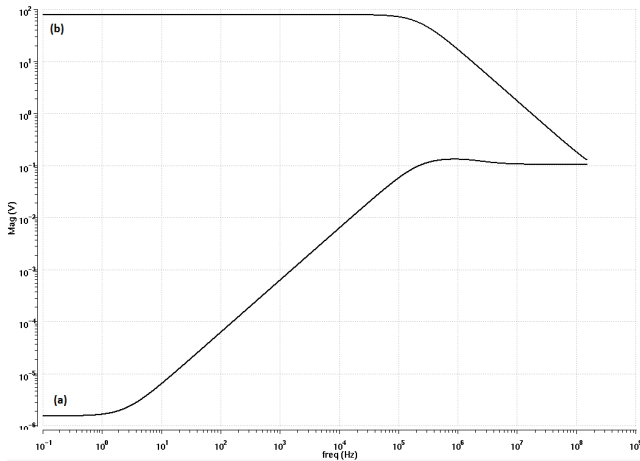


Figure 7. AC simulation result for main (b) and common (a) modes . Differential mode is too low to be simulated.

IV. DISCUSSION

Simulations show that we succeeded to achieve the requirement for the true-tripolar amplifier with much less transistors than the usual structure keeping the power consumption under 12 μ A for 3.3 V supply. The simulated rejection ratios seem very encouraging. Nevertheless, some mismatches were not simulated and the results have now to be confirmed by real measurements with the fabricated ASIC. Moreover, the estimated noise does not take in account all the sources in the circuit but only the input and load transistors, and may be measured as well.

V. CONCLUSION

In this paper, we have focused on the first stage of an acquisition system for recording electrical signal from peripheral nerves. Whereas the classical true-tripolar configuration offers an interesting parasitic signal rejection at the cost of multiplying the number of transistors, the amplifier presented in this work provides a very simple low noise, low power way to implement the true-tripolar

functionality. It offers the ability to integrate large number of channels into a single ASIC. We are working now on an experimental setup for the characterization of the ASIC to confirm simulations results presented here.

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