Accurate and Efficient Analytical Electrical Model of Antenna for NFC Applications

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"Analogue Network of Converters": a DFT Technique to Test a Complete Set of ADCs and DACs Embedded in a Complex SiP or SOC

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Abstract

In this paper, complex mixed signal circuits such as SiP or SOC including several ADCs and DACs are considered. A new DFT technique is proposed allowing the test of this complete set of embedded ADCs and DACs in a fully digital way such that only a simple low cost tester can be used. Moreover, this technique called "Analogue Network of Converters" (ANC) requires an extremely simple additional circuitry and interconnect.

1. Introduction

The market pressure for data and telecommunication applications is now driving the need for integrating very different analogue or mixed-signal blocks into a single System-in-Package (SiP) or System-On-Chip (SOC). The integration of many different functions into a single package offers several clear benefits but, on the other side, implies very significant test challenges. As an illustration of these difficulties, examples are usually reported where the test of the analogue blocks in the system may represent up to 90% of the whole test effort while these analogue blocks only represent 10% of the whole chip area.

When testing analogue blocks, the main difficulty comes from the performance requirements of the test instruments. Indeed, analogue testing is made of a long sequence of parameter characterization that is performed using very expensive instruments able to accurately measure analogue signals. In addition to these required expensive instruments, we should note that controllability and observability of deeply embedded analogue blocks are much reduced and the possibility of external testing may be limited. Also, as signals become faster and systems are operated at higher speeds, external testing become more susceptible to noise, crosstalk and probing problems.

To overcome these problems, several authors have proposed different BIST techniques where signals are internally generated and/or analysed [1-7]. Another possible and less expensive solution consists in using DFT techniques to internally transform the analogue signals into digital signals that are made controllable and observable from the chip I/Os [3,8]. As a result, only digital signals are externally handled by a non-expensive "digital" test equipment (Low Cost Tester).

In current systems, it is to mention that converters (ADCs and DACs) are one of the main components of any mixed-signal chip. Nowadays, many ADCs and DACs may be implemented in a complex SOC or SiP. For instance, the PNX8327 a PHILIPS device for set-top box applications contain 2 ADCs and 7 DACs embedded on the same SiP. Testing this whole set of converters is a very complex task requiring a long test time because of the above mentioned problems of accessibility, signal integrity, accuracy of converter parameter measurements.

In this context, this paper proposes an original DFT technique called "Analogue Network of Converters" (ANC) that permits to test the whole set of embedded ADCs and DACs. An extremely small circuitry is added to the original chip allowing to apply a fully digital test approach to the System-in-Package/System-On-Chip.

In the remainder of the paper, section 2 gives the fundamental principle of the ANC technique. In this section, the test of the set of n DACs and m ADCs is made equivalent to a system of equations where the converter characteristics are the unknowns. Section 3 explores the space of possible configurations of the network and defines the corresponding equations. In section 4, the proposed ANC technique is validated through simulations and measurements. Finally, section 5 gives some concluding remarks.

2. ANC Fundamental Principle

As often mentioned, analogue testing is classically oriented to performance characterization of a function under test. Performance characterization is obtained through a number of static and dynamic parameter estimations. Two important dynamic parameters are THD and SFDR. They are computed with the

measurement of the harmonics of the converter output signal.

2.1. Analogue Network of Converters

Considering for instance the test of a single ADC using efficient instruments, it has been demonstrated that the output signal can be represented by (1). This equation includes an ideal sampled sine wave x(n) and the sum of all the harmonic values introduced by the converter errors.

$$s(n) = x(n) + \sum_{k\geq 0} H_k^{converter} \cos(k(\theta_n + \theta_0)) \qquad (1)$$

In equation (1), n is the sample index, θ_0 the initial phase shift, $H_k^{converter}$ the amplitude of the k^{th} harmonic and θ_n is the nominal sampling phase

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n \qquad (2)$$

where M is the number of samples and P the number of periods in the record.

The above equation may also apply to the test of a single DAC, because the analogue output signal is converted into a digital sample set.

Considering a complex system with several ADCs and DACs, the objective of this paper is to measure the harmonic values $H_k^{converter}$ of each converter output signal using a fully digital way. To be fully digital from an outside chip perspective, a very simple circuitry is added to the system :

- to realize the analogue sum of any combination of DAC outputs,
- to connect the resulting sum to any combination of ADC inputs.

This DFT technique is illustrated in Figure 1. A simple OPAMP-based analogue adder can be used to implement the proposed DFT. The multiplexer control signal I_i allows to connect the corresponding DAC_i. In the same way, the multiplexer control signal O_j allows to connect the corresponding ADC_j.

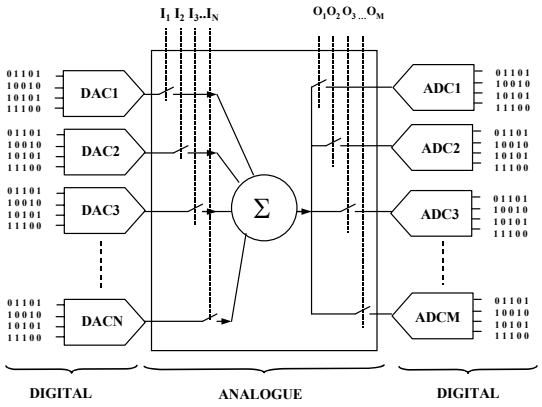

Figure 1: The ANC DFT technique

When n DACs are connected with m ADCs, this is called a configuration C(n,m). Using configuration C(1,1), the spectrum of the output signal can be computed and we can extract the values of the harmonics $H_k^{C(1,1)}$. But in this case, the output signal includes the errors of DAC1 and the errors of ADC1. In other words, the spectrum includes the harmonic contribution of DAC1 and the harmonic contribution of ADC1. So, due to the linearity of the system, we can write the following equation:

$$\sum H_k^{measure} = \sum H_k^{m} = \sum \left(H_k^{DAC1} + H_k^{ADC1}\right) \qquad (3)$$

In (3), we assume that the harmonic amplitudes created by the DAC are negligible with respect to the fundamental amplitude of the signal. Thus, we can consider the signal driving the ADC as a single tone signal. This working hypothesis will be verified in the validation phase described in section 4.

Equation (3), shows the relation between the harmonic contribution of the different converters. Indeed, in equation (3), the left member is known; it is the bins measured at the output of the ADC, while the right member represents the unknowns.

This example demonstrates the relation between one configuration and its resulting equation. This leads to the fundamental idea of the ANC DFT technique. By using different configurations C(n,m) we are able to obtain a set of different equations. So, with an adequate set of configurations (i.e; system of equations), we expect to be able to fully determine the set of unknowns, i.e. the individual harmonic contribution of each converter. The next section explores the space of possible configurations to obtain such a set of equations.

3. Configuration C(n,m)

The ANC principle consists of using different hardware configurations in terms of converter interconnections. Then, the idea is to find adequate test setup to discriminate the influence of each converter on the final response. In practice, the only test setup parameters we can easily control are the phase and the amplitude of the digital stimulus. In this section, two configurations, using DAC1 DAC2 and ADC1, are studied in order to discriminate their harmonic contributions.

3.1. Configuration C(1,1) at full scale

The first configuration considered is made up of a single DAC and a single ADC (Figure 2).

According to the harmonic contribution model (3), the influence of the two data converters on the sampled signal can be expressed by:

$$s(n) = x(n) + \sum_{k\geq 0} \left(Hdac1_k^{FS} + Hadc1_k^{FS}\right)\cos(k(\theta_n + \theta_0)) \qquad (4)$$

where $Hdac1_k^{FS}$ and $Hadc1_k^{FS}$ are respectively the k^{th} harmonic contribution of the DAC and the ADC for an input signal reaching the converter full scale. Please note that, in this study, we consider that all the converters have the same dynamic range.

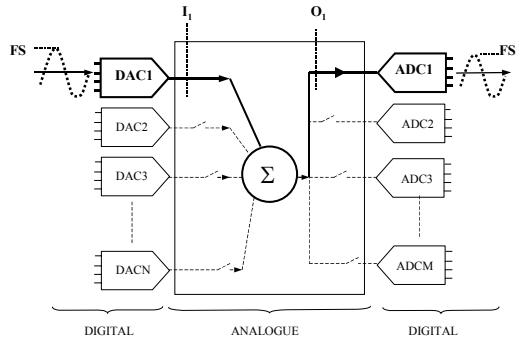

Figure 2: C(1,1) test configuration

If we only consider the three converters DAC1, DAC2 and ADC1, we generate two test setups. In a first step, a sine wave is sourced from DAC1 to ADC1, with amplitude covering the converter full-scale. The expression of $H_k^{m,a}$, the amplitude of the k^{th} harmonic measured on the ADC output is given by:

$$H_k^{m,a} = Hdac1_k^{FS} + Hadc1_k^{FS} \quad (5)$$

In the second step, the test path goes through DAC2 and ADC1. The amplitude of the test signal still reaches the full scale of the converters. Therefore, we obtain a second equation given by (6), where $H_k^{m,b}$ is the amplitude of the k^{th} harmonic measured on the ADC output.

$$H_k^{m,b} = Hdac2_k^{FS} + Hadc1_k^{FS} \quad (6)$$

At this point, we have three unknown parameters ($Hdac1_k^{FS}, Hdac2_k^{FS}, Hadc1_k^{FS}$) and only two equations (5 and 6) .

One could think to play with the amplitude and phase of the input signal to establish new equations. Unfortunately, variations of these test setup parameters give no additional independent information to discriminate the influence of each converter on the final response. Indeed, the input signal phase has no influence on the converter harmonic contribution and even if the input signal amplitude A_{in} modifies the converter harmonic contribution ($Hdac1_k^{A_{in}} \neq Hdac1_k^{FS}$ if $A_{in} \neq FS$), each new acquisition would give a new equation but also two new unknown parameters ($Hdac\,1_k^{A_{in}}$, $Hadc\,1_k^{A_{in}}$). To avoid this problem, the two DACs output can be added to establish a new configuration. This new configuration is called C(2,1) and is described in the next section.

3.2. Configuration C(2,1) at full scale

The second hardware configuration is made up of two DACs and one ADC. The input of the ADC is the sum of the two DAC outputs.

Unfortunately, considering three converters with the same resolutions, the sum of two full-scale signals from DAC1 and DAC2 with no relative phase shift is twice the converter full scale and would saturate the ADC.

The solution to overcome this problem is to introduce a relative phase shift of $2\pi/3$ between the two input signals (Figure 3)

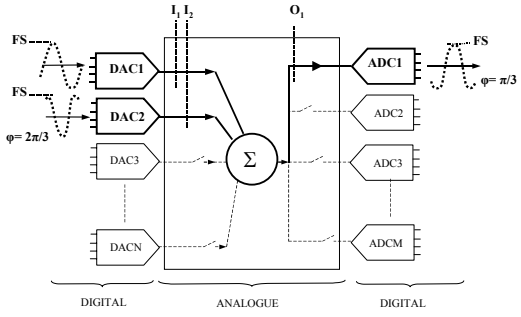

Figure 3: Third test setup

The sum of the two DAC outputs is a full-scale signal; this property is mathematically explained by (7)

$$\cos\left(x+\frac{2\pi}{3}\right)+\cos(x)=2\cos\left(x+\frac{\pi}{3}\right)\cos\left(\frac{\pi}{3}\right)=\cos\left(x+\frac{\pi}{3}\right) \quad (7)$$

We obtain (11), the third equation,

$$H_k^{m,c} = Hdac1_k^{FS} + Hdac2_k^{FS}\cos(k2\pi/3) + Hadc1_k^{FS}\cos(k\pi/3) \quad (8)$$

where $H_k^{m,c}$ is the amplitude of the k^{th} harmonic measured on the ADC output. So finally, we obtain the following equation system for each k^{th} harmonic contribution:

$$\begin{cases} H_k^{m,a} = Hdac1_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,c} = Hdac\,1_k^{FS} + Hdac\,2_k^{FS}\cos(k2\pi/3) + Hadc\,1_k^{FS}\cos(k\pi/3) \end{cases}$$

This system would enable the discrimination of the harmonic contribution of every converter if the three equations were independent. This condition is not verified for harmonic components that are of a prime order and greater than three. Indeed for these harmonics, the third equation is a linear combination of the two other equations.

We have observed a similar limitation whatever the relative phase shift introduced between the two input signals. So, this 3-equation system permits to discriminate the 4 first harmonics, but is not sufficient to calculate the THD or the SFDR. To go further and discriminate more harmonics, it is necessary to vary the input signal amplitude, as described in following sections.

3.3. Configuration C(1,1) and C(2,1) at ½ FS

The second parameter we can control is the input signal amplitude. As previously explained (cf3.1) the use of different amplitudes induces additional unknown parameters. Nevertheless, it also introduces new test setup possibilities that can be exploited to get additional independent useful information.

Practically, we have looked for a system of equations that allows the discrimination of the three converter

harmonic contributions, $\mathrm{Hdacl}_k^{FS}, \mathrm{Hdac2}_k^{FS}, \mathrm{Hadcl}_k^{FS}$ using test stimuli with amplitude at full-scale and amplitude at ½ full-scale.

The new third equation is the result of a test at ½ full scale through DAC2 and ADC1

The measured harmonics are the sum of DAC2 and ADC1 harmonic contributions for an input signal at ½ full-scale.

$$H_k^{m,c} = \mathrm{Hdac2}_k^{FS/2} + \mathrm{Hadcl}_k^{FS/2} \quad (9)$$

due to this test we have 5 unknowns and only 3 equations. To solve the system we need to have the same number of unknowns and equations. As a consequence C(2,1) configuration with both amplitude and phase variation, is used to establish the two last equations. The 4th test setup involves a full-scale input signal on DAC1 and a ½ full-scale input signal on DAC2 with a ⦸ phase shift (Figure 4). The resulting signal at the ADC input is a sine wave at ½ full-scale:

$$\cos(x) + \frac{\cos(x+\pi)}{2} = \cos(x) - \frac{\cos(x)}{2} = \frac{\cos(x)}{2} \quad (10)$$

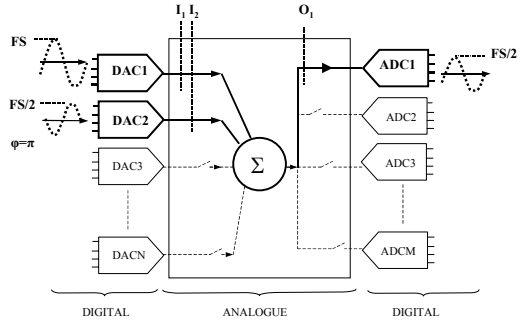

Figure 4: Fourth test setup

The resulting equation is the sum of the harmonic contribution at full-scale of DAC1, the harmonic contribution at ½ full scale of DAC2 balanced by the phase shift and the harmonic contribution at ½ full scale of ADC1.

$$H_k^{m,d} = \mathrm{Hdac1}_k^{FS} + \mathrm{Hdac2}_k^{FS/2}\cos(k\pi) + \mathrm{Hadc1}_k^{FS/2} \quad (11)$$

The 5th and last required test is very similar to the previous one. The input amplitudes are the same but they are relatively phase shifted of φ_1. The resulting signal at ADC input is now a sine wave at full-scale with a phase shift of φ_2.

$$\cos(x) + \frac{\cos(x+\varphi_1)}{2} = \cos(x+\varphi_2) \quad (12)$$

$$\text{with } \varphi_1 = \pi - 2\arccos\left(\frac{1}{4}\right),\ \varphi_2 = \pi - \arccos\left(\frac{1}{4}\right) \quad (13)$$

The 5th equation then corresponds to the sum of the harmonic contributions balanced by their phase shift:

$$H_k^{m,e} = \mathrm{Hdacl}_k^{FS} + \mathrm{Hdac2}_k^{FS/2}\cos(k\varphi_1) + \mathrm{Hadcl}_k^{FS}\cos(k\varphi_2) \quad (14)$$

In summary, the proposed test strategy is composed of five successive tests. Each test consists in an acquisition and a spectral analysis (with Fast Fourier Transform) to evaluate harmonic bins. We obtain a 5-equation system for each harmonic bin:

$$\begin{cases} H_k^{m,a} = \mathrm{Hdac1}_k^{FS} + \mathrm{Hadc1}_k^{FS} \\ H_k^{m,b} = \mathrm{Hdac2}_k^{FS} + \mathrm{Hadc1}_k^{FS} \\ H_k^{m,c} = \mathrm{Hdac2}_k^{FS/2} + \mathrm{Hadc1}_k^{FS/2} \\ H_k^{m,d} = \mathrm{Hdac\,1}_k^{FS} + \mathrm{Hdac\,2}_k^{FS/2}\cos(k\pi) + \mathrm{Hadc\,1}_k^{FS/2} \\ H_k^{m,e} = \mathrm{Hdacl}_k^{FS} + \mathrm{Hdac2}_k^{FS/2}\cos(k\varphi_1) + \mathrm{Hadcl}_k^{FS}\cos(k\varphi_2) \end{cases}$$

This system of independent equations is sufficient to calculate the value of the required harmonic contributions ($\mathrm{Hdacl}_k^{FS}, \mathrm{Hdac2}_k^{FS}, \mathrm{Hadcl}_k^{FS}$). It allows thus a fully independent characterization of the three converters of the C(2,1) configuration in terms of harmonic contributions.

3.4. Configuration C(n,m)

Thanks to the converter characterization obtained from the C(2,1) configuration, it seems easy to test every other converter embedded in the complex chip.

The idea is to use one of the three previously characterized converters as a measurement instrument whose non-ideal features are well known.

The first step consists in using the C(2,1) configuration to characterize the three first converters (ADC1, DAC1 and DAC2). Then, DAC1 can be used to characterize the harmonic contribution of each ADCi in the chip by using only one digital stimulus at full-scale to obtain the following additional equations:

$$H_k^{m,j} = \mathrm{Hdac1}_k^{FS} + \mathrm{Hadci}_k^{FS} \quad (15)$$

In the same way, ADC1 can be used to characterize all the DACs present within the system.

Concerning test time, it directly depends on the number of required acquisitions. The first step of the test procedure needs five acquisitions to test three devices. Then, only one additional acquisition per device under test is needed. So, the number of acquisitions for a complex chip with n DACs and m ADCs is only of n+m+2 acquisitions without any external analogue equipment requirement.

Moreover, because only digital ATE resources are required, it is conceivable to test several converters at the same time. Consequently, after the first step, each new step could use simultaneously all available characterized converters as measurement instruments. In this configuration, the testing time could be drastically reduced.

4. Validation

A number of simulations have been conducted to validate the proposed approach. The converter model used for simulation is first introduced, then the simulation setup is defined, and finally simulation results are presented. The performance of the proposed test strategy is discussed in terms of estimation error on

the harmonic components and on the dynamic parameters.

4.1. Data converter model

In order to simulate the test strategy, we need to establish a model that takes into account the effects of the converter non-idealities. Three main sources of errors will be considered, i.e. the sampling jitter of the converter, the non-linearities of its transfer function and the thermal noise.

Let us consider r(n) an input sine wave passing through an ideal converter and affected by the jitter, Jt, and the thermal noise, Nth.

$$r(n) = 2^N \left(\frac{V_0}{V_{FS}} \right) \cos(\theta_n + J_t + \theta_0) + 2^N \left(\frac{V_{DC}}{V_{FS}} \right) + N_{Th} \quad (16)$$

where N and V_{FS} respectively represent the number of bits and the full-scale voltage of the converter, V_0 and V_{DC} respectively correspond to the amplitude and the DC component of the input sine-wave, and θ_0 and θ_n are respectively the initial and nominal sampling phase of the signal. $J_t = 2\pi f_0 \delta_t$, with f_0 the frequency of the input signal and δ_t a centred Gaussian noise. The thermal noise is usually modelled by a centred Gaussian noise.

The second significant source of errors that has to be considered is the non-linearity of the converter transfer function. In order to alleviate this drawback, we choose an approach that consists in using "true" INL curves extracted from measurements on real data converters. Consequently, let us consider s(n) the signal deteriorated by the two types of errors:

$$s(n) = [\, r(n) + INL([r(n)]) \,] \quad (17)$$

where INL(x) is a non-linearity curve measured through histogram testing of a real converter. This non-linearity curve is indexed by the rounded signal including the sampling jitter effect [r(n)]. The complete equation is rounded to model the quantization effect.

Equation (17) is the equation that models the deterioration of a sine-wave signal passing through a converter affected by sampling jitter, transfer function non-linearities and thermal noise. This equation has been used for the simulations described in the following sections.

4.2. Simulation setup

In order to validate the proposed test strategy, we have conducted a number of simulations considering data converters of the same resolution and sampling frequency. The objective is to compare the values of the harmonic components evaluated using the proposed strategy to the ones obtained using a classical stand-alone test.

In an initial phase, we have performed measurements on real data converters to extract INL curves. Practically, these INL curves have been determined by performing a histogram test on 15 different PHILIPS 12-bits ADC TDA9910. Using equation (17), we can therefore model 15 different converters. Then we have conducted two sets of simulation:

At first, we have considered each data converter in a stand-alone configuration to get reference values.

Then, we have considered five different C(2,1) configurations, with every time three different converters. For each C(2,1) configuration, we have simulated the test algorithm described in section3.3.

4.3. Results and discussion

As an example, Figure 5 presents the results obtained for one converter. The amplitude of the harmonic components evaluated using the C(2,1) configuration (grey bins) are compared to the amplitude of the harmonic components computed using the classical stand-alone test configuration (black bins).

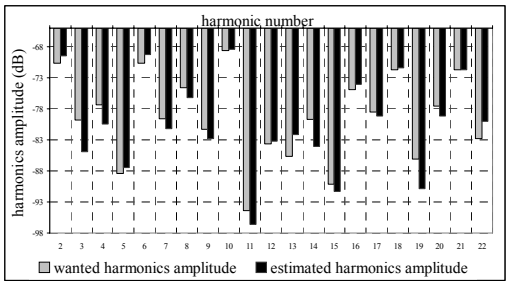

Figure 5: 20 harmonics of one converter

The maximum estimation error observed on the amplitude of the first 20 harmonic components is about 5dB. However, it is worth nothing that this error is observed for a harmonic component of very small amplitude (≈-85dB). Considering only the major harmonic components with amplitude higher than –75dB, the observed estimation error remains below 2dB. These results show the efficiency of the proposed strategy that permits an accurate evaluation of the converter harmonic components.

Similar simulations have been performed for the complete set of 15 different converters. Results are summarized in Table 1 that reports the maximum estimation error observed on the amplitude of the first 20 harmonic components for the different converters. Results have been classified in three ranges according to the amplitude of the harmonics.

Table 1: Estimation error

Maximum Error for Ranges of Wanted Amplitudes (dB)							
Conv.	h>-75dB	-75dB>h h>-85dB	-85dB>h		h>-75dB	-75dB>h h>-85dB	-85dB>h
#1	0,28	-7,99	-16,84	#9	0,25	8	6,58
#2	-0,64	7,58	-19,23	#10	3,5	1,03	3,7
#3	0,36	7,62	3,55	#11	-0,1	-2,1	-2,96
#4	-0,26	6,1	-8,49	#12	-0,29	-1,02	22,9
#5	-0,25	0,91	11,6	#13	-0,37	1,2	4,59
#6	0,33	-1,89	5,73	#14	0,14	3,17	14,2
#7	0,24	-3,73	-18,16	#15	0,45	-4,84	5,42
#8	0,39	2,1	-22,31				

Analyzing these results of Table 1, it can be seen that the higher is the amplitude of the harmonic component, the lower is the estimation error. On the complete set of 15 converters, the maximum estimation error remains below 3.5dB for harmonic components with amplitude higher than -75dB, 8.00dB for harmonic components with amplitude between -75dB and -85dB, and 22.31dB for harmonic components with amplitude smaller than -85dB. Despite of few significant estimation errors, the estimated values are still in the amplitude range of the wanted harmonics. This is a satisfactory result, taking into account that the purpose of the test is to distinguish converters that exhibit poor performances, i.e. converters that present harmonic components with high amplitude (typically higher than 75dB for a 12-bit converter).

To further validate the efficiency of the proposed strategy, we have evaluated two classical dynamic parameters, namely the Total Harmonic Distortion (THD) and the Spurious-Free Dynamic Range (SFDR), for the 15 different converters. These parameters are evaluated from the spectral distribution. Results are summarized in Table 2, which reports the THD/SFDR values computed using the stand-alone configuration and the THD/SFDR values computed using the C(2,1) configuration, and the corresponding estimation error

Table 2: THD and SFDR estimation error

Converter Number	Wanted THD (dB)	THD estimation (dB)	THD error (dB)	Wanted SFDR (dB)	SFDR Estimation (dB)	SFDR error (dB)
#1	-59.1	-59.0	-0.1	68.8	69.3	-0.5
#2	-58.0	-57.9	-0.1	69.3	69.9	-0.6
#3	-58.2	-58.2	0	67.9	67.5	0.4
#4	-64.3	-63.9	-0.4	69.4	68.9	0.5
#5	-66.7	-66.9	0.2	70.9	71.1	-0.2
#6	-61.7	-58.8	-2.9	63.4	64.2	-0.8
#7	-48.1	-48.1	0	67.1	66.3	0.8
#8	-62.7	-62.2	-0.5	65.4	64.7	0.7
#9	-60.7	-60.9	0.2	64.9	65.5	-0.6
#10	-59.7	-59.7	0	62.2	62.2	0
#11	-61.5	-61.8	0.3	64.0	65.1	-1.1
#12	-61.6	-61.4	-0.2	62.8	62.8	0
#13	-70.4	-69.6	-0.8	71.1	67.4	3.7
#14	-55.5	-55.6	0.1	65.0	65.0	0
#15	-64.0	-63.6	-0.4	68.6	68.4	0.2

Analyzing these results, it can be seen that the proposed strategy enables a very accurate measurement of both these dynamic parameters, with an estimation error that remains below 3.7dB for the 15 different converters considered in the experiment. Note that such a low estimation error actually corresponds to the accuracy range that we can expect for the measurement of these parameters taking into account fluctuations in the test environment. Indeed, the reference values computed here with the stand-alone configuration are obtained considering ideal test instruments. However in a real environment, the repeatability of the measurements is impacted by unavoidable fluctuations in the test instrumentation. As a result, it is very classical to observe dispersion in the range of 5 to 10% when measuring the THD and SFDR parameters in a real environment.

5. Conclusion

This paper has introduced the novel concept of "Analogue Network of Converters" (ANC) to test distortion of embedded converters. Thanks to this approach we have demonstrated that is possible to solve the problem of expensive instruments in testers by achieving a fully digital test. Moreover by using embedded DSP, it could be possible to implement a complete BIST setup. This is a breakthrough in the domain of BIST strategy and data converter tests.
Our test strategy is well suited to SiP components. They are complex components, containing several DACs and ADCs. In addition to this complexity of design, there is a complexity of test due to reduced blocks observability and controllability.

The further works would consist in a validation by experimentation and evaluation of the robustness by varying several parameters like: different amplitudes between converters or various data converter resolutions.

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