Simulating Laser Effects on ICs, from Physical Level to Gate Level: a comprehensive approach

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I. INTRODUCTION

Laser shots on secure ICs have proven to be a very effective mean to perform fault attacks. As depicted in Figure 1, due to photo-electric effects, laser can induce transient pulses on gate output and thus generate faults in downstream registers.

It is therefore essential for designers of secure devices to have a CAD environment to check the resistance of the circuits against laser attacks and/or to validate the effectiveness of countermeasures during early stage of the design cycle without requiring actually manufacturing some prototype. In this paper we present a complete environment for modeling and simulating the laser effects on circuits during the synthesis step. It takes into account laser parameters and relies on circuit layout information

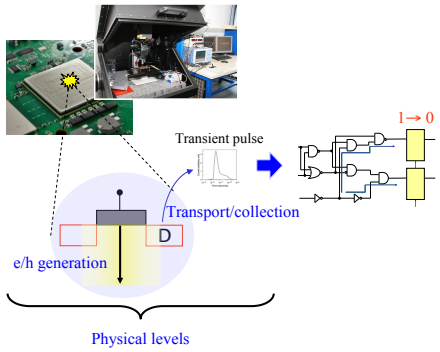

Figure 1. Physical level including laser modeling and transport/collection modeling.

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II. LASER PHYSICAL MODELING

Laser effects on electronics are very similar to effects induced by radiations in the sense that both laser and radiations generate electron-hole pairs in the semi-conductor; the charges are transported into the media and are collected at the electrodes of the device. In order to model these phenomena, a complete description of "MUSCA SEP3" (MUlti-SCAles Single Event Phenomena Predicted Platform) is provided in [1]. It is based on a Monte Carlo approach, and consists in sequentially modeling all the physical and electrical mechanisms.

A. Silicon-laser interaction modeling

Pulsed lasers generate electron-hole pairs by photo-ionization process, ionizing mechanisms are addressed in detail in [2]. If linear absorption in semiconductor is considered (low doping level), the linear transfer energy (LET) can be defined by the equation (1):

$$LET(z) = \frac{\alpha.\lambda.E_{e/h}}{\rho.h.c}.E_{laser}.e^{-\alpha.x} \quad (1)$$

α is the absorption coefficient in cm^{-1}, λ is the pulsed laser wavelength in nm, $E_{e/h}$ is the energy required to induce an electron-hole pair in eV, ρ is the Si density in mg/cm^3, h is the Planck constant, c the light velocity and E_{laser} the laser energy. Equation (1) allows for calculating the LET as a function of the depth penetration z. Since, differently from particles, laser beam does not have a punctual effect, it is necessary to define the radial deposition of the charges. Thus, the equation (2) describes the radial profile of the deposited charge:

$$I(r,z) = I_o(z).e^{-\frac{2.r^2}{\omega(z)^2}}.E_{laser}.e^{-\alpha.z} \quad (2)$$

$$\text{with } \omega(z)^2 = \omega_o^2.\left(1+\left(\frac{\lambda.(z-z_o)}{\pi.n.\omega_o^2}\right)^2\right)$$

ω_o is "beam waist" i.e. the beam width for the focalization point ($z = z_o$) and n is the refraction index.

Thanks to equations (1) and (2), it is possible to describe the 3-dimensionnal charge deposition on the semi-conductor material.

B. Carrier transport and charge collection modeling

Carrier generation and transport in the silicon active area is the most important part of the simulation flow and significantly influences the accuracy of collection-charge assessment. MUSCA SEP3 calculates the transient-current response based on the underlying physics phenomena, including field modulation, multiple-node charge collection, and ambipolar diffusion. The model is time-adapted to a Monte-Carlo approach of the SEE prediction problematic.

C. Technological and design description

Required information are directly extracted from layout files in GDS format (General Design Specification) such as the areas and positions of the active layer. Figure 2 illustrates all active junction extracted from a NAND cell GDS file (0.35-µm technology).

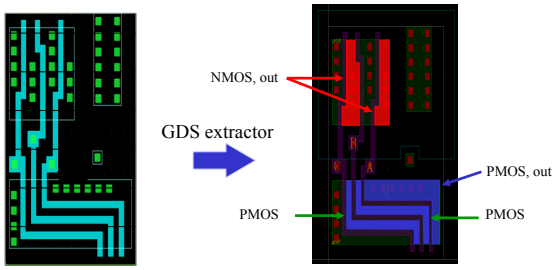

Figure 2. GDS extractor applied to academic NAND cell

The representative 3D structure for Monte-Carlo

simulation only contains N and P active junctions (drains and sources) of the design. The global collection volume takes into account the depletion capacitance of Drain-Substrate junction.

Transient currents issued from physical model can be injected on each illuminated collection node, i.e., the drain of each transistor. Doing so, the electrical model of the transient pulses can be associated with the circuit netlist. The link between the layout and the netlist is performed in our flow thanks to the "Calibre" tool.

III. ELECTRICAL/LOGIC-LEVEL LASER MODELING

A. Electrical-level laser-induced fault model

According to the physical level model described in previous section, the laser effect is modeled as a plug-in current source for each illuminated junction as depicted in Figure 3.

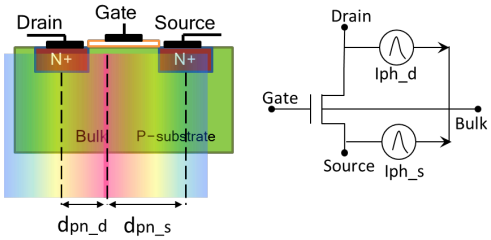

Figure 3. Simple electrical model for a large spot laser-induced fault

In order to link the physical-level models and the electrical-level models for simulation purpose, we developed a database. The database contains a set of files, each file corresponds to a standard cell in library and to a laser configuration data (energy, spot size). In each file, the transient current pulses I(t) are enumerated for each collection zone according to the position of the laser for each logic state of the standard cell.

This database therefore provides access to the different transient currents on each standard cell according to the laser characteristics. The previously described physical-level models are for the calculation of I(t). However, the goal is to use these currents in electrical-level simulations. Thus, the format of database clearly indicates the different names for each zone having collected a current to link the list of I(t) and the information circuits.

B. logic-level laser-induced fault model

Abstraction of physical perturbations into higher-level fault models is the common practice to improve the performances of fault simulators and other conception/test tools. For instance, the Stuck-At fault model together with circuit modeling at logic level allows dealing with very large circuits. However, for laser-induced fault attacks, laser is triggered intentionally within a certain instant. In this case, the classical Stuck-At fault simulation is no longer applicable because it is necessary to take the duration of the fault pulse and the delay of nets and gates into account. Therefore, the logic-level timing simulation is required and the logic-level simulator must be able to read the Delay-Annotated file, which provides information related to the delays of each gate in the Standard Delay Format (.sdf).

IV. MULTI-LEVEL FAULT SIMULATION

In our approach, a multi-level simulator "tLIFTING" [3] is chosen because it contains transistor-level simulator for describing laser-induced fault model and logic-level simulator for whole circuit simulation. In additional, an integrated layout parser can locate the affected transistors within the illuminated zone. As an open-source tool, it was expanded to read the database that is generated by "MUSCA SEP3". Figure 4 sketches the whole architecture of the two different level simulators.

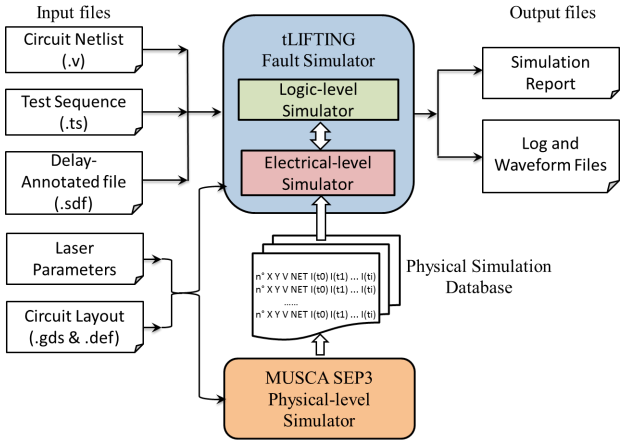

Figure 4. From physical-level to logic-level laser-induced faults simulation architecture

The simulation process is presented in Figure 5. Starting from the laser's parameters, it is possible to extract the affected p-n junctions and look up the corresponding I(t) from physical-level simulation database. With these fault current descriptions, the faults are modeled and injected into the transistor-level circuit element description. After the transistor-level fault simulation for the affected gates, if the perturbation changes the state(s), the difference(s) will be translated to logic-level and returned to the whole circuit to finish the fault simulation at logic-level.

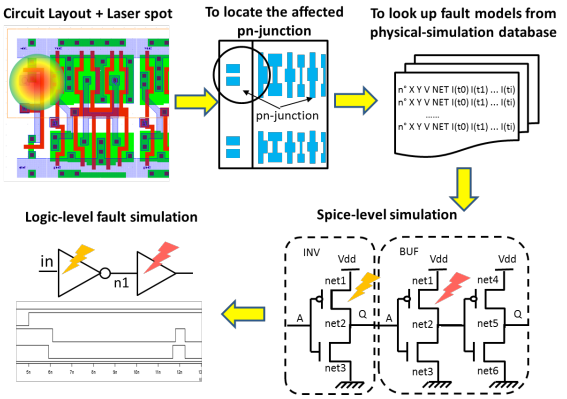

Figure 5. The multi-level laser-induced fault simulation process

V. ACKNOWLEDGEMENTS

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