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Simulating Laser Effects on ICs, from Physical Level to Gate Level: a comprehensive approach

F. Lu, G. Di Natale, M.-L. Flottes, B. Rouzeyre
LIRMM (Université Montpellier II / CNRS UMR 5506)
Montpellier, France
{lu, dinatale, flottes, rouzeyre}@lirmm.fr

G. Hubert
ONERA,
Toulouse, France
guillaume.hubert@onera.fr

I. INTRODUCTION
Laser shots on secure ICs have proven to be a very effective mean to perform fault attacks. As depicted in Figure 1, due to photo-electric effects, laser can induce transient pulses on gate output and thus generate faults in downstream registers.

It is therefore essential for designers of secure devices to have a CAD environment to check the resistance of the circuits against laser attacks and/or to validate the effectiveness of countermeasures during early stage of the design cycle without requiring actually manufacturing some prototype. In this paper we present a complete environment for modeling and simulating the laser effects on circuits during the synthesis step. It takes into account laser parameters and relies on circuit layout information

![Figure 1.](Image) Physical level including laser modeling and transport/collection modeling.

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II. LASER PHYSICAL MODELING
Laser effects on electronics are very similar to effects induced by radiations in the sense that both laser and radiations generate electron-hole pairs in the semiconductor; the charges are transported into the media and are collected at the electrodes of the device. In order to model these phenomena, a complete description of “MUSCA SEP3” (Multi-SCAles Single Event Phenomena Predicted Platform) is provided in [1]. It is based on a Monte Carlo approach, and consists in sequentially modeling all the physical and electrical mechanisms.

A. Silicon-laser interaction modeling
Pulsed lasers generate electron-hole pairs by photo-ionization process, ionizing mechanisms are addressed in detail in [2]. If linear absorption in semiconductor is considered (low doping level), the linear transfer energy (LET) can be defined by the equation (1):

\[ \text{LET}(z) = \frac{\alpha_{\text{abs}} E_{\text{z}}}{\rho \cdot c} \cdot E_{\text{laser}} \cdot e^{-\alpha z} \]

\( \alpha \) is the absorption coefficient in \( \text{cm}^{-1} \), \( \lambda \) is the pulsed laser wavelength in nm, \( E_{\text{abs}} \) is the energy required to induce an electron-hole pair in \( \text{eV} \), \( \rho \) is the Si density in \( \text{mg/cm}^3 \), \( h \) is the Planck constant, \( c \) the light velocity and \( E_{\text{laser}} \) the laser energy. Equation (1) allows for calculating the LET as a function of the depth penetration \( z \). Since, differently from particles, laser beam does not have a punctual effect, it is necessary to define the radial deposition of the charges. Thus, the equation (2) describes the radial profile of the deposited charge:

\[ I(r, z) = I_0(z) \cdot e^{\frac{r^2}{\alpha(z) \cdot o^2}} \cdot E_{\text{laser}} \cdot e^{-\alpha z} \]

with \( \alpha(z) = \frac{\lambda(z - z_o)}{\pi \cdot n \cdot o^2} \)

\( o_o \) is "beam waist" i.e. the beam width for the focalization point \( (z = z_o) \) and \( n \) is the refraction index.

Thanks to equations (1) and (2), it is possible to describe the 3-dimensional charge deposition on the semiconductor material.

B. Carrier transport and charge collection modeling
Carrier generation and transport in the silicon active area is the most important part of the simulation flow and significantly influences the accuracy of collection-charge assessment. MUSCA SEP3 calculates the transient-current response based on the underlying physics phenomena, including field modulation, multiple-node charge collection, and ambipolar diffusion. The model is time-adapted to a Monte-Carlo approach of the SEE prediction problematic.

C. Technological and design description
Required information are directly extracted from layout files in GDS format (General Design Specification) such as the areas and positions of the active layer. Figure 2 illustrates all active junction extracted from a NAND cell GDS file (0.35-μm technology).

![Figure 2.](Image) GDS extractor applied to academic NAND cell

The representative 3D structure for Monte-Carlo
simulated laser-induced fault model and logic-level simulator for whole circuit simulation. In additional, an integrated layout parser can locate the affected transistors within the illuminated zone. As an open-source tool, it was expanded to read the database that is generated by “MUSCA SE3”. Figure 4 sketches the whole architecture of the two different level simulators.

**Figure 4.** From physical-level to logic-level laser-induced faults simulation architecture

The simulation process is presented in Figure 5. Starting from the laser’s parameters, it is possible to extract the affected p-n junctions and look up the corresponding I(t) from physical-level simulation database. With these fault current descriptions, the faults are modeled and injected into the transistor-level circuit element description. After the transistor-level fault simulation for the affected gates, if the perturbation changes the state(s), the difference(s) will be translated to logic-level and returned to the whole circuit to finish the fault simulation at logic-level.

**Figure 5.** The multi-level laser-induced fault simulation process

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