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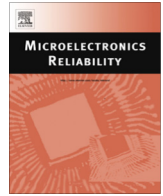
Voltage scaling and aging effects on soft error rate in SRAM-based FPGAs

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ABSTRACT

This work investigates the effects of aging and voltage scaling in neutron-induced bit-flip in SRAM-based Field Programmable Gate Array (FPGA). Experimental results show that aging and voltage scaling can increase in at least two times the susceptibility of SRAM-based FPGAs to Soft Error Rate (SER). These results are innovative, because they combine three real effects that occur in programmable circuits operating at ground-level applications. In addition, a model at electrical level for aging, soft error and different voltages in SRAM memory cells was described to investigate by simulation in more details the effects observed at the practical neutron irradiation experiment. Results can guide designers to predict soft error effects during the lifetime of devices operating in different power supply mode.

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1. Introduction

SRAM-based Field Programmable Gate Arrays (FPGAs) are very attractive to critical applications because they provide high logic density with reasonable performance capability. In addition, reconfigurability in the field allows to update circuit's configuration and to correct them remotely in harsh environments [1]. Aging and soft errors have become the two most critical reliability issues for nano-scaled CMOS designs. Aging is defined as a set of degeneration effects, such as Hot-Carrier Injection (HCI), electromigration, and Bias Temperature Instability (BTI) and others. Negative BTI (NBTI) affects PMOS transistors, increasing their threshold voltage and is considered to be the most important long-term effect to degrade circuit performance. It increases transistor-switching delays that may eventually lead to timing errors. The impact of NBTI on SRAM cells performance has been under research and NBTI modelling in static and dynamic operation has been investigated [2].

Various timing errors in CMOS designs can be avoided by reducing the clock frequency of the circuit during its lifetime. However, the impact of the transistor switching delay may lead to an increase in the susceptibility to neutron-induced bit-flip in SRAM memory cells due to its slow answer to signal recovery, as discussed in [3,4]. High-energy neutrons are produced in nuclear

cascade showers created by nuclear spallation reactions between cosmic rays (mainly protons) and atmospheric nuclei (nitrogen and oxygen) and reach the ground level. According to the altitude and position on Earth it may have different neutron fluxes. Neutron-induced soft errors can occur due to the interaction of neutrons and the material producing secondary particles [5].

These particles can ionize the sensitive p–n junctions, which may collect some charge. If the collected charge in the struck node is higher than the critical charge (Q_{crit}) of the junction node, an undesirable transient current pulse is generated that is characterized as a soft error. Systems operating in harsh environments during long period of time, *e.g.* in automotive, medical, and avionic applications, are the most critical ones as they are stressed during their lifetime. In consequence, they may present a significant aging effect and must be tolerant to neutron-induced soft errors. Related works have already shown that NBTI can lead to a small increase of the Soft Error Rate (SER) in SRAM cells fabricated in 45 nm CMOS technologies [3,4,6].

However, to the best of our knowledge, the literature has not reported SER studies regarding the influence of aging in SRAM-based FPGAs, where millions of SRAM cells are used as configuration memories to customize the configurable matrix in the user's design. In this article, we investigate the SER in an SRAM-based FPGA fabricated in 45 nm CMOS technology under neutron-induced effects when accelerated aging has been performed. We compare the measured sensitive area (cross-section) of the device post aging exposed under neutron to the sensitive area reported by

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the fabricant. Results show that the sensitive area can increase more than twice due to aging effects.

In addition, some FPGAs working in harsh environment may operate in systems with serious limitations of power due to its remote access. It is well known that SRAM-based FPGAs present a relative high static and idle power due to its millions of SRAM cells presented in the configurable memory bits. In order to reduce this power consumption, one common technique is to reduce the voltage supply of the entire FPGA core [7]. However, when doing that, the FPGA may be more susceptible to soft errors as well.

We analyse the combination of three different effects: soft error, aging and voltage scaling in SRAM cells at electrical simulation level to understand these three combined effects. The goal is to predict (based on a simulation method) the impact of these three effects on SRAM memory cells and further the impact in SRAM-based FPGA. We performed practical neutron-induced soft error rate experiments in SRAM-based FPGA under aging-induced variations and voltage scaling, and compare the results with the ones from the electrical simulation method. Results at electrical level could predict an increase of the soft error susceptibility by at least twice, when aging is also considered. The same proportion was measured under radiation.

2. Soft errors, aging and voltage scaling in SRAM-based FPGAs

SRAM-based FPGAs are complex integrated circuits composed of an array of configurable logic blocks (CLB) surrounded by a complex routing architecture, embedded memories (Block RAM), digital signal processing components (DSP), and a set of control and management logic. The CLBs are divided into slices. Each one is composed of a Look-up Table (LUT), which implements the combinational logic, and flip-flops (DFF) for the sequential elements. The routing architecture is composed of millions of pre-defined wires that can be configured by multiplexers and switches to build the desirable routing. The configuration of all CLBs, routing, DSP blocks and IO blocks is done by a set of configuration memory bits called bitstream. This one is loaded into SRAM memory cells, which are reprogrammable and volatile. According to the size of the FPGA device, the bitstream may contain millions of bits.

The selected device is the XC6SLX45-3CSG324 Spartan-6 Xilinx FPGA on a Digilent Atlys prototyping board [8]. This device is manufactured with a 45 nm technology and has a nominal core voltage of 1.2 V. The slices of this device can be divided into 3 different types. SLICEXs are the basic slices composed of LUTs and flip-flops. SLICELs include in addition an arithmetic carry structure and wide multiplexers. SLICEMs allow using the LUTs as distributed RAM and shift registers. All these resources are configured by a bitstream composed of 11,939,296 bits that are loaded into the SRAM configuration memory.

2.1. Radiation-induced soft error

At ground level, integrated circuits are susceptible to soft errors due to neutron effect [5]. As FPGAs have a large amount of SRAM memory cells, they are very susceptible to bit-flips in their configuration memory. According to the FPGA process technology the bitstream cells can be more or less susceptible to bit-flips. When a soft error occurs in the configuration memory, it can provoke a bit-flip. This one can change the configuration of a routing connection, the configuration of a LUT or a flip-flop in the CLB. This can be dramatic, since the bit-flip may change the functionality of it. Soft error in the configuration memory bits of an SRAM-based FPGA has a persistent effect and it can only be corrected when a new bitstream is loaded to the FPGA.

Two Soft Error Rates (SERs) can be analysed when SRAM-based FPGAs are exposed to neutron-induced soft errors. One is the static error rate, which is the number of bit-flips that occur per time in the bitstream. The other is the dynamic error rate, which is the number of errors in the design output synthesized into the FPGA. For the static error rate, the bitstream is continuously read and compared to the golden bitstream. Previous work performing static testing in this device at a neutron radiation facility [9] using an average neutron flux of 3.43×10^4 n/(cm^2 s) has shown a bit-flip upset rate of 0.27 upsets per minute.

2.2. Aging effects aging effect

Aging is a natural process that any integrated circuit suffers during its lifetime. The effects of aging can be seen as the degradation of a circuit in terms of its performance and also an increase in the leakage current. In order to analyse the effect of aging in FPGAs, it is possible to perform aging acceleration. This one is achieved by exposing the FPGA to an elevated temperature and core voltage [10]. For this purpose, the core was supplied with an external power supply at 1.8 V (above its nominal value of 1.2 V). The FPGA was heated to 80 °C using a thermal chamber, while a stress-design was in operation (to maintain a switching activity at given locations). The FPGA was configured with as array of Ring Oscillators (RO) as depicted in Fig. 1. Four gates were used for the structure of the RO, manually placed and routed in SLICEX and Switch Matrix. The manual mapping ensures an identical physical implementation of all ROs. In the following, the aging period refers to 10 days, including 7 days of effective aging and 3 days of recovery, required to clear the effects of reversible aging.

To measure the impact of aging on FPGA, the FPGA was characterized before and after aging using an ElectroMagnetic (EM) method, first proposed in [11]. In this method, the RO (Fig. 1) is successively placed in each of the 3411 CLBs of the Spartan-6 FPGA. Approximately half of the CLBs are based on one SLICEX and one SLICEL, and the other half on one SLICEX and one SLICEM (we will refer to CLBXL and CLBXM in the following). Each RO oscillates at a specific frequency, which is directly related to process, voltage and temperature (P, V, T).

Voltage is controlled using an external high precision DC power supply. The temperature is fixed using a thermal chamber. As demonstrated in [12], the measurement error is lower than 100 kHz with this equipment. Therefore, the variations between two different
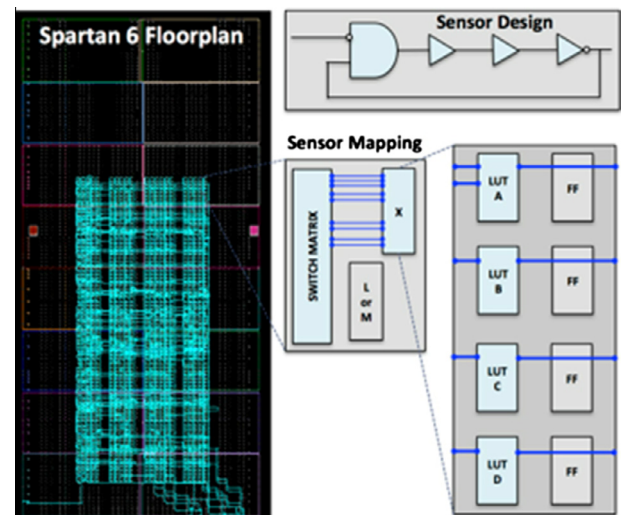

Fig. 1. Group of ring oscillators into the FPGA.

positions of the sensor are mainly due to process variations. During measurement, a near-field EM probe, placed over the chip, captures the EM emissions generated by the RO inside the chip. The signal from the sensor is amplified by a low noise amplifier and digitalized using an oscilloscope. An FFT is realized to obtain the frequency of each RO and then the chip cartography is build. The whole measurement system is illustrated in Fig. 2.

Characterization results obtained before the aging process are summarized in Table 1. As there are two kinds of CLBs (CLBXL and CLBXM), the mean frequencies are not the same for all the ROs. After aging, the FPGA is characterized again (Table 2). It can be noticed that the entire FPGA is affected by aging, even though from experimental results, it is clear that locations configured by ROs are more impacted. Compared to the measurements done before stress, we can observe clearly that the aging process has decreased the mean frequency of the ROs, as expected. Fig. 3 depicts the histograms of the ROs frequencies before and after aging. Both bimodal distributions have the same aspect and are only translated.

2.3. Voltage scaling

Scaling down the voltage in Spartan-6 FPGA reduces the mean frequencies of the RO (as all the transistors operating in a lower voltage supply also increase transistor-switching delays, as the aging effect). Voltage scaling in the SRAM cells also reduces the noise margins, which means that under neutron-induced soft errors, cells are more susceptible to flip, since the transistors that are at on state and can recover the upset node are slower and have more difficulties to restore the signal [13]. A previous experiment under neutron-induced soft errors has shown that the upset bit-flip rate can increase up to 50% for a 20% reduction in the supply voltage [9].

In this work, we analyse the bit-flip error rate under the effect of aging and voltage scaling combined by means of modelling the effects in SRAM cell at electrical simulation and by exposing the devices under neutron irradiation. These results are innovative because they associate three real effects that occur in FPGAs operating at ground-level applications and must be considered to evaluate the actual SER.

3. Analysing soft errors, aging and voltage scaling in SRAM cells by an electrical simulation method

An important measurement for soft-error sensitivity of a circuit is the critical charge (Q_{crit}), which is the minimum amount of

Fig. 2. EM measurement setup.

Table 1
Characterization results before aging process of ring oscillators USING CLBXL and CLBXM.

	F_{mean} (MHz)	Max var. (MHz)	3σ (MHz)
CLBXL	427.1	20.0	9.2
CLBXM	414.2	26. 8	10.8

Table 2
Characterization results after aging process of ring oscillators using CLBXL and CLBXM.

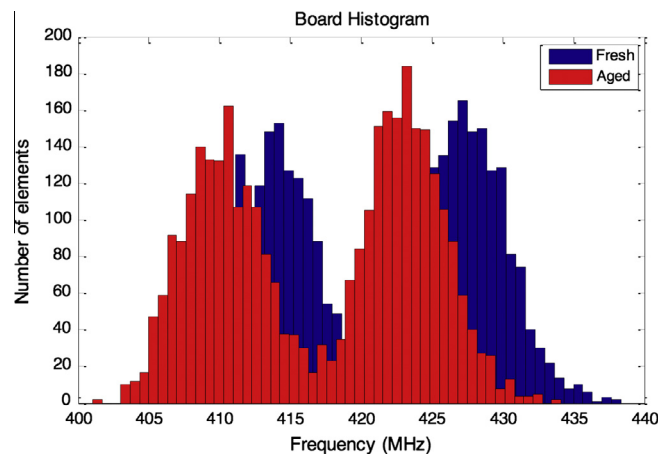|	F_{mean} (MHz)	Max var. (MHz)	3σ (MHz)
CLBXL	423.1	20.3	8.8
CLBXM	410.0	19.0	8.4

Fig. 3. Frequency degradation due to aging.

charge to inject in a circuit node to produce a soft error [14]. The critical charge can be determined from circuit simulation of the SRAM cell. In this work, Q_{crit} of a storage cell is computed by injecting a double-exponential current pulse at the storage node. Current collection is simulated at the reverse-biased drain junction of the turned-off NMOS transistor of the 6T-SRAM cells. Its amplitude is increased after each simulation, in order to find the threshold value between cell recovery and an upset. The critical charge is computed as the amount of charge injected by the current pulse.

It is important to observe that the critical charge is dependent on circuit parameters, such as bias voltage and transistor sizing, as well as device parameters, such as carrier mobility and threshold voltage. Consequently, Q_{crit} is sensitive to process variability and transistor aging. In this regard, Q_{crit} of modern SRAM memories are vulnerable to Bias Temperature Instability (BTI) effects due to the fact that BTI increases transistor threshold voltage, reducing current drive and, consequently, the critical charge. For digital circuits (such as SRAM cells) integrated in sub-100 nm process technologies the dominating aging mechanism is NBTI. This is due to the short times of hot carrier stress during active switching events, in comparison to the longer static time with BTI stress conditions [15]. Also, stress at high temperature tends to exacerbate the relevance of NBTI even more.

In order to account for the critical charge variability and aging effects due to NBTI (negative bias temperature instability), Monte Carlo simulations using a SPICE tool were performed to compute the critical charge distribution of 1000 6T-SRAM cells under different bias conditions. The SRAM cells were simulated using 45 nm Predictive Technology Model (PTM) transistor model [16].
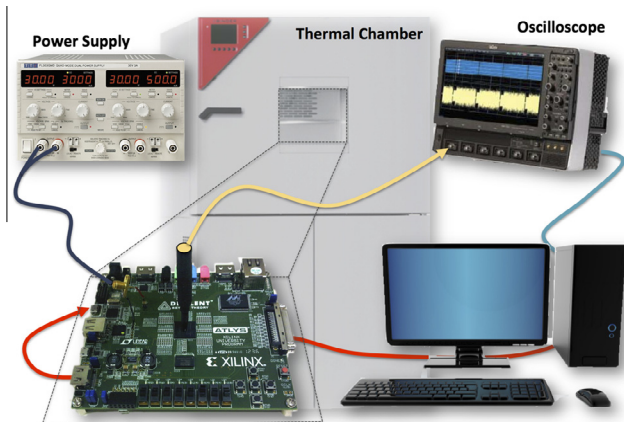
Transistor aging and process variations were modelled as threshold voltage shifts, whose mean and standard deviation were estimated by comparing simulation results to measurements of a number of implemented ROs during the EM analysis. Threshold voltage shifts are presented in Table 3.

The critical charge was computed only for strikes at logic 1 node. This decision is related to the fact that this node has a smaller critical charge compared to the logic 0 node, as shown by [17]. This is a consequence of the fact that the pull-up PMOS transistor usually has a weaker current drive compared to the pull-down NMOS transistor; therefore, a larger current pulse is required to flip a storage node from 0 to 1 than from 1 to 0. Also, BTI effects are more pronounced in PMOS transistors (NBTI) than in NMOS transistors (PBTI) for the 45 nm technology SRAM cell; hence, the logic 1 node is also more severely affected by BTI in this technology than the logic 0 node.

Aiming to provide an insight on how the degradation of the critical charge affects the probability of a soft error on a SRAM cell, a simplified situation may be analysed. Considering that the critical charge of a storage node is a random variable normally distributed and that the collected charge is also a normally distributed random variable, independent of the bias voltage, it is possible to determine the probability of a single event as:

$$CDF = 0.5\left[1 + erf\left(\frac{\mu_1 - \mu_2}{\sqrt{\sigma_1^2 + \sigma_2^2}}\right)\right] \qquad (1)$$

where μ_1 and μ_2 are the mean collected charges and the mean critical charges, respectively; σ_1 and σ_2 are the standard deviations of the collected charge and of the critical charge, respectively.

For each 6T-SRAM cell, the critical charge was calculated by sweeping the amplitude of a current source injected at a storage node of the cell, and integrating the threshold current that caused a bit-flip. The current source used was modelled as a double-exponential. The mean and standard deviation of the critical charge calculated are presented in Table 4.

It is possible to observe, based in Table 4, that the mean critical charge of the SRAM cells was reduced by roughly 8.2% due to stress. At first, this result may indicate that the tolerance to bit-flip of the 6T-SRAM is mildly affected by transistor aging. That is not always the case, however, as the number of bit-flips does not increase linearly with the reduction of the critical charge. It is important to consider that the probability of a bit-flip is also related to the charge deposited by an incoming particle. This charge is not a constant value, but rather a statistical distribution. In this work, for simplicity, this distribution is assumed to be normal. Hence, the probability of a bit-flip is related to the probability of the deposited charge of an incoming particle to be larger than the critical charge of the node it strikes.

Fig. 4 shows that Q_{crit} is strongly related to the bias voltage, in a trend, which is in accordance to that observed by [14]. Also, it is clear that the threshold voltage increase in the pull-up PMOS transistor due to BTI effects, degrades Q_{crit} of the cell, reducing it by

Table 3
Estimated mean and standard deviation of the threshold voltage shift before and after stress.

	NMOS		PMOS	
	Mean (mV)	Standard deviation (mV)	Mean (mV)	Standard deviation (mV)
Before stress	0	15	0	15
After stress	0	15	−50	15

Table 4
Calculated mean and standard deviation of the critical charge of 1000 6T-SRAM cells.

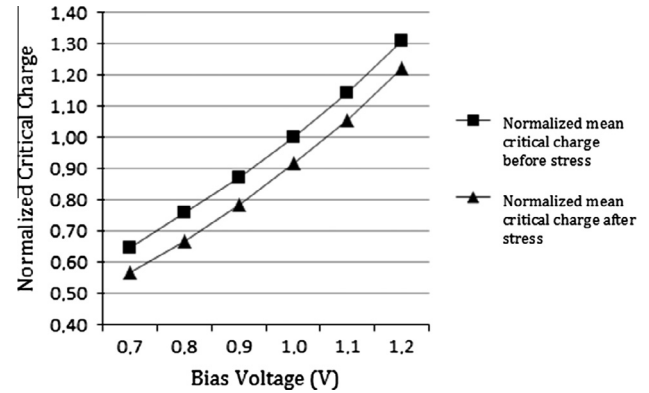|	Mean (aC)	Standard deviation (aC)
Before stress	287.2	7.4
After stress	263.7	8.1

Fig. 4. Effect of the critical charge in a SRAM cell before and after stress (aging effect).

roughly 8% for the applied threshold voltage shift. On the other hand, there is no indication that threshold voltage shifts due to transistor aging affects the relation $\partial Q_{crit}/\partial V_{DD}$. This relation, however, is affected by the width of the current pulse employed in simulation, as presented by [14]. The width of the current pulse can be estimated through device level simulations, based on device characteristics and the Liner Energy Transfer (LET) of the incoming particle. For smaller current pulse widths, the impact of bias voltage reduction on Q_{crit} is decreased, which may cause the impact of aging to dominate the critical charge degradation.

4. Neutron-induced soft error test experiment with aging and voltage scaling effects

Two FPGAs were tested: one FPGA without stress (here after "FPGA before stress") and one FPGA stressed (here after "FPGA after stress") under neutron radiation tests, performed at the ISIS facilities located at the Rutherford Appleton Laboratory (RAL) in the Didcot, UK. Irradiation was performed at room temperature with normal neutron incidence. The FPGA boards and the power supply are placed in the radiation chamber, while the computer used to monitor the test remotely is located in the control room. One USB connection is used between the FPGA board and the computer for the FPGA configuration memory readback via JTAG. The two FPGAs were irradiated with an average neutron flux of $3.43 \times 10^4 \pm 10\%$ n/(cm^2 s) and $4.10 \times 10^4 \pm 10\%$ n/(cm^2 s) respectively. The neutron fluence is calculated as the product of the average neutron flux and the time the FPGAs are exposed to the neutron flux.

The experiment consists of configuring the FPGA with a *golden* bitstream containing the test-design and then constantly read back the FPGA configuration memory with the Xilinx iMPACT tool through the JTAG interface. In the experiment control computer, the *golden* bitstream is compared against the *readback* bitstream. If differences are found, the FPGA is reconfigured with the *golden* bitstream and the differences are stored in the computer. This procedure is repeated for each core supply voltage and for both FPGAs. For both FPGAs, the errors are defined as any bit-flip in the configuration memory detected by the *readback* procedure.
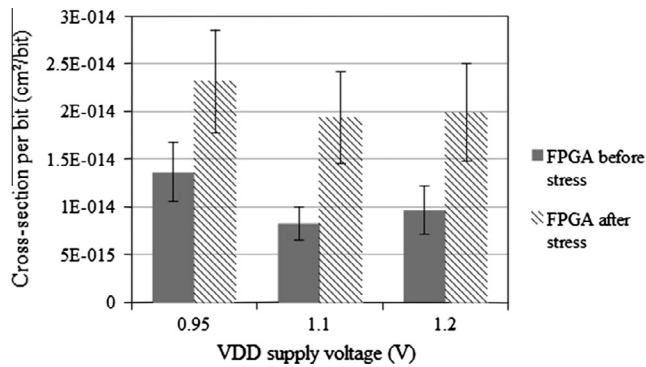
Fig. 5. Neutron cross-section of the configuration memory bits for Spartan-6 FPGAs before and after stress (aging effect) for different power supply modes.

With the aim of characterizing the soft error rate susceptibility of both FPGAs, the bit-flip cross-section per bit is calculated as defined:

$$\sigma_{SEU-bit} = \frac{N_{SEU}}{\Phi_{neutron} \times N_{bits}} \qquad (2)$$

where N_{SEU} is the number of bit-flips (SEU), $\Phi_{neutron}$ is the neutron fluence and N_{bits} is the number of bits of the device, as presented in [18].

In order to evaluate the soft errors under the effects of voltage scaling, three voltages were selected including the nominal voltage value: 1.2 V (nominal), 1.1 V and 0.95 V. The experimental data for FPGA before stress were obtained from [9].

Fig. 5 presents the cross-section per bit of configuration memory bits for both FPGAs and for the three different supply voltages. The error bars are calculated using Poisson statistics. As the power supply voltage is reduced, the nominal neutron cross-section increments for both FPGAs. Moreover, we also clearly observe that the aging process impacted more significantly the cross-section than the voltage scaling. These results are consistent with the predicted results in the latter section.

5. Conclusions

Based on Monte-Carlo electrical simulations and neutron experiment results, we observe the influence of aging and voltage scaling to soft error rate in SRAM-based FPGAs. Results have shown that the error rate can increase more than twice when considering aging and voltage scaling, so it is important to add this type of measurement and discussions when considering FPGAs for high-reliable applications. Based on the proposed methodology based on electrical simulation, it is possible to predict the increase in error rate due to aging and voltage scaling and this can guide designers to minimize those effects.

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