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A Delay Probability Metric for Input Pattern Ranking Under Process Variation and Supply Noise

Anu Asokan, Aida Todri-Sanial, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel
LIRMM-University of Montpellier II/CNRS, Montpellier, France
Email: lastname@lirmm.fr

Abstract—Ongoing technology scaling has increased delay defects in integrated circuits. Some of the delay defects are due to crosstalk, supply noise, process variations, etc. They degrade the performance and field reliability of circuits. However, testing the circuits with path delay patterns under worst-case conditions helps to detect such defects. Estimation of patterns with worst-case path delay becomes difficult using the conventional techniques due to their unpredictable behavior. In this paper, we first describe the problem and then propose our approach in identifying a worst-case path delay pattern under the impact of process variations and supply noise. A delay probability metric is presented in this work, for an efficient identification of worst-case path delay pattern, which is the basis of our ranking method. The simulation results of ITC’99 benchmark circuits show the feasibility of our delay probability metric.

Index Terms—delay defects, delay probability metric, process variations (PV), supply noise (SN)

I. INTRODUCTION

Ongoing technology scaling has increased delay defects in integrated circuits. Their early detection, lowers defect escape rate and ensures better circuit performance and field reliability. Delay defects are majorly introduced by the variations in the manufacturing process, as well as the noise disturbances in the power supply and ground networks. Timing-aware automatic test pattern generation (ATPG) tools are commercially utilized to detect delay-related defects. But they are incapable of accurately generating the worst-case path delay pattern as they do not consider physical defects affecting the gates, interconnects, power supply and ground networks, etc. Gate or path delay can be modeled using statistical static timing analysis (SSTA) [1]. SSTA and process corner based techniques work with delay probability distributions. However, they are too complex to work with realistic path delay distributions and identify an accurate delay pattern. This has motivated us to propose a simple and novel delay probability metric to identify a worst-case path delay pattern for capturing delay defects.

Unpredictable process parameter fluctuations and changing operating voltage conditions cause random variations in the circuit parameters, thereby affecting the expected nominal path delay values. Fluctuations in the manufacturing process affect the gate parameters such as threshold voltage ($V_{th}$), oxide thickness ($t_{ox}$), transistor length ($L_g$) and width ($W_g$), as well as the width of interconnects (resistance, inductance and capacitance). Operating voltage of a circuit varies depending on the noise disturbances in their power supply (i.e., power supply noise) or ground networks (i.e., ground bounce), varying the drive strength in the gates. Also, path delay of a circuit varies randomly depending on the input patterns and their arrival times. The combined impact of all these effects makes path delay estimation difficult. Therefore, a simple yet effective method for identifying the worst-case or the most effective path delay patterns that can capture a delay defect during testing is essential. In this work, we propose a delay probability metric to identify a worst-case path delay pattern in the presence of PV and SN.

There are a number of contributions that investigate the impact of PV and SN. Based on the source of physical defects, they can be classified as delay defect: (1) due to a single source (i.e., PV, SN or crosstalk only), (2) from multiple sources, and (3) irrespective of the source. The first classification focuses only on process variations [2]–[5]. Francisco et al. [2] proposed a statistical timing analysis framework based on delay correlation information between two paths. Critical path delay measurement using a ring oscillator is presented in [3]. Authors in [4] have proposed an algorithm to detect a resistive interconnect defect for a path with minimum delay variance. An optimization framework is suggested by Yu [5] based on SSTA for worst-case circuit analysis. In the second classification, different approaches for pattern generation from multiple sources were proposed [6]–[8]. Todri et al. [6] has analyzed power supply noise and ground bounce for capturing worst-case path delay patterns based on simulated annealing. Xu [7] described a statistical model for skitter with PV and power supply noise effects. Peng [8] explains their work of pattern evaluation and selection considering crosstalk and PV. In the third classification, worst-case delay of a circuit path is analyzed, with no detailed reference to the source of defects. A theoretical framework for statistical timing analysis is proposed by Orshansky and Keutzer [9] for detecting the worst-case path delay in a circuit.

In contrast to all these works, our goal is to re-examine the problem of path delay pattern generation by introducing a delay probability metric for ranking patterns under the impact of PV and SN. Using the probabilistic metrics, we can estimate and identify an efficient worst-case path delay pattern or set of patterns that can capture the worst path delay. Our method is practical and easily adaptable to be implemented on any existing pattern generation flow. Complementary to the previous works, we have additionally incorporated the impact...
of ground bounce in supply noise. Our major contributions in
this paper are summarized as follows:
- A probability metric is presented to identify worst-case
  path delay pattern while considering the combined impact
  of PV and SN. This metric aims at detecting the most-effective
  pattern for path delay testing from the subset of all input
  patterns.
- Ranking method is described based on the mean delay
  difference and the area of the delay probability distribution of
  all input patterns.
- Case study and simulation results are shown to validate
  our method.

The rest of this paper is organized as follows. In Section
II, we formulate the problem of path delay distribution for
detecting a worst-case pattern in the presence of PV and SN.
Section III demonstrates the individual and combined impact
of PV and SN. Section IV presents the simulation results on
ITC’99 benchmark circuits. Finally, in Section V, we conclude
our paper.

II. PROBLEM FORMULATION

In this section, we describe the problem that we address
and propose our mathematical approach in identifying test
patterns that can capture the worst-case path delay under the
impact of PV and SN. Initially, we estimate the dependent
circuit parameters that affect the delay of a circuit path. Then,
describe the proposed probabilistic metrics for ranking patterns
based on their effectiveness. Finally, we describe our method
of ranking patterns based on a delay probability metric.

A. Path Delay Estimation

In this subsection, we describe the proposed analytical
method for computing the ranking order of test patterns. The
problem of path delay test is a well-understood and widely
investigated problem by the scientific community, in effectively
identifying the test patterns for performance evaluation that
would eventually lead to high-quality test patterns that can
lower defect escape rate. With technology scaling, increased
circuit densities and faster switching circuits, identifying the
high quality patterns is getting even more challenging. Even
more so when the impact of physical design issues and PV
are taken into account. Due to the nature of the problem with
many parameters that can cause a wide delay distribution, we
exploit a probability based-approach to rank patterns based on
their effectiveness for capturing the worst case delay under the
impact of PV and SN.

Each test pattern triggers a given switching activity on the
circuit and the critical path under observation. As already
shown in [6], critical paths can undergo drastic delay variation
that can lead to slow-down and/or speed-up effects. We expect
that such delay variations will be even more pronounced when
PV of transistors and interconnects are included.

Problem definition: We aim to identify the set of patterns
that are the most effective for capturing the worst case path
delay under the impact of PV and SN; based on the delay
probability density function of each pattern.

Path delay on a circuit is computed by considering the
delays of both interconnects and gates. Supply noise which
exhibits itself as power and ground voltage fluctuations can
impact the operating regions of transistors, hence the delay
behavior of the gates. Additionally, different gates on a path
can suffer from different amounts of supply noise. Random
process variations induce deviation on the transistor’s and
interconnect’s dimensions and carrier’s mobility. In this work,
we consider process variation on threshold voltage, $V_{th}$, oxide
thickness, $t_{ox}$, transistor gate length, $L_g$ and width, $W_g$
and interconnect length and width that impact interconnect par-
sitics, $R$, $L$, $C$. From supply noise perspective, we consider
noise on power, $V_{dd}$ and ground, $G_{nd}$.

The delay of a pMOS transistor due to a rising input can be
expressed as [10]:

$$\delta_r = \frac{2C_L}{\beta_p[(V_{dd} - G_{nd}) - |V_{thp}|]} \left[|V_{thp} - 0.1(V_{dd} - G_{nd})| + \frac{1}{2} \log \left|\frac{(20|V_{thp}|)}{(V_{dd} - G_{nd})}\right|\right]$$  \hspace{1cm} (1)

where $C_L$ is the load capacitance including the next stage
load and interconnect capacitance and $V_{thp}$ is the threshold
voltage of pMOS transistor. Similarly, the transistor delay for
a falling input can be expressed as [10]:

$$\delta_f = \frac{2C_L}{\beta_n[(V_{dd} - G_{nd}) - V_{thn}]} \left[|V_{thn} - 0.1(V_{dd} - G_{nd})| + \frac{1}{2} \log \left|\frac{(20|V_{thn}|)}{(V_{dd} - G_{nd})}\right|\right]$$  \hspace{1cm} (2)

where $V_{thn}$ is the threshold voltage of nMOS transistor and
$\beta$ is the transistor gain factor (in pMOS and nMOS), can be
expressed as:

$$\beta = \frac{\mu \epsilon}{t_{ox}} \left(\frac{W_g}{L_g}\right)$$  \hspace{1cm} (3)

where $\mu$ is the effective surface mobility of the carriers in
the channel, and $\epsilon$ is the permittivity of the gate insulator.
Based on the transistor delay, the gate delay can be computed,
such as for an inverter the average gate delay can be computed
as:

$$\delta_g = (\delta_f + \delta_r)/2$$  \hspace{1cm} (4)

Interconnects are usually modeled as $\pi$-networks with RLC
parasitics, their delay, $\delta_{int}$ can be computed by applying
Elmore delay formulation as a function of $\zeta_i$ at node $i$, as
in [11]:

$$\delta_{int} = 1.047e^{-\zeta_i} + 1.39\zeta_i$$  \hspace{1cm} (5)

where $\zeta_i$ is expressed as:

$$\zeta_i = \frac{1}{2} \left(\frac{\sum_k C_k R_{ik}}{\sqrt{\sum_k C_k L_{ik}}}\right)$$  \hspace{1cm} (6)
where $R_k$ is the interconnect resistance, $C_k$ is the interconnect capacitance, $L_k$ is the interconnect inductance and $k$ represents the number of elements on the $n$-network interconnect model. Hence, the delay on a path can be computed as the sum of gate delays and interconnects delays (i.e. for $n$ gates and $n-1$ interconnects on a given path) that are triggered by a given input pattern as:

$$
\delta_{path} = \sum_{i=1}^{n} \delta_{g_i} + \sum_{i=1}^{n-1} \delta_{int_i}
$$

(7)

B. Delay Probability Distribution

For a given path, the delay would be a function of many variables due to PV and SN. Path delay variations due to these variables can be expressed as a function of parameters as:

$$
\delta_{path} = f(V_{dd}, G_{nd}, V_{th}, l, G_{ox}, L_g, W_g, R, L, C, C_L) = f(SN, PV)
$$

(8)

**Definition:** In general terms, the path delay variation, $\delta_{path}$ for a given input pattern, $PI$ can be represented as a normal distribution function. As path delay (due to $\delta_g$, or $\delta_{int}$) can be real-valued random values whose distribution are unknown, the highest probability of worst-case path delay can be observed better using a normal delay distribution function. The path delay due to test patterns for all parameters (PV and SN) can be expressed as normal distribution $N(\mu_{PI}, \sigma_{PI})$.

The mean and standard deviation of a path delay for a given input pattern, $PI$ and all parameters can be expressed as:

$$
\mu_{PI} = \frac{1}{N} \sum_{i=1}^{N} \delta_{path_i}
$$

(9)

$$
\sigma_{PI} = \sqrt{\frac{1}{N} \sum_{i=1}^{N} (\delta_{path_i} - \mu_{PI})^2}
$$

(10)

where $N$ represents the total number of path delay measurements for a given path under PV and SN parameters.

C. Probabilistic Pattern Ranking Method

Here, we describe the concept of deriving pattern ranking method utilizing the path delay distribution function. Fig. 1 illustrates the probability density distribution of an input pattern under process variation and supply noise. Assuming that for a known design, there is a predefined delay threshold with $\mu_{nom}$ that represents the tolerable delay of the circuit.

**Definition:** We define the *probability of identification, $P_{identification}$ that can analytically estimate the likeliness of a pattern $j$ under PV and SN conditions to cause a path delay at each node $i$, $\delta_{path_i}$ larger than the allowed delay threshold, $\mu_{nom}$, and can be expressed as:

$$
P_{identification}[\mu_{PI} \geq \mu_{nom}] = \int_{\mu_{nom}}^{\mu_{max_j}} \delta_{path_i}(t) dt
$$

(11)

where $\mu_{max_j}$ of a pattern $j$ is defined as:

$$
\mu_{max_j} = \mu_{PI} + \frac{3\sigma_{PI}}{2}
$$

(12)

Hence, for each pattern, the $P_{identification}$ allows us to compute the exposed area of the probability density function beyond a delay threshold also as shown in Fig.1. Utilizing this metric, we further define the pattern ranking method that considers both the mean, $\mu_{PI}$ and probability of identification, $P_{identification}$, of each pattern for classifying the patterns for inducing the worst path delay under PV and SN conditions. The ranking metric, $Rank_{PI}$, is defined as:

$$
Rank_{PI} = \alpha_1 \mu_{PI} + \alpha_2 P_{identification}
$$

(13)

where $\alpha_1$ and $\alpha_2$ are weight coefficients between 0 to 1 that can be given for taking into account both the changes in mean, $\mu_{PI}$ and the identification metric $P_{identification}$, where $\mu_{PI}$ is expressed as:

$$
\mu_{PI} = \mu_{nom} - \mu_{PI}
$$

(14)

Fig. 1. Delay Probability distribution of an input pattern

The values for $\alpha_1$ and $\alpha_2$ can be chosen based on their priority (i.e., $\mu_{PI}$ or $P_{identification}$) during path delay testing. We further utilize these probability metrics for ranking the patterns on a sample circuit to illustrate the effectiveness of the proposed ranking method.

III. CASE STUDY

In this section, we illustrate our proposed delay probability metric by applying it on a sample circuit as shown in Fig. 2. For simplicity, we have considered a small circuit as a case study, but our metric can be applied to any large circuit. The sample circuit comprises interconnect models and gates connected to a global power supply voltage and ground networks. To study the impacts of PV and SN on path delay, we incorporate parameter variations in gates (at transistor level) and interconnects (on their widths) and then control the power supply and ground voltage locally (at gate level). The transistor and interconnect models are derived from
90nm Predictive Technology Model (PTM) [12]. HSPICE simulations are performed on the circuit for three different cases to analyze: (1) the impact of PV only, (2) the impact of SN only, and (3) the combined impact of PV and SN. For each case the following three steps are performed: (i) estimate path delay ($\delta_{\text{path}_j}$), (ii) compute mean ($\mu_{P_{I_j}}$) and standard deviation ($\sigma_{P_{I_j}}$) from the delay probability distribution of each input pattern ($P_{I_j}$), and (iii) identify the worst-case path delay pattern ($P_{\text{identification}_j}$) based on our ranking method. We utilize MATLAB to execute the mathematical computations of equations described in Section II.

In the first case, we study only the impact of PV, by varying the interconnect and transistor parameters while applying a nominal global supply voltage at their gates. Fig. 4 depicts the probability density distribution function of all the input patterns ($P_{I_j}$) at the gate level. Path delay of the circuit can be measured between any two points, for our case study we observe between {Op1} and {Ip1}.

We perform HSPICE simulations and measure the path delay for all the process corners in the circuit. Input pattern numbers, corresponding input vectors and their input transitions (i.e., rising and falling input signals) are shown in column I, column II and column III respectively of Table. I. Our delay probability metric can give all the possible path delays, but we are focused only on finding a worst-case path delay. Their corresponding metrics will indicate the input pattern to be the most effective for capturing path delay defects under PV and SN conditions.

A. Case I: Impact of Process Variations

In the first case, we study only the impact of PV by varying the interconnect and transistor parameters while applying a nominal global supply voltage at their gates. Fig. 4 depicts the probability density distribution function of all the input
**TABLE I**

**RANKING METHOD FOR IDENTIFYING WORST-CASE PATH DELAY PATTERNS**

<table>
<thead>
<tr>
<th>Pattern (PI)</th>
<th>Input vectors (V1, V2) at {lp1 lp2 lp3}</th>
<th>Input transition</th>
<th>Under PV</th>
<th>Under SN</th>
<th>Under PV and SN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>μPId</td>
<td>Pmean</td>
<td>μPId</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rank</td>
<td>Rank</td>
<td>Rank</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PIdn</td>
<td>Pmean</td>
<td>PIdn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rank</td>
<td>Rank</td>
<td>Rank</td>
</tr>
<tr>
<td>P1</td>
<td>{10 10 10}</td>
<td>(Fall Fall)</td>
<td>0.27ps</td>
<td>0.51</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7.73ps</td>
<td>0.67</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.12ps</td>
<td>0.68</td>
<td>4</td>
</tr>
<tr>
<td>P2</td>
<td>{10 10 01}</td>
<td>(Fall Rise)</td>
<td>4.67ps</td>
<td>0.60</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7.97ps</td>
<td>0.58</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.56ps</td>
<td>0.63</td>
<td>7</td>
</tr>
<tr>
<td>P3</td>
<td>{10 01 10}</td>
<td>(Fall Rise)</td>
<td>0.07ps</td>
<td>0.50</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7.33ps</td>
<td>0.66</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.22ps</td>
<td>0.67</td>
<td>5</td>
</tr>
<tr>
<td>P4</td>
<td>{10 01 01}</td>
<td>(Fall Rise)</td>
<td>9.47ps</td>
<td>0.70</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>17.3ps</td>
<td>0.80</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11.8ps</td>
<td>0.89</td>
<td>2</td>
</tr>
<tr>
<td>P5</td>
<td>{01 10 10}</td>
<td>(Rise Fall)</td>
<td>0.13ps</td>
<td>0.49</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7.36ps</td>
<td>0.67</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.5ps</td>
<td>0.69</td>
<td>6</td>
</tr>
<tr>
<td>P6</td>
<td>{01 10 01}</td>
<td>(Rise Fall)</td>
<td>9.47ps</td>
<td>0.70</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>17.3ps</td>
<td>0.80</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11.7ps</td>
<td>0.89</td>
<td>3</td>
</tr>
<tr>
<td>P7</td>
<td>{01 01 10}</td>
<td>(Rise Rise)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>P8</td>
<td>{01 01 01}</td>
<td>(Rise Rise)</td>
<td>35.9ps</td>
<td>0.94</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>48.2ps</td>
<td>0.98</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25.9ps</td>
<td>0.99</td>
<td>1</td>
</tr>
</tbody>
</table>

*μPId = Difference between nominal delay (μnom) and delay mean of an input pattern μ(Pi)

The results of these case studies indicate that by applying the proposed ranking method, we can identify the pattern(s) that lead to the worst-case path delay when PV and SN conditions are present.

### IV. EXPERIMENTAL RESULTS

In this section, we present our experimental results based on five ITC’99 benchmark circuits [14]. We apply our probabilistic method on a single critical path, however it can be

Patterns under PV. For each input pattern, their respective μPId, Pidentification and rank are listed in column IV, V and VI of Table I. Using our probabilistic pattern ranking method, we obtain PIs as the worst-case path delay pattern under the impact of PV. This is also shown in Fig. 4 as the pattern with the largest area exposed beyond the nominal delay threshold line.

**B. Case II: Impact of Supply Noise**

In this section, we present our experimental results based on five ITC’99 benchmark circuits [14]. We apply our probabilistic method on a single critical path, however it can be
TABLE II
RESULTS OF ITC’99 BENCHMARK CIRCUITS

<table>
<thead>
<tr>
<th>Clk</th>
<th>X-bit input pattern</th>
<th>ATPG</th>
<th>Our method</th>
<th>% μ_{PID}</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Input pattern</td>
<td>μ_{PID}</td>
<td>P_{cid}</td>
<td>Rank</td>
</tr>
<tr>
<td>b01</td>
<td>11001X</td>
<td>110010</td>
<td>136ps</td>
<td>0.91</td>
</tr>
<tr>
<td>b02</td>
<td>0000X</td>
<td>00000</td>
<td>159.34ps</td>
<td>0.96</td>
</tr>
<tr>
<td>b05</td>
<td>00X0X</td>
<td>00100</td>
<td>171.9ps</td>
<td>0.84</td>
</tr>
<tr>
<td>b06</td>
<td>100UX</td>
<td>100110</td>
<td>123ps</td>
<td>0.93</td>
</tr>
<tr>
<td>b11</td>
<td>XXXXXXXX0000X</td>
<td>11000110001</td>
<td>172.76ps</td>
<td>0.82</td>
</tr>
</tbody>
</table>

applied to any paths. Table II shows the summary of our experimental results. We utilized an ATPG tool for generating X-bit input patterns mentioned in column II. Then, we filled only the relevant X-bits (indicated in italics and bold letters) based on efficient X-filling method [15].

We explain in detail the results of our delay probability metric for b05 benchmark circuit. For all the X-filled input patterns (i.e., 00000, 00001, 00100, and 00101), we computed the mean delay difference μ_{PID} (i.e., 176.9ps, 191.3ps, 171.9ps, 182.67ps) and P_{identification} (i.e., 0.86, 0.91, 0.84, 0.90), and then ranked (i.e., 3, 1, 4 and 2) each input pattern. We selected the input pattern with rank 1 (i.e., 00001 as shown in column VII), as by our method this pattern has the highest probability to give the worst-case path delay under the impact of PV and SN. Also, we selected the input pattern generated by the ATPG tool (i.e., 00100 as shown in column III) and indicate its rank in column VI. In column XI, the mean delay difference (i.e., 10.14%) between the two patterns (our method pattern and ATPG pattern) is obtained. Such discrepancies further indicate the need for investigate the worst-case path delay problem and reveal the effectiveness of our method in ranking.

The pattern generated by random X-filling using the ATPG tool differs from the pattern generated by our probabilistic method. This indicates that, while a test pattern sensitizes a path for path delay testing, it doesn’t necessarily capture its worst-case path delay. Whereas, proposed method, investigates the set of patterns and aims to rank them based on the likelihood to obtain the worst path delay when process variation and supply noise variations are taken into account. The proposed method is practical to be embedded on pattern generation flow i.e., post-ATPG X-filling, which is also the focus of our future work.

V. CONCLUSIONS

In this paper, we proposed a delay probability metric for identifying a worst-case path delay pattern under the impact of process variation and supply noise. The presented probabilistic pattern ranking method aims at capturing delay defects during path delay test. Our experimental results on ITC’99 benchmark circuits suggests to improve the existing pattern generation methods by incorporating the impacts of PV and SN. As future research, we aim to implement the probabilistic method in X-filling pattern generation flow.

REFERENCES