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TSV Aware Timing Analysis and Diagnosis in Paths with Multiple TSVs

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***Abstract*—3D-IC test becomes a challenge with the increasing number of TSVs and demands for effective 3D aware test techniques. In this work, we propose a timing aware model to capture delay variations on a path due to resistive open TSVs. The key idea is to analytically model delay and apply our correlation-based resistive open TSV detection method to attain path delay fault coverage. We propose two methods to investigate timing variation introduced by resistive open TSVs in a critical path delay with multiple TSVs. Method I computes the correlation of multiple TSVs in a path to overall path delay to determine if TSVs are the source of the introduced delay. Method II pinpoints which TSV is faulty by computing the delay fault coverage of each TSV in a path with multiple TSVs. Our results indicate the accuracy of our proposed method and promotes early identification of resistive open defects TSVs.**

***Keywords*—3D integration; Through-Silicon vias (TSV); resistive open TSV; timing aware model; multivariate statistics**

I. Introduction

Three-dimensional (3D) integrated circuits (IC) stacking technology promises to solve the interconnect bottleneck problem by vertically connecting tiers using Through Silicon Vias (TSVs). Despite all advancements in 3D-IC, the 3D integration imposes new test challenges such as test access, test cost, design for testability, and new manufacturing defects related to 3D processing steps such as wafer thinning, bonding and wafer alignment [1]. Therefore, dies and TSVs need to be tested both before (i.e. pre-bond test) and after bonding (i.e. post-bond test) to ensure that dies, TSVs and 3D integration are defect free.

Defects such as resistive open TSVs caused by not completely filled or partly broken TSV channel can be very difficult to be detected given that the TSV channel still conducts but weakly due to an increased resistivity. From the path delay perspective, these defects increase delay and may cause timing violation. In this work, we target path delay test for resistive open TSV.

3D test architecture include Design-for-test (DfTs) solutions for post-bond test providing modular test access to all components through the stacked tiers [2]. Also, the on-going development on 3D test standards suggest insertion of wrapped embedded cores [3] and dedicated scan flip-flops between TSVs [4]. These scan registers interface tier logic and TSV, enabling the controllability and observability of the interface. From a critical path point of view, this 3D test architecture introduces an additional number of stage-paths due to insertion of dedicated scan flip-flops between TSVs. Through these stage-paths is possible to obtain accurately the delay from tier interface between the next tier.

In this work, we exploit such 3D test architecture representation and focus our timing analysis on a critical path that contains multiple TSVs. We assume that ATPG is performed along the 3D DFT architecture and we apply our test method to a post-ATPG test set. Thus, there is no need to perform fast-than-at-speed test for our detection method. Given that stage-paths can be controllable and observable thanks to the 3D test architecture, we analytically model the stage-path delay between tiers in order to investigate the TSV induced delay. We aim to check the robustness of TSVs by analyzing stage-path delay with the overall path delay through our test framework. Our main contributions are summarized below:

- We propose a new timing analysis model for post-bond TSV test, where we compute the relationship between timing variations induced by resistive open TSVs and the overall path delay with multiple TSVs. By this computation, we can define if the introduced delay is caused by resistive open TSVs or due other factors that affect the 3D path delay (i.e. non-uniform switching, supply noise and crosstalk).
- The proposed timing analysis model considers a 3D test architecture [4], where it is based on custom 3D test wrapper enabling modular test approach. This modular 3D test approach enables access to stage-paths, where the stage-path delay is analytically formulated to identify the conditions of each TSV. Our proposed *stage-path model* is based on accurate timing analysis of the stage-path taking into account the TSV parasitics, TSV-to-TSV coupling, and multiple parameters introduced from both physical and electrical factors present on die level.
- We define our *path delay fault coverage* with our proposed *correlation-based resistive open TSV detection method*. Our method computes the correlation coefficient based on the formulated stage-path delay model.

This paper is organized as follows. Section II overviews related works in TSV testing and 3D test flow. In Section III, the stage-path delay model is analytically formulated. Section IV provides the correlation-based detection method of resistive open TSVs in critical paths containing multiple TSVs. Section V presents simulation results to demonstrate the applicability of our method. Finally, Section VI concludes this paper.

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II. Related Works and 3D Test Flow

The 3D-IC test is very challenging due to the complexity of 3D circuits and test cost, thus requiring a test methodology that is suitable for 3D-ICs. A number of works address 3D test for both pre-bond [5] and post-bond testing [6]–[8]. In pre-bond test phase, tiers have not been stacked yet and TSVs interconnects and intra-die circuitry are tested prior to be stacked. Pre-bond test requires test access to manage the small number of contacts during probing and the fragile structure of TSV microbumps and high dimension TSVs. As solution to test access, many existing works design the DfT architecture based on wrappers. In post-bond test the test access is enabled by additional DfT and TSVs given that the probing access is only possible by the external pins of the tier closest to the packaging. The additional DfT registers assure that the stack is working and that no defects has been introduced during the thinning, alignment and bonding tiers together [1]. %vspace-0.2em

Typical 3D DfT architectures provide controllability and observability of inter-dies and TSVs through wrappers located at die-level. These wrappers are normally based in IEEE Std 1500 or 1149.1 test standards [4], and it contains at least one register per each TSV. This 3D test flow introduces additional stage-paths and enables the observability and controllability through scan flip-flops as shown in Figure 1. Thus, it is possible to evaluate *each* stage-path delay between tiers thanks to the wrapper scan flip-flops.

Many works have presented techniques to test TSV delay in literature for both pre-bond and post-bond. In [5], [9]–[11] presented self test circuits which detects open TSVs. In [7], a DfT is proposed to detect open or short interconnects in a 3D-IC. They insert a JTAG interface to each die and test interconnects in the interposer and substrate. Also, with their interconnect redundancy scheme is possible to pinpoint which element is faulty and repairs it. However, their algorithm only tests full open interconnects or large resistive open TSV values. Although previous works have proven their methods to be effective for their objectives, we target timing variations caused by resistive open TSVs. We explore 3D test architecture based on IEEE 1149.1 [4] and apply our *correlation-based detection method* to further prune their results and detect resistive open TSVs at smaller resistance values. To the best of our knowledge, this is the first paper that proposes detection of resistive open TSV based on correlation-based resistive open TSV detection method. We aim to identify first if TSVs are the source of timing variations in a critical path with multiple TSVs and secondly we aim to identify which TSV(s) causes it. As will be shown in the next sections, we analytically formulate stage-paths delay model and show our correlation-based method to identify the condition of TSVs.

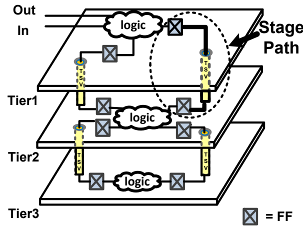

Fig. 1. Conceptual view of the additional stage-paths that are introduced between dedicated scan flip-flops (FF) enabling TSV interconnects be controllable and observable. The figure shows a critical path with four stage-paths.

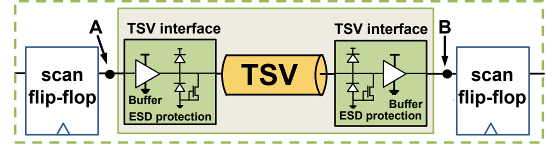

Fig. 2. Circuit schematic of the TSV interface and TSV interconnection connecting two tiers. Each stage-path is surrounded by scan flip-flops and delay is measured from point A to point B.

III. Stage-Path Delay Computation

In this section, we derive an analytical model for stage-path delay. We further exploit stage-path delay model to investigate the effect of resistive open TSVs on the critical path delay. We assume that path selection is performed with custom commercial tools and we focus on selected paths which contain TSVs. In Figure 2, a single stage-path delay is measured from point *A* to *B* and it is composed by the TSV interface. The TSV interface is composed by TSV driver and receiver buffer gate, Electro-Static Discharge (ESD) protection diodes, a weak pull-down device [12] and TSV interconnect. ESD protection and the weak pull down device work as protection to electrical discharges that can come from the tiers due to different technologies nodes and supply voltage. Given that the ESD protection and the weak pull-down have negligible timing impact, they are not considered in our stage-path delay formulation.

Definition: Stage-Path (SP) delay is the delay measured between wrapper scan flip-flops. The stage-path contains the TSV and the TSV interface in both ends of the TSV. The TSV interface is composed by buffers (TSV drivers and receivers), a weak pull down and an individual ESD protection.

Stage-path delay can experience either delay speed-up or slow-down due to the voltage levels at power V_{DD} and ground V_{SS} terminals [14], [15]. Stage-path delay also can vary with the input vector, buffer gates intrinsic parasitics and TSV parasitics. TSV-to-TSV coupling can also further exacerbate delay variations due to the capacitive coupling.

We present a stage-path delay closed formula to analyze timing variations while taking into account the TSVs parasitics, input vectors, and intra-die physical and electrical factors such as supply noise voltage, ground bounce, drain saturation current, and drain source current from gates and threshold voltage. We define stage-path delay as a function of input vector (V_{in}), TSV parasitics (i.e. $R_{TSV}, L_{TSV}, C_{TSV}$), TSV-to-TSV coupling (i.e. *Cc* and *Gsi*), driver and receiver buffer intrinsic parasitics ($R_{Buff}, L_{Buff}, C_{Buff}$), power ($V_{DD}$) and ground ($V_{SS}$) supply voltage. Moreover, as the stage-path delay is analytically modeled in function of technology node parameters, the closed formula can be applicable to present and future technologies. Thus, stage-path delay can be ex-

pressed as a function of physical and electrical factors such as:

$$stage_path\ delay \equiv \Delta SP = f(R_{TSV}, L_{TSV}, C_{TSV}, Cc, \\ Gsi, R_{Buff}, L_{Buff}, C_{Buff}, V_{DD}, V_{SS}, V_{in}) \quad (1)$$

where *Cc* represents the oxide capacitance, depletion capacitance and the silicon capacitance and *Gsi* the silicon conductance through the substrate [13]. We compute ΔSP for low-to-high (LH) and high-to-low (HL) transitions. The incremental charge on buffer delay considering power and ground supply noise can be expressed as in [14]:

$$\Delta SP_{LH} = k_1.(\Delta_{V_{DD}} + \Delta_{V_{SS}}) \\ -k_2.(\Delta_{V_{DD}} - \Delta_{V_{SS}}) + k_5$$

and

$$\Delta SP_{HL} = -k_1.(\Delta_{V_{DD}} + \Delta_{V_{SS}}) \\ -k_2.(\Delta_{V_{DD}} - \Delta_{V_{SS}}) + k_5 \quad (2)$$

where ΔSP_{HL} is the calculated stage-path delay for LH and ΔSP_{HL} for HL. The k_1 is positive constant for rising transition is $+k_1$ and for falling transition it is $-k_1$, while k_2 is a positive constant. The constants' values depend on the input transition, gate load, and parasitics. The constants k_1, k_2 and k_5 are obtained by [14]:

$$k_1 = \frac{t + \Delta t}{2V_{DD}.(1+\alpha)} + \frac{C_{load}}{2I_{DO}} \quad (3)$$

$$k_2 = \frac{t + \Delta t}{2V_{DD}.(1+\alpha)} - \frac{C_{load}}{2I_{DO}} \quad (4)$$

$$k_5 = \Delta t.\left(0.5 - \frac{1 - vt}{1+\alpha}\right) \quad (5)$$

where t is the transition time, vt is the threshold voltage, α is the ratio of drain to source current, I_{DO} is the drain saturation current (when $V_{GS} = V_{DS} = V_{DD}$) of the driver buffer and it is defined on the sizing of the driver. C_{load} represents the TSV capacitance and the receiver buffer intrinsic capacitance.

In the following section, we present our correlation analysis methods that compute the relationship between stage-path delay calculation and the total path delay. Based on

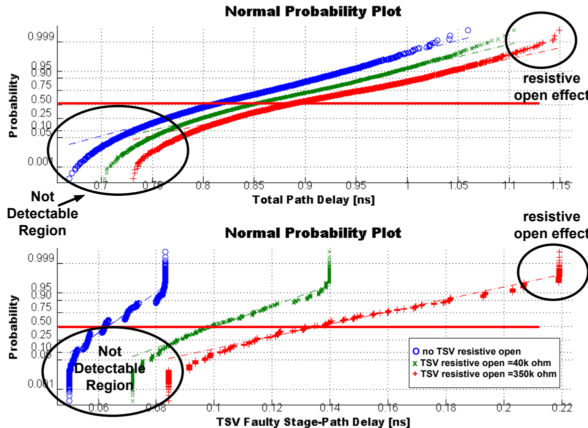

Fig. 3. Total path path delay and stage-path delay of resistive open TSV. It is possible to observe the region where faulty TSV is detectable and the TSV resistive open effect on the normal probability plot. We assume the not detectable region as the region with probability under 50%, shown bellow the line.

these mathematical models, we formulate our correlation-based detection method of resistive open TSVs in critical paths containing multiple TSVs.

IV. Critical Path with Multiple TSVs

In this section, we describe our proposed correlation-based detection method in paths with multiple TSVs. This method is based on statistical correlation method that statistically analyzes the relationship between two variables and to attain path delay fault coverage. We mathematically compute the relationship between delay variations induced by resistive open TSVs and the overall path delay with multiple TSVs. Our proposed correlation-based detection method can confirm or dismiss if the introduced delay is caused by resistive open TSVs.

In a 3D-IC, path delays already experience variations [16]–[18] due to the physical and electrical conditions such as non-uniform switching, supply noise and crosstalk. These delay variations may create slow-down or artificial speed-up on path delay, obscuring small delay variations inflicted by resistive open TSVs that could let them go undetected. Therefore, our main objective is to determine whether the obtained delay increase is due to a resistive open TSV or due to the other physical-electrical factors. For our analysis, we consider that TSVs have an independent defect rate meaning that more than one TSV can be resistive open in the critical path. The next subsections show our proposed two correlation-based detection methods. In Method I, we provide path delay analysis considering *all* stage-path delays to contrast the TSV effect on path delay containing multiple TSVs. In Method II, we pinpoint which TSV is faulty by computing the path delay fault coverage of *each* stage-path individually.

A. Normality Check

As a prerequisite, we need to check that delay data is normal. We perform normality check for total path and stage-path delay with one resistive open TSV in a path with multiple TSVs. As shown in Figure 3, we observe total path and stage-path delay for different resistive open TSV values. As expected, delay increases with the presence of resistive open TSV and it impacts on the normal property of data. Also, we observe that the delay behavior in the non-detectability region have a non-normal shape. As in [19], it is possible to resample delay into subset of delay inside the detectability range. In our analysis, we screen stage-path and total path delay into resistive open TSV detectability confidence intervals. Thus, delay variations in a path can be represented by a normal distribution:

$$D_{totalpath} \sim N(\mu_{totalpath}, \sigma_{totalpath}) \quad (6)$$

where $\mu_{totalpath}$ is the mean and $\sigma_{totalpath}$ is the standard deviation.

B. Method I: Resistive open TSV(s) detection in a path with multiple TSVs

In this sub-section, we refer to *mixture stage-path delay* as the *mixture delay density function* of all stage-paths in the path. We present the mathematical formulation to quantify

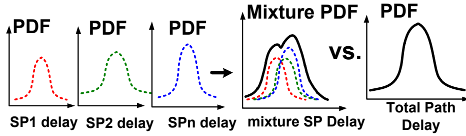

Fig. 4. Conceptual representation of Method I. Given a path with n stage-paths (SP) delay, we obtain the mixture probability density function of *all* stage-path delays and compare with total path delay.

correlation by deriving the correlation coefficient, in this paper represented by ψ, also referred as Pearson Product-Moment Correlation Coefficient (ρ). Our objective is to compute the correlation between the mixture distribution of *all* stage-paths in the path versus the total path delay, as shown in Figure 4. Here, we investigate the induced delay from resistive open TSVs and their impact in total path delay.

Similarly to the total path delay, stage-path delays can be represented by normal distributions. We assume that their mixture distribution function will still be a normal distribution. Thus, we can express the mixture distribution ($D_{mixture}$) as $D_{mixture} \sim N(\mu_{mixture}, \sigma_{mixture})$.

Definition: The mixture distribution F is a weighted sum of probability density functions (PDF) of a normally distributed random variable x [20]. Each PDF corresponds to a stage-path delay distribution from a path with n stage-paths.

Given the set of probability density functions $p_1(x), ..., p_n(x)$ of n stage-path delays in the path, we obtain the finite mixture distribution F [20] by:

$$F = \sum_{i=1}^{n} w_i p_i(x) \tag{7}$$

such that w_i is the mixture weight of each component density. w_i is the observation probability of each component and it must satisfy $w_i \geq 0$ and $\sum_{i=1}^{n} w_i = 1$. The w_i is computed during the Gaussian Mixture Model (GMM) parameters estimation. Each mixture component $p_i(x)$ is a Gaussian distribution with respect to the vector of delay values x. And $p_i(x)$ is parameterized by mean μ_i and standard variation σ_i. For $D_{mixture}$ the $\mu_{mixture}$ and $\sigma_{mixture}$ can be expressed as:

$$\mu_{mixture} = \sum_{i=1}^{n} w_i \mu_i \tag{8}$$

$$\sigma^2_{mixture} = \sum_{i=1}^{n} w_i(\sigma_i^2 + \mu_i^2) - \mu^2_{mixture} \tag{9}$$

For example, Figure 4 shows the mixture distribution, $D_{mixture}$ of n stage-path delay distributions. Thus, we compute the correlation coefficient of the $D_{mixture}$ versus the overall path delay D_{total}. The correlation ψ of the variables D_{total} and $D_{mixture}$ can be calculated as:

$$\psi = \left| \frac{cov(D_{mixture}, D_{total})}{\sqrt{var(D_{mixture})var(D_{total})}} \right| \tag{10}$$

and

$$0 \leq \psi \leq 1 \tag{11}$$

where, *cov* is is the covariance matrix and *var* is the variance. The covariation function is given by:

$$cov(D_{mixture}, D_{total}) = E[D_{mixture}D_{total}] - E[D_{mixture}]E[D_{total}] \tag{12}$$

where E is the mathematical expectation. The correlation coefficient ψ is bounded by *0* and *1*, a value close to zero means that TSV in stage-path is not the source of path delay variation. In addition, ψ values close to 1 means a significant correlation between the mixture stage-path delay and the total path delay, allowing us to determine path delay fault coverage. The path delay fault coverage of our method is shown by ρ_I:

$$\rho_I = \left| \left(1 - \left(\frac{\kappa}{n}\right)\right) - \psi \right| \tag{13}$$

where ψ is the correlation coefficient, κ is the number of faulty TSVs and n the number of TSVs in the path.

C. Method II: Resistive open TSV diagnosis in a path with multiple TSVs

After identifying that TSVs are the source of path delay variation, in this subsection we want to narrow down the solution space by identifying which TSV(s) are faulty. Here, we present the mathematical formulation to quantify the linear relationship between *each* stage-path delay versus ideal stage-path delay (i.e. no resistive open), by computing the correlation coefficient, as shown in Figure 5. Our objective is to pinpoint which TSV is faulty by computing the delay fault coverage of *each* TSV in a path with multiple TSVs.

As shown previously, delay variations in a critical path and stage-path delays can be represented by normal distributions. A single stage-path delay $D_{stagepath}$ is expressed by:

$$D_{stagepath} \sim N(\mu_{stagepath}, \sigma_{stagepath}) \tag{14}$$

Thus, ρ_{II} of $D_{nominalstagepath}$ versus $D_{stagepath}$ can be calculated as:

$$\rho_{II} = (1 - |\gamma|) * \beta \tag{15}$$

where

$$\gamma = \frac{cov(D_{stagepath}, D_{nominalstagepath})}{\sqrt{var(D_{stagepath})var(D_{nominalstagepath})}} \tag{16}$$

and β is the ratio factor given by:

$$\beta = max\left(\frac{\mu_{stagepath}i}{\mu_{ideal}}\right) \cong 1 \tag{17}$$

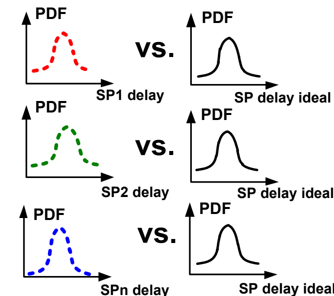

Fig. 5. Conceptual view of Method II. For *each* n stage-paths (SP) delay in a path, we obtain the mixture probability density function and compare with total path delay.each Stage-Path Delays.

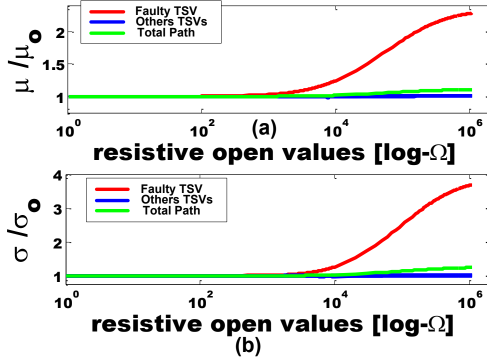

Fig. 6. In this example, we sweep resistive open TSV values for a path with n TSVs and only one is resistive open TSV while others remain ideal. We compute (a) the mean of *each* stage-path delay rationed by the nominal mean (i.e. ideal) and (b) the standard deviation of each stage-path delay rationed by the nominal standard deviation.

where μ_{ideal} is the mean of a stage path delay defect-free, no supply noise and no TSV-to-TSV coupling and $\mu_{stagepath}i$ is the i_{th} stage-path delay. ρ_{II} is bounded by $0 \leq \rho_{II} \leq 1$, where a ρ_{II} value close to *1* means a high detectability of resistive open TSV. And a value approximately *0* means stage-path delay distribution is very correlated with a defect-free TSV, where we can define not faulty, by this way, we pinpoint which TSV(s) are faulty. Thus, ρ_{II} allows us to identify the condition of TSVs in the path and to define our path delay fault coverage.

For example, in Figure 6, we can obtain the mean and the standard deviation values from the mathematical formulations for various resistive open values. In a path with n TSVs where, only one TSV is resistive open while others remain ideal (i.e. no resistive open). We sweep the open resistance values and we show the mean and standard deviation from the mathematical formulations. We observe that stage-delay distribution for the faulty TSV experiences a significant increase in their means and standard deviations as the resistive open values increases. Also, we observe that the mean and standard deviation from other stage-path delays with ideal TSVs remain constant. Whereas, the mean and standard deviation from the total path increases with resistive open TSV indicating its influence on the overall path delay.

V. Simulations Results

In order to show the effectiveness and applicability of our proposed methods, we use a simple sample circuit as shown in Figure 7 that illustrates a realistic 3D circuit taking into account physical and electrical factors such as TSV parasitics and voltage levels fluctuations. Moreover, each TSV is surrounded by the TSV interface as in Figure 2. We utilize

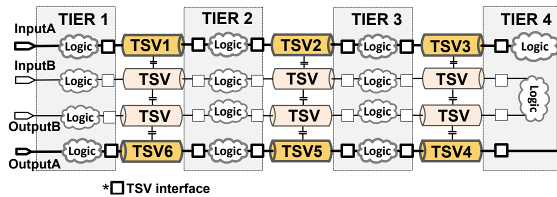

Fig. 7. Sample circuit used for our experiments have two paths containing multiple TSVs. Each path has *six* TSVs that are surrounded by TSV interface.

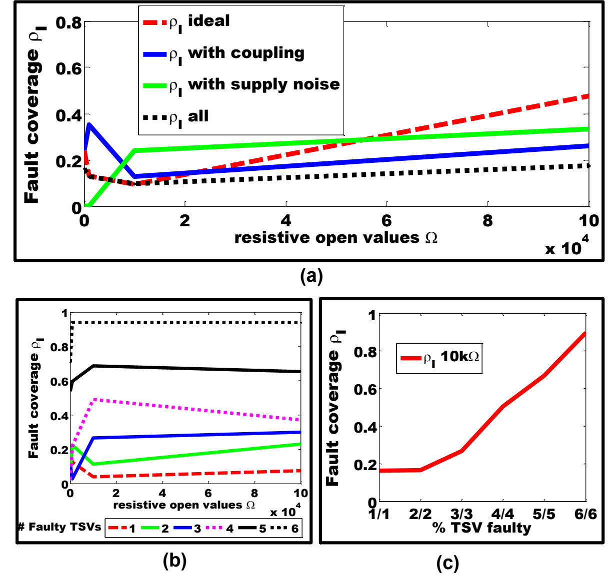

Fig. 8. Method I, ρ_I is the fault coverage of our correlation method between the mixture distribution of *all* stage-path delays in the path versus the total path delay. In (a), we study resiliency of TSVs with conditions in path delay such as supply noise, coupling and with both coupling and supply noise (worst case) and the ideal distribution (i.e. no supply noise and no coupling). In (b), ρ_I versus open resistances (from 0 to $0.1M\Omega$) for different number of faulty TSVs in a path with *6* TSVs. In (c), Faulty coverage of the TSV faulty percentage in the path with $10k\Omega$ resistive open with ideal conditions (i.e. no supply noise and no coupling).

TSVs of $3\mu m$ radius and $15\mu m$ length and their parasitics are extracted in [21], also we consider TSV-to-TSV coupling with TSV pitch of $50\mu m$.

Our sample circuit has two critical paths with multiple TSVs and each path has *six* stage-paths. We perform HSPICE simulations to capture delay variations in path delay and contrast with the resistive open TSV effect on delay. The results are based on the path containing the TSVs $\{TSV1, TSV2, ..., TSV6\}$. We insert resistivity open defects in range of 0 to $1M\Omega$. The intra-die logic gates circuitry was synthesized using *Nangate Open Cells 45nm cell library* with V_{DD}=1. In our analysis, we consider various conditions such as input vectors (i.e. *8* test vectors for *Input A* and *Input B*), TSV-to-TSV coupling and supply noise fluctuations either for power and ground up to *10%* variation. Thus, each stage-path distribution is obtained with *64* delay measurements while sweeping all parameters above mentioned.

We use MATLAB to perform our mathematical analysis and to compute the correlation-based detection method given the measured delay. First, in Method I, we compute the linear relationship between the mixture distribution of *all* stage-path delays versus the total path delay, to contrast if faulty TSV are the source of delay in total path. Second, in Method II, given that we identified if TSVs are the source of delay, we pinpoint which TSV(s) are faulty.

A. Applying Method I to identify if TSVs are the source of path delay

Here, we perform delay analysis considering *all* stage-paths. We use MATLAB to calculate the mixture distribution of *all six* stage-path delays. Then, we compute ρ_I to evaluate the

relationship between mixture distribution delay versus total path delay. We aim to assure that TSVs are the source of the introduced delay rather than other physical and electrical conditions (such as supply noise, parasitics and coupling), we analyze our proposed path delay fault coverage method inserting resistive open values in only one TSV in the path under different conditions, as shown in Figure 8. Figure 8.a shows ρ_I for ideal case (i.e. no noise and no coupling) and supply noise worst case ($V_{DD} = 0.9$ and $V_{SS} = 0.1$), where we observe that path delay is affected up to 23% in the path fault coverage. We also observe a variation in path delay fault coverage of 33% in presence of TSV-to-TSV coupling ($50\mu m$ of pitch). For both supply noise and TSV-to-TSV coupling we obtain up to 99% in accuracy of our method for varying all parameters. Figure 8.b shows ρ_I for different number of faulty TSVs in the path with *six* TSVs, in this experiment we consider different test vectors, coupling and supply noise at worst case setup. In Figure 8.c the path delay fault coverage of our method, ρ_I is computed for varying number of faulty TSVs in the path with ideal conditions for a TSV resistive open value of $10k\Omega$. We observe that as the number of faulty TSVs increases, greater is the detectability of our method.

B. Applying Method II to determine which TSV(s) are resistive open

After the identification that resistive open TSVs are the cause of path delay increase, we analyze stage-paths individually to identify which TSV(s) are the source of increase on delay. For our experiments we use the circuit shown in Figure 7 that contains *six* TSVs in the path and we insert TSV open resistance values from *small* (i.e. $0 \leq R < 10k\Omega$); *mid* i.e. ($10k \leq R < 100k\Omega$), and *big* (i.e. $100k \leq R < 1M\Omega$). Then, we compute ρ_{II} derivation for *each* stage-path individually, as shown in Figure 9. In order to verify which TSV is faulty, in Figure 9.a we observe ρ_{II} for only one resistive open TSV within the path. For each faulty TSV, we compute ρ_{II} of faulty stage-path delay distribution versus the nominal stage-path delay. Figure 9.b shows the comparison of both methods while considering supply noise and TSV-to-TSV coupling.

VI. Conclusion

This work proposes a correlation-based resistive open TSV detection method that explores mathematically delay models by dividing the path delay in stage-path delays. We perform our mathematical analysis and electrical simulations considering a typical 3D test architecture, with physical and electrical conditions such non-uniform supply voltage, producing a more realistic solution to the problem. Our proposed method investigate if faulty TSVs are the cause of delay variations in a path with multiple TSVs. After identifying that TSVs are the source of timing variation we compute our correlation-based resistive open TSV detection to identify which TSV(s) cause it. Experiments show that is possible to detect resistive open TSVs with good accuracy (99%) with the correlation-based method.

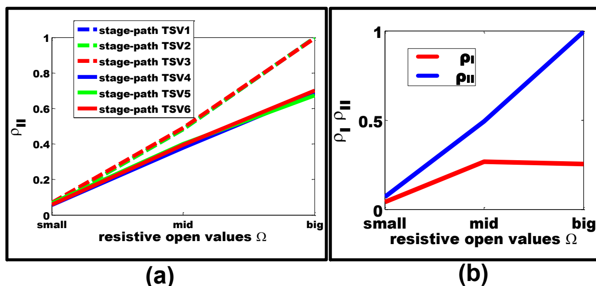

Fig. 9. In (a), ρ_{II} vs. resistive open TSV values for different faulty TSV in the path. In (b), we compare both methods ρ_I and ρ_{II} with supply noise and TSV-to-TSV coupling for many resistive open values. We consider resistive open values (R) in three distinct ranges; *small* from 0 to $10k\Omega$; *mid* from $10k$ to $100k\Omega$; and *big* from $100k$ up to $1M\Omega$.

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