# Asynchronous Design for Harsh Environments

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***Abstract*—Radiation robust circuit design for harsh environments like space is a big challenge for today engineers and researchers. As circuits become more and more complex and CMOS processes get denser and smaller, their immunity towards particle strikes decreases drastically. This work has for objective to improve the SoC robustness against particle attacks targeting very advanced processes. This should be possible combining three already proven robust design techniques: Asynchronous communication, Silicon on Insulator (SOI) technologies and Spintronics (MRAM). The combination of these three techniques should give some fundamentally new architecture with higher performances than what is available today in terms of robustness but also in terms of speed, consumption and surface.**

## I. Introduction

TODAY, there are several ways to develop microelectronic circuits adapted for space applications that meet the harsh constraints of temperature range, voltage and most importantly immunity to radiation, whether in terms of technical design or manufacturing process. The aim of this work is to improve circuit robustness targeting several very advanced techniques and approaches of microelectronics to design architectures adapted to this type of radiative environment. The techniques used here are: Asynchronous communication, Silicon on Insulator (SOI) technologies and magnetic memory (MRAM) technology. Such an assembly would be totally innovative and should benefit without precedent, in terms of silicon area, consumption and robustness which is the main target of our work.

In addition to having a particularly low consumption compared to the synchronous circuits and being almost insensitive to delays and therefore to changes in manufacturing process, asynchronous circuits can be considered more robust towards SEE than traditional design [1]. Secondly, it is widely recognized in the field of microelectronics that integrated circuits manufactured on SOI substrates are more robust to radiation due to the smaller volume of the active areas of the transistors [4] and also thanks to the possibility of local insulation provided by the manufacturing process. The radiation-induced errors are very localized and therefore cannot be spread from one block to another. Finally, non-volatility in space application opens new opportunities for systems, for example the possibility to reload the system in a previously known state after strategical storage management. One of the important parts of this work will also be to integrate inherently radiation robust non-volatile components, such as Magnetic Tunnel Junctions (MTJ) (Fig. 1) which are the basic element of MRAM. MTJ devices are composed of two ferromagnetic layers separated by an insulator called tunnel barrier. Data is stored in the form of the direction of the magnetization and not in the form of an electric charge which makes these devices intrinsically immune to radiations [2].

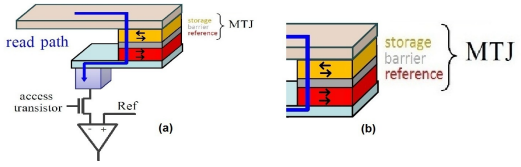


Fig. 1. Example of a Magnetic Tunnel Junction: (a) Sense reading in a MTJ (b) Zoom on the active part of the junction.

In this paper we will present a preliminary study of the performance of asynchronous and synchronous design towards particles strikes. We chose to simulate the effect of heavy ions since they are one of the most energetic and dangerous particles for electronic circuits. They are produced by solar wind or flares and have energies from a few $keV$ to $10MeV$. The effect of a heavy ion hitting a transistor has been documented in the past and has shown that the most sensitive strike location of a transistor is the drain [3].

## II. Simulation results

We started off by designing two memory elements of synchronous and asynchronous design. A Flip-flop and a Half-Buffer for respectively synchronous and asynchronous [6]. These two structures conduct the same role in the two worlds and were designed to have the same timing characteristics so they could be compared coherently.

All simulation results presented in this paper were run with Spectre electrical simulator under Cadence Analog Design Environment platform using the 28nm FD-SOI technology from ST Microelectronics.

### A. Particle injection

To simulate the effect induced by a particle hitting the drain we inject a current pulse which has the same characteristics

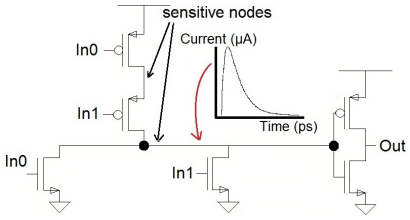


Fig. 2. Example of a particle injection (current pulse) in an OR gate.

as a heavy ion strike to the drain of a transistor. This current pulse is determined by the following equation [5]:

$$I_{inj} = \frac{Q_{inj}}{\tau_1 - \tau_2}(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}})$$

Where $Q_{inj}$ is the charge in Coulombs of a particle that vary from $-2pC$ to $2pC$, $\tau_1$ and $\tau_2$ are material dependant constants, here respectively $150ps$ and $50ps$. This current pulse will be sequentially injected in all the sensitive nodes of the evaluated circuit to determine the global sensitivity of the circuit (Fig. 2). A sensitive node being any internal node except nodes connected to the supply voltage, ground, or any of the inputs or outputs.

### *B. Influence of the supply voltage*

We conducted particle strike simulations at different supply voltages. In both synchronous and asynchronous designs, we observed the inverse relationships between supply voltage and the amplitude on the induced pulse. This can be explained by the fact that, as the supply voltage increases the conductance of the transistor increases also.

### *C. Impact of the threshold voltage*

In the 28nm FD-SOI design kit we have the choice between LVT (Low $Vt$) and RVT (Regular $Vt$) transistors. In our initial hypothesis RVT transistors would be more robust to particle strikes than LVT because of their superior $Vt$, thus less sensitive to commutations. The simulation results demonstrated that LVT are more robust for both synchronous and asynchronous designs. This can be explained by the fact that LVT transistors have a higher leakage current than RVT, so the induced current pulses are evacuated quicker due to the higher leakage.

### *D. Influence of body biasing*

FD-SOI enables us to use body biasing to play around with the $Vt$ of transistors. We then looked at the influence of vbb (body biasing voltage) in particle induced errors. In RVT transistors, as vbb increased (boost configuration, $Vt$ decreases) the global number of errors induced by heavy ion strikes on the circuit decreased. As the transistors response is boosted the accumulated charges caused by particle strikes can be evacuated quicker. Concerning LVT transistors, being already more robust to particles than RVT, increasing or decreasing vbb has no further effect on them (Fig. 3). Once again both designs reacted in the same way to body biasing.

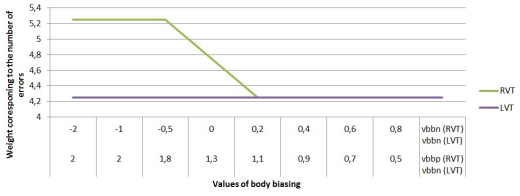


Fig. 3. Graphical representation of the number of particles induced errors depending on the Body Biasing.

## III. Conclusion and perspectives

This preliminary work has allowed us to fully understand the influence of heavy ion strikes on transistors in both synchronous and asynchronous worlds. We have seen the influence of the supply voltage and body biasing on LVT and RVT transistors when confronted with particles strikes. The simulation results have demonstrated that using the highest supply voltage permitted by the technology, in conjunction with LVT transistors is the best option to harden systems at transistor level. The differences between synchronous and asynchronous design can not be determined with transistor level simulations on simple structures. Since the differences are based on the communication protocols, the robustness of one design method over the other should become visible in a more complexe architecture such as a pipeline structure.

Our next step will be to compare both asynchronous and synchronous architectures in a pipeline to see how the errors are propagated through the different stages; this should give us an in-depth comparison of both asynchronous and synchronous design towards radiative environments. Another major step will be the manner of integration of MTJs in the Half-Buffer and Flip-Flop rendering them non-volatile and potentially even more robust. This will lead to the final step of our study which will be hardening techniques by design such as DMR (Dual Modular Redundancy) and TMR (Triple Modular Redundancy). Indeed, the use of non-volatility thanks to MTJs should allow the restoration of secure data after a particle strike. This will allow us to compare both synchronous and asynchronous architectures in new conditions to determine which is more robust in harsh radiation environments.

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