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Rudy Ferraro, Salvatore Danzeca, Matteo Brucoli, Alessandro Masi, Markus Brugger, et al.. Design of a Radiation Tolerant System for Total Ionizing Dose Monitoring Using Floating Gate and RadFET Dosimeters. TWEPP: Topical Workshop on Electronics for Particle Physics, Sep 2016, Karlsruhe, Germany. lirmm-01382578

#### HAL Id: lirmm-01382578 https://hal-lirmm.ccsd.cnrs.fr/lirmm-01382578

Submitted on 17 Oct 2016

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# Design Of A Radiation Tolerant System For Total lonizing Dose Monitoring Using Floating Gate And Radfet Dosimeters





R. FERRARO, S. DANZECA, M. BRUCOLI, A. MASI, M. BRUGGER and L. DILILLO

### 1. Abstract

The Total Ionizing Dose Monitor (TIDMon) is a radiation tolerant system designed to measure the effect of the TID on a new prototype of Floating Gate Dosimeter (FGDOS) and compare it against the Radiation-sensing Field Effect Transistors (RadFETs) dosimeter.

In this work we present the design strategy adopted for the control of the sensors and the architecture, the radiation reliability and the performance achieved by the system.

# 2. Design Choices

#### Two parts compose the system:

- The tester part which is a generic radiation tolerant architecture able to acquire mixed-signals from the DUT and perform complex data processing.
- The DUTs part that contains the dosimeters sensors and the circuitry needed to manage them.

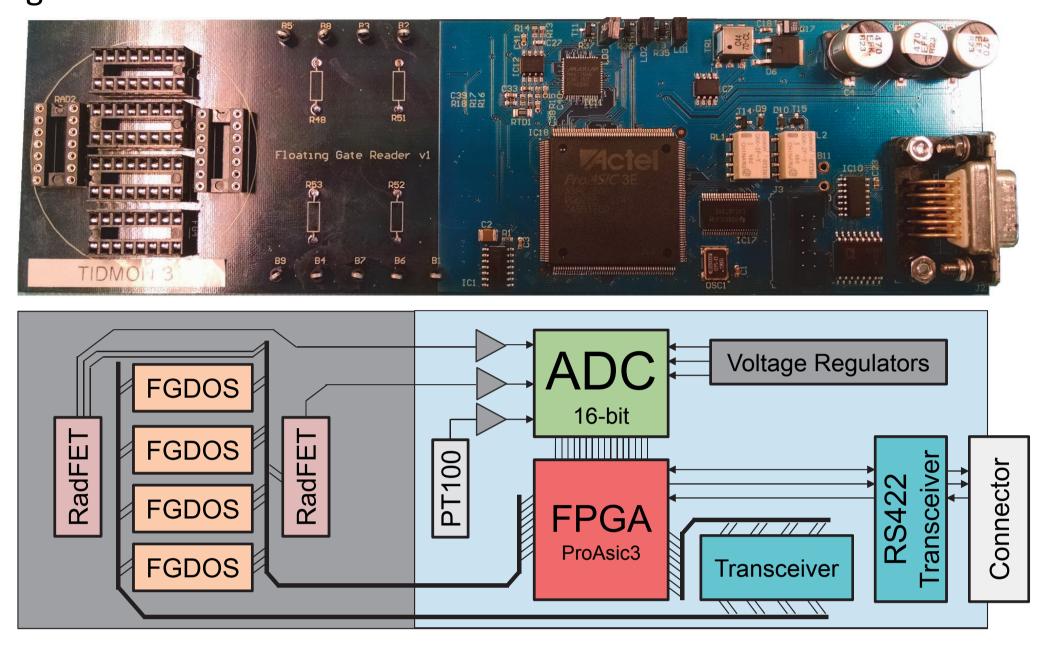


Figure 1 – TIDMon board and general hardware architecture with on the right the Tester part and on the left the

#### The tester part is composed of :

- A Flash-based FPGA which offers us the possibility to improve continuously the embedded sensor controllers and to manage online different test configurations.
- A **16-bit ADC** and Op Amps that allow the measuring of the DUT values: RadFET voltages, RadFET current source and floating gate currents.
- Monitored Voltage Converters for the powering of the DUTs and Tester elements.

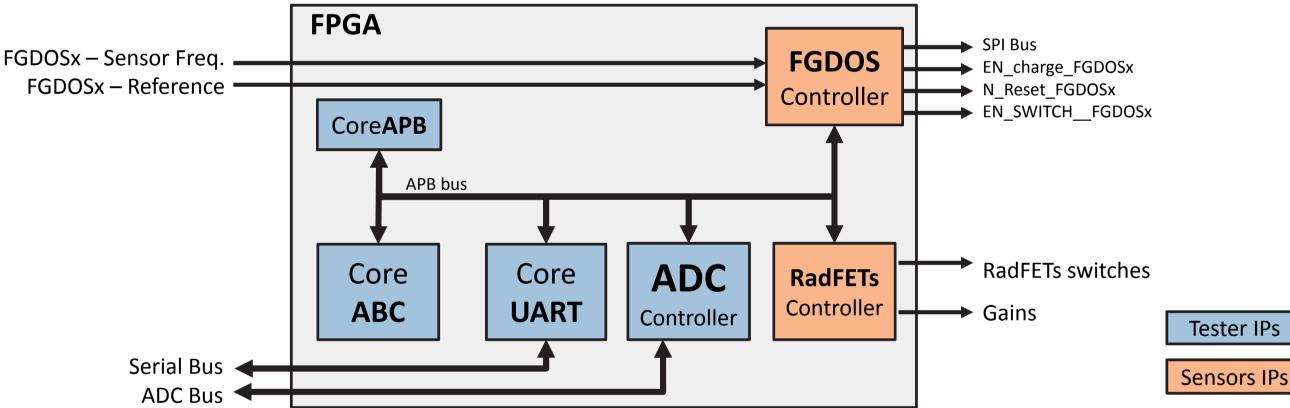


Figure 2 – TIDMon FPGA architecture with in blue the generic IP provide by the tester structure and in orange the dedicated IP for the DUTs

### Four IP cores constitute the generic tester part :

- **The CoreABC,** an assembler-based configurable softcore provided by MicroSemi which is the master of the system. The core contains in assembly-based language the reading routine of the sensors.
- The CoreAPB, an APB interface to connect the slave IP cores to the CoreABC.
- The CoreUART, a configurable APB serial controller provided by MicroSemi.
- The ADC Controller which provides the measurements of the analogue values of the sensors and the reference values of the board.

### Two IP cores are dedicated to the sensors :

- The FGDOS Controller performs the measurement of the frequencies and manages up to four FGDOS.
- The RadFETs Controller performs the reading procedure for up to two RadFETs.

### 4. Radiation Assurance

- ➤ A Triple Modular Redundancy (TMR) mitigation technique is applied on the FPGA IP cores at the register level by means of a commercial synthesis tool and at the memory level manually.
- > The board is entirely based on **COTS** components tested against radiation effects:
  - SEEs and TID: 230 MeV protons (up to  $9.10^{11} p/cm^2$ )
  - <u>Displacement damage:</u> 1 MeV neutrons (up to  $4.10^{12} n/cm^2$ )
  - **TID:**  $^{60}Co$  source up to 50 krad(Si) TID

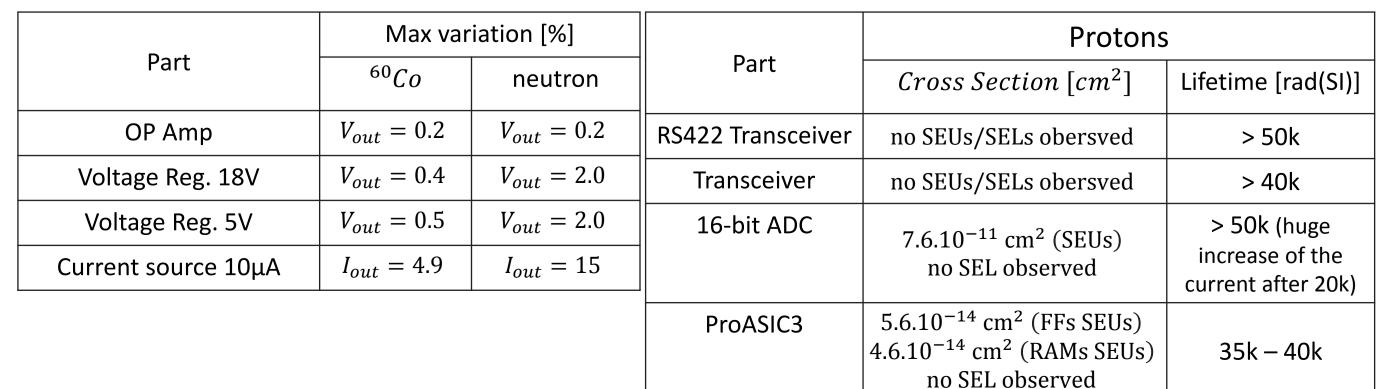


Figure 3 – Summary of the results of the radiation test campaigns on the main analogic and digital components

## 3. TID Monitoring procedure

The TIDMon measures every second the TID sensors and also the voltage regulators and the current source of the board in order to monitor the level of degradation of the tester.

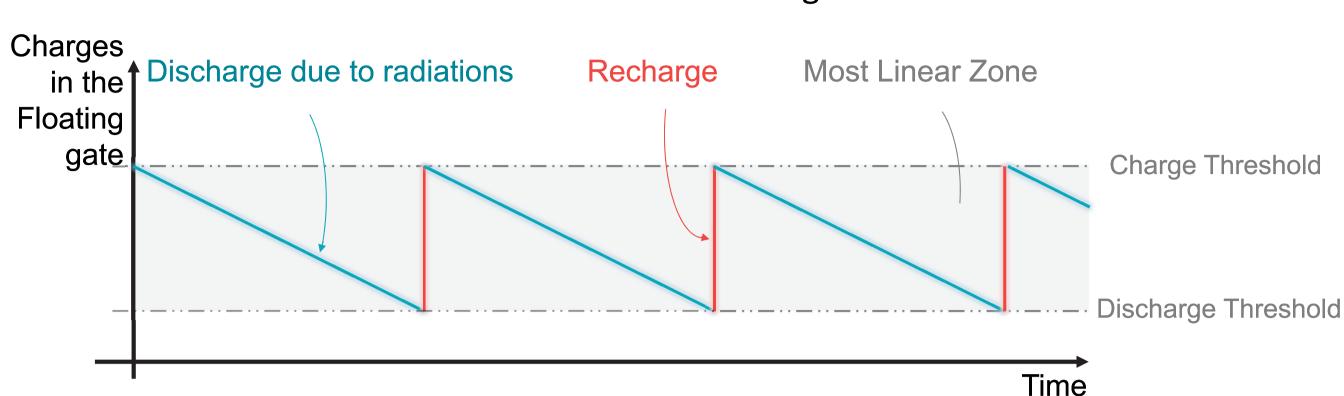


Figure 3 – Functional operation of FGDOS during irradiation, the output of the sensor is provides by an embedded Voltage Controlled Oscillator (VCO) that convert the gate potential in a square wave signal.

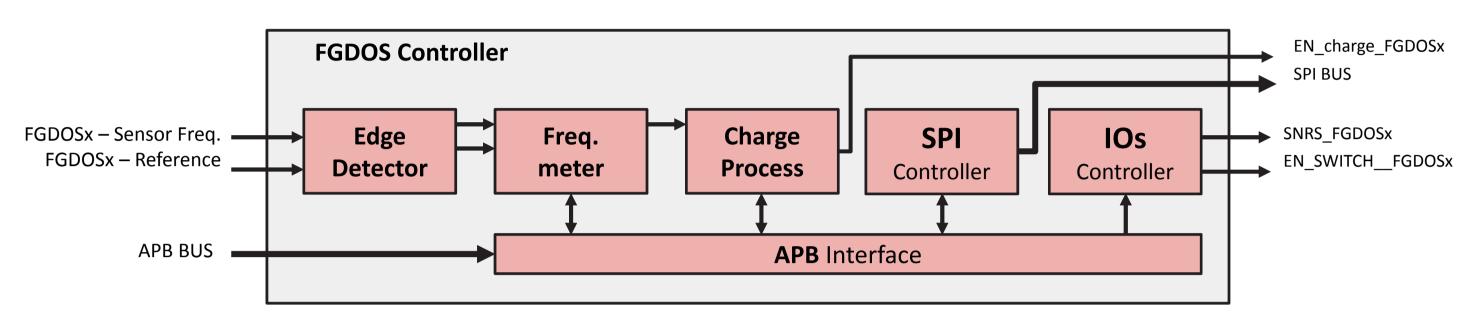


Figure 4 – FGDOS controller IP architecture

- The frequency meter process used two sub-processes :
  - A precise one that calculates the frequency in 1s with an accuracy of 1 Hz.
  - A fast one that calculates the frequency in 15ms with an accuracy of 128 Hz.
- The charge process recharges automatically the sensor to a desired value when it is discharged below a defined threshold. These two values are configurable online.
- The SPI interface allows to:
  - Set the radiation sensitivity (High / Low)
  - Read the internal temperature sensor
  - Bypass the VCO, to have on the output the current of the reading MosFET of the floating gate.

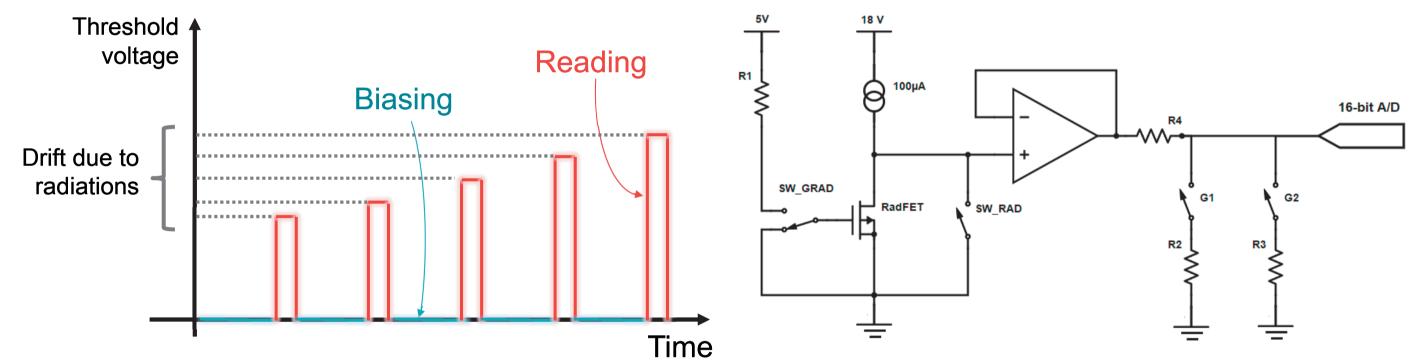


Figure 6 – RadFET Dosimeter reading procedure and circuit with ADC Gains which allows the exploitation of the full range of the sensors.

- Reading Step: The gate and drain are shorted to the ground, and the sensor is supplied by a current source for a period of 100 ms.
- <u>Biasing Step</u>: The drain, source and gate pins are shorted to the ground. The gate can be biased to 5V in order to increase the sensibility.

## 5. Results

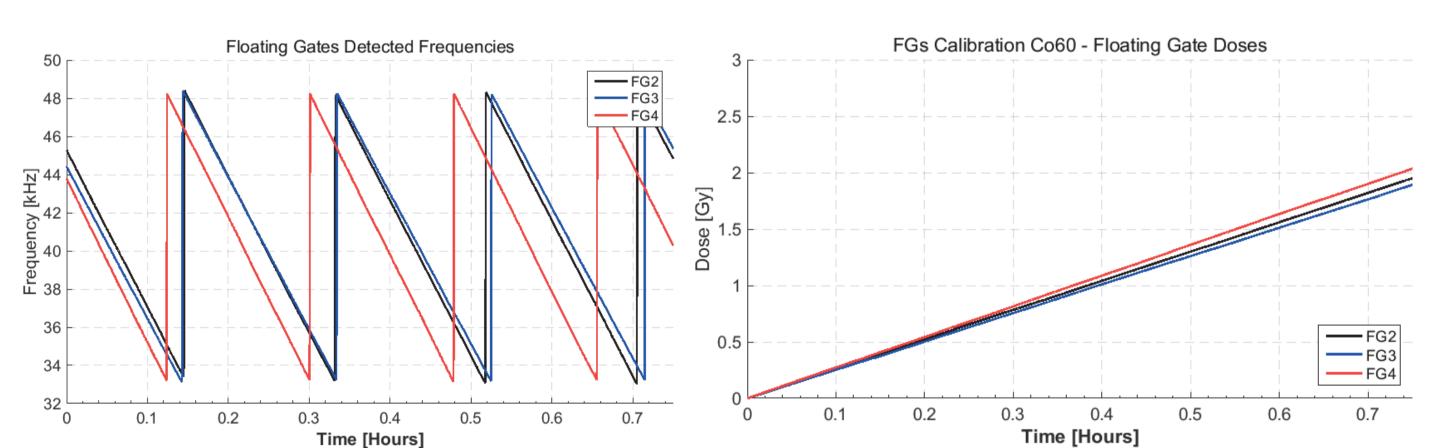


Figure 7 – FGDOS measurement perform during a  $^{60}Co$  radiation test campaign and the corresponding processed dose.

- In the nominal configuration of the FGDOS with a sampling of 1 Hz, the TIDMon is able to charge the sensors in less than 1 sample, thus the **blind time is reduced to the minimum**.
- > The TIDMon can achieve a measuring accuracy of 16 mrad(SI).
- $\succ$  The board worked without issues during the several test campaigns performed at CHARM mixed-field facility or with  $^{60}Co$  irradiation.

### 6. Conclusions

- > The TIDMon allows us to finely characterize and find the best conditioning to use the FGDOS with the maximum of performance as a TID sensor for CERN dosimetry purposes.
- The tester architecture proved to be **robust against various harsh radioactive environments** and can operate up to 30 krad(SI).
- > The next step to consider for the Tester architecture will be to extend the lifetime of the architecture actually limited by the increase of the ADC current consumption as a result of the accumulated dose.
- The performances and the modularity of the test architecture provides us a quick and robust, ready-to-use test system able for other CERN radiation testing activities.