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*Abstract*— This work investigates the effects of aging and voltage scaling in neutron-induced bit-flip in SRAM-based FPGAs. Experimental results show that aging and voltage scaling can increase in at least two times the susceptibility of SRAM-based FPGAs to Soft Error Rate (SER). These results are innovative, because they combine three real effects that occur in programmable circuits operating at ground-level applications. In addition, a model at electrical simulation for aging, soft error and different voltages was described to investigate the effects observed at the practical neutron irradiation experiment. Results can guide designers to predict soft error effects during the lifetime of devices operating in different power supply mode.

*Keywords—FPGA; radiation; aging; volage scalling*

## I. INTRODUCTION

Aging and soft errors have become the two most critical reliability issues for nano-scaled CMOS designs. However, to the best of our knowledge, the literature has not reported the influence of aging in SRAM-based FPGAs in the soft error rate. In FPGAs, millions of SRAM cells are used as configuration memories to customize the configurable matrix in the user's design. We investigate the SER in SRAM-based FPGA fabricated in 45nm CMOS technology under neutron-induced effects when accelerated aging has been performed. We compare the measured sensitive area (cross-section) of the device post aging exposed under neutron to the sensitive area reported by the fabricant. Results show that the sensitive area can increase more than twice due to aging effects. In addition, some FPGAs working in harsh environment may operate in systems with serious limitations of power due to its remote access. It is well known that SRAM-based FPGAs present a relative high static and idle power due to its millions of SRAM cells presented in the configurable memory bits. In order to reduce this power consumption, one common technique is to reduce the voltage supply of the entire FPGA core [1]. However, when doing that, the FPGA may be more susceptible to soft errors as well.

In this work, we analyze the combination of those three effects: soft error, aging and voltage scaling. We performed practical neutron-induced soft error rate experiments in SRAM-based FPGA under aging-induced variations and voltage scaling and compare the results with the ones from the electrical simulation method. Results at electrical level simulation can predict an increase the soft error susceptibility by at least twice, when aging is also considered. The same proportion was measured under radiation.

## II. PROPOSED METHODOLOGY: AGING, VOLTAGE SUPPLY AND SOFT ERROR RATE MEASUREMENTS

The selected device for this work is the Spartan-6 Xilinx FPGA. This device is manufactured with a 45nm technology and has a nominal core voltage of 1.2V. All these resources are configured by a bitstream composed of 11,939,296 bits that are loaded into the SRAM configuration memory bit structure. The FPGA was configured with as array of Ring Oscillators (RO) as depicted in Fig. 1. Four gates were used for the structure of the RO, manually placed and routed into 3411 CLBs of the FPGA.

Aging is a natural process that any integrated circuit suffers during its lifetime. The effects of aging can be seen as the degradation of a circuit in terms of its performance and also an increase in the leakage current. In order to analyze the effect of aging in FPGAs, it is possible to perform aging acceleration.

This one is achieved by exposing the FPGA to an elevated temperature and core voltage [2]. For this purpose, the core was supplied by a voltage of 1.8V using an external power supply. The FPGA was heated to 80°C using a thermal chamber, while a stress-design was in operation (to maintain a switching activity at given locations). The aging period refers to 10 days, including 7 days of effective aging and 3 days of recovery, required to clear the effects of reversible aging.
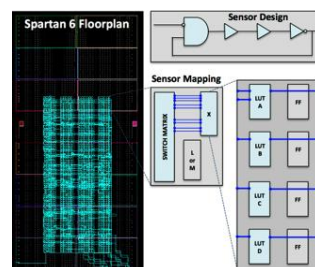


Fig. 1. Group of ring oscillators into the FPGA.

To measure the impact of aging on FPGA, the FPGA was characterized before and after aging using an ElectroMagnetic (EM) method proposed in [2]. Each RO oscillates at a specific frequency, which is directly related to Process, Voltage and Temperature (P,V,T). Voltage is controlled using a high precision DC power supply. The temperature is fixed using a thermal chamber. Fig 2 shows the degradation.
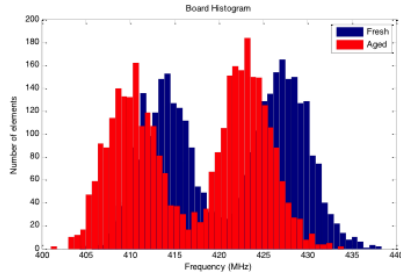


Fig. 2.  Frequency degradation due to aging

In order to evaluate the influence of voltage scaling and aging for soft errors, two FPGAs were tested: one FPGA without stress (here after "FPGA before stress") and one FPGA stressed (here after "FPGA after stress"). The neutron radiation tests have been performed at the ISIS facilities located at the Rutherford Appleton Laboratory (RAL) in the Didcot, UK. Irradiation was performed at room temperature with normal neutron incidence. The FPGA boards and the power supply are placed in the radiation chamber, while the computer used to monitor the test remotely is located in the control room. The two FPGAs were irradiated with an average neutron flux of $3.43 \times 10^4$ n/(cm$^2$.s) and $4.10 \times 10^4$ n/(cm2.s) respectively. The neutron fluence is calculated as the product of the average neutron flux and the time the FPGAs are exposed to the neutron flux. With the aim of characterizing the soft error rate susceptibility of both FPGAs, the bit-flip cross-section per bit is calculated as defined:

$$\sigma_{SEU-bit} = \frac{N_{SEU}}{\Phi_{neutron} \times N_{bits}}$$

Where $N_{SEU}$ is the number of bit-flips (SEU), $\Phi_{neutron}$ is the neutron fluence and $N_{bits}$ is the number of bits of the device. Fig. 3 presents the cross-section per bit of configuration memory bits for both FPGAs and for the three different supply voltages: 1.2V (nominal), 1.1V and 0.95V. As the power supply voltage is reduced, the neutron cross-section for both FPGAs increases. Moreover, we also observe that the aging process impacts more significantly the cross-section than the voltage scaling.

### III. Monte-Carlo Simulations

Fig. 4. shows results obtained by Monte Carlo simulations where the critical charge of a SRAM cell (Qcrit) is strongly related to the bias voltage, in a trend, which is in accordance to that observed by [3]. Also, it is clear that the threshold voltage of the pull-up PMOS transistor increase due to BTI effects, one of the main effects of aging, which degrades Qcrit of the cell.

For short transient pulses simulated at electrical level, the impact of bias voltage reduction on Qcrit is low, which may cause the impact of aging to dominate the critical charge degradation. Final version of the paper will present more details of the electrical level prediction model and the practical results.
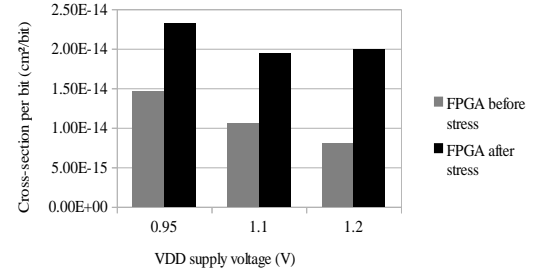


Fig. 3.  Cross-section for FPGAs before and after stress (aging effect) for different power supply modes
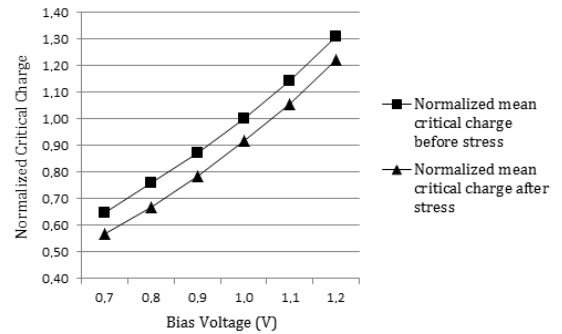


Fig. 4.  Effect of the critical charge in a SRAM cell according to the bias voltage for SRAM before and after stress (aging effect)

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