Alleviating Through-Silicon-Via Electromigration for 3-D Integrated Circuits Taking Advantage of Self-Healing Effect

Yuanqing Cheng, Aida Todri-Sanial, Jianlei Yang, Weisheng Zhao

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A Study of 3-D Power Delivery Networks With Multiple Clock Domains

Aida Todri-Sanial, *Member, IEEE*, and Yuanqing Cheng, *Member, IEEE*

***Abstract*— Ongoing advancements in 3-D manufacturing are enabling 3-D ICs to contain several processing cores, hardware accelerators, and dedicated peripherals. Most of these functional units operate with independent clock frequencies for power management reasons or simply for being hard intellectual properties. Thus, as diverse and heterogeneous circuits can be implemented on a 3-D IC, it also leads to the use of multiple clock domains. While these domains allow many functional units to run in parallel to exploit 3-D potentials, they also introduce power delivery challenges. This paper proposes an efficient analysis for assessing the worst case power supply noise on 3-D power delivery networks (PDNs) with multiple clock domains. This paper discusses power and thermal integrity issues that arise from multiple clock domains that share the same 3-D global PDN. We first examine power supply noise distribution on each tier and investigate scenarios that lead to worst case noise. Thermal analyses are also performed and heat distribution among clock domains and tiers is examined. In addition, the impact of clock domain structure and frequency on the overall power supply noise and temperature distribution has been quantified. Experiments show that the multiclock domains can induce excessive noise and the through-silicon-vias can contribute to power supply noise and heat transfer among tiers. This paper presents a summary of guidelines for modeling, analyzing, and exploring a design of reliable 3-D PDNs with multiple clock domains.**

***Index Terms*— 3-D ICs, clock networks, power and thermal integrity, power delivery networks (PDNs), through-silicon-vias (TSVs).**

I. Introduction

LONG global interconnects are the principal performance bottleneck for high-performance system-on-chip (SoCs) [1]. Such long interconnects are becoming the main obstacle in terms of communication bandwidth, latency, and power consumption [2]. Network-on-chip (NoC) architectures have emerged as an efficient methodology to offset such drawbacks and outperform mainstream bus architectures [2], [3]. Today, SoC designs are getting more complex and a variety of intellectual-property (IP) blocks can be integrated in them. These designs often employ several processors, memories, and special function units. Each of these blocks can operate at different frequencies and often require individual clock domains.

To further exploit the use of various functional blocks in the same package, 3-D integration presents a path toward higher circuit density and bandwidth in small form factor. The 3-D integration leverages on the vertical direction to minimize communication distances, increase the number of cores/IPs, and provide more connectivity among the blocks. In addition, 3-D technology enables heterogeneous integration and new class of applications and systems through significantly improved performance and energy efficiency of complex architectures [3], [4]. These heterogeneous systems often require multiple clock domains.

Current manufacturing advancements have led to the development of through-silicon-vias (TSVs) with fine pitch and thinned dies to accommodate stacking of several circuit layers. There are many research centers that investigate 3-D integration and are designing complex systems, such as stacking of several memory layers on top of logic, sensors and actuators on top of logic, and multicore systems connected through TSV arrays [5]. The synergy of using 3-D integration and NoC is making possible to shorten communication distances, thus improving performance and ultimately reducing overall power consumption.

The continuing drive for higher performance systems has led to unprecedented increase in clock frequency and even more so due to the growing need of smart and connected electronic devices and systems. One of the challenging tasks for an efficient 3-D design is the distribution of clock across a large system with multiple tiers while meeting the clock skew and slew budgets. A widely and effective applied method for 3-D and even 2-D systems is to design globally asynchronous clocks and abandon the single clock synchronous systems. Such paradigm introduces multiple clock domains and accommodates cores and/or IPs to operate at different frequencies while in a single system. Multiple clock domains are also widely effective not only for implementing different functional blocks but also for power management and energy-efficient system design [6].

However, the use of multiple clock domains poses the challenges on reliable delivery of power supply voltage to each tier on a 3-D stack. There are several challenges that the multiple clock domains introduce to 3-D power delivery networks (PDNs). Assume that there are two clock domains on tier 1 ($T1$), as shown in Fig. 1. Block 1 with freq_1 has fast switching and power hungry circuits, while block 2 with

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A. Todri-Sanial is with the Department of Microelectronics, Laboratoire Informatique Robotique Microelectronic de Montpellier and French National Center of Scientific Research (CNRS), Montpellier 34095, France (e-mail: aida.todri@lirmm.fr)

Y. Cheng is with the School of Electrical and Information Engineering, Beihang University, Beijing 100191, China (e-mail: yuanqing@ieee.org).

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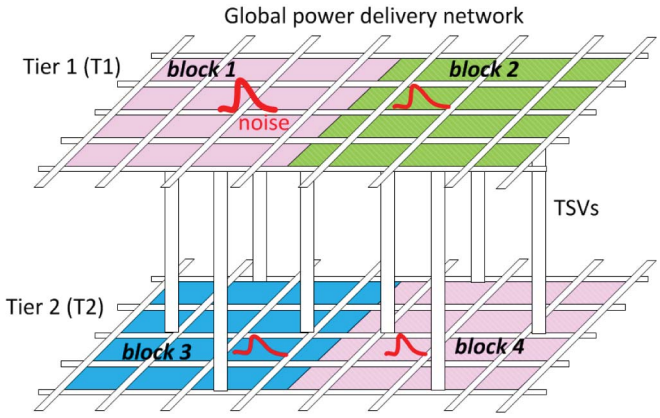

Fig. 1. Illustration of a two-tier 3-D PDN with several blocks representing multiple clock domains.

$freq_2$ has slow switching with low-power demand circuits. Both these blocks operate with the same voltage supply and share the global power grid. Due to fast and frequent switching of block 1, voltage fluctuations (power supply noise) are introduced on the power grid, which consequently impact the performance of block 2. Furthermore, TSVs serve to connect power networks among tiers, but undesirably they also transfer power supply noise between them. For example, block 3 in tier 2 ($T2$) will also experience excessive voltage fluctuations due to the noise transfer from $T1$ to $T2$. Worst case noise may occur when a block is experiencing self-induced noise and transferred noise from neighboring clock domains or tiers that can lead to critical performance issues. We will elaborate on derivation and quantifying these two types of noises later on this paper.

Heat dissipation and transfer among tiers exhibit a similar trend but in the reverse direction. Circuit blocks that are near to heat sink benefit from immediate cooling also referred to as primary heat flow path, while circuits that are further away experience higher temperatures. The tiers next to package have some of the heat alleviated due to the secondary heat flow path from die to package, whereas the middle tiers tend to experience higher temperature gradients. TSVs conduct the electrical connections between tiers but also transfer heat from a hot to a cooler tier, hence contributing to nonuniform thermal gradients in a tier and between tiers [7], [8]. The heat transfer between the tiers creates thermal wave zones around the TSVs, and hot spots can be created on the overlapping of these waves, which can detrimentally impact the performance of devices and parasitics of interconnects and eventually lead to Joule heating phenomenon [8]. Hence, multiple clock domains facilitate power management and improve communication latencies, but also introduce critical reliability concerns on 3-D PDNs due to nonuniform power supply and temperature distribution.

The objective of this paper is to investigate the worst case power supply noise and temperature distribution on 3-D PDNs due to 3-D heterogeneous systems with multiple clock domains. We quantify the impact of multiple clock domains, such as topologies, operating frequencies, and granularities on reliability and robustness of 3-D PDNs. In addition, we outline a comprehensive review of various design guidelines for exploring the design knobs (i.e., power track sizing, TSV sizing and placement, decoupling capacitance insertion, workload assignment, and stacking order) to obtain reliable 3-D PDNs with multiple clock domains.

A. Contributions of This Paper

Despite these efforts, research on resiliency of 3-D PDNs is still in early stages. While the aforementioned works have started to investigate the reliability issues of 3-D PDNs, the impact of multiple clock domains on power and thermal integrity of 3-D PDNs remains to be inspected. The contributions of this paper are summarized as follows.

1) We provide a summary of guidelines for electrothermal modeling and simulation of 3-D PDNs with multiple clock domains.
2) We perform in-depth electrical and thermal analysis to understand the voltage droop and temperature distribution in 3-D ICs with multiple clock domains.
3) We investigate different clock domain frequencies and quantify their impact on power supply noise and temperature distribution on 3-D PDNs.
4) We identify potential power and thermal integrity issues by inspecting workload assignment and stacking order.
5) We evaluate possible design knob solutions, such as insertion of decoupling capacitances, TSV sizing and placement, and core placement for achieving reliable 3-D PDNs.
6) We perform several case studies and draw practical design guidelines that can be specially important during the design phase of 3-D PDNs to mitigate some of the excessive heat and voltage droop introduced by multiple clock domains.

The rest of this paper is organized as follows. Section II covers the related and recent works. Section III explains the preliminaries and the models utilized in this paper. Section IV provides the analyses of 3-D PDNs with multiple clock domains. In Section V, we provide our experimental results and case studies. Section VI presents a summary of practical design guidelines for reliable 3-D PDNs with multiple clock domains. Section VII concludes this paper.

II. Related Works

Investigations on 3-D stacked systems have attracted a lot of attention in the recent years from both academia and industry. There exists a rich body of research papers that are relevant for this paper and can be mainly grouped into two categories, such as papers focused on the design of 3-D clock networks and 3-D PDNs.

On the design of 3-D clock networks, several topological approaches have been investigated, such as clock trees, meshes, and hybrids. Zhao *et al.* [9], [10] proposed a 3-D clock tree synthesis algorithm for low-power and reliable clock networks while taking into account the TSV count and clock buffer insertion. Recently, Bang *et al.* [11] proposed a novel clock tree synthesis and synchronization scheme based on the concept of clustered clocking for 3-D ICs. A 3-D TSV fault-tolerant clock tree synthesis method was

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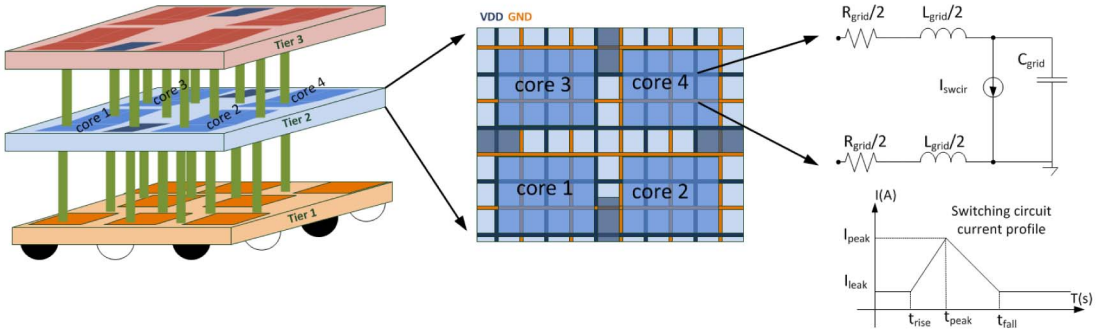

Fig. 2. Illustration of PDN and ground delivery network for a three-tier system.

presented in [12] while minimizes the number of clock TSVs. Kim and Kim [13] proposed a 3-D clock tree embedding algorithm for 3-D ICs with zero clock skew routing constraint. Thermal effects were included when modeling the 3-D clock tree and the design of adaptive clock buffers was proposed for designing thermally robust clock trees in [14]. Savidis *et al.* [15] investigated various clock distribution topologies and developed models to accurately determine the clock delay. Lung *et al.* [16] investigated the TSV fault-tolerant clock network design. A comparison of various different 3-D clock topologies, such as H-trees and with the combination of local and global meshes, is provided in [17]. In this paper, we will exploit and utilize these developments to explore the impact of different 3-D clock topologies on the reliability of 3-D PDNs.

On the design of 3-D PDNs, several groups of papers can be identified. On the first group, the impact of the 3-D integration technology on PDNs is investigated. In [18], 3-D PDNs are modeled and analyzed by inspecting the TSV array model. Moreover, He *et al.* [19] investigated the impacts of TSV dimensions and placement on 3-D PDNs. More analyses were performed in [20] on different TSV densities and aspect ratios and their impact on 3-D PDNs.

On the second group, various topological approaches were investigated for reliable 3-D PDNs. Healy and Lim [21] proposed a novel topology for 3-D PDNs while taking into account TSV placement and package parasitics. Khan *et al.* [22] explored different 3-D PDN topologies. Pavlidis and De Micheli [23] investigated different power distribution and return paths that impact the overall voltage droop on 3-D PDNs. Floorplanning and optimization of PDN and ground delivery network are explored in [24].

On the third group, optimization methods and design knobs are explored for alleviating the excessive voltage droop. Todri *et al.* [25] and Todri-Sanial *et al.* [26] provide the electrothermal modeling and analysis of 3-D PDNs and explore the optimization of 3-D PDNs for electrothermal constraints. In [27]–[29], power supply noise issues are investigated and decoupling insertion is explored. Decoupling capacitance insertion for 3-D power grid optimization is explored in [30]. Planning and placement of power and ground TSVs were investigated in [31].

On retrospect, the issue of power supply noise due to multiple clock domains is also critical to 2-D systems. There are several works that have looked into this problem and have investigated the timing issues introduced and presented power grid optimization methods, such as in [32] and [33]. Power supply noise issues are also present on 3-D PDNs with multiple clock domains; however, new challenges arise due to vertical integration, stacking order, TSV sizing, placement, and overall number of TSVs. TSVs allow power delivery among many vertical tiers, but they also contribute to power supply noise transfer among cores and tiers. As the experiments demonstrate, mitigation of voltage droop on 3-D PDNs is not as straightforward as in 2-D systems, but it requires several design knobs to be applied simultaneously due to the lateral and vertical inherent noise distribution behavior in 3-D systems.

III. Preliminaries

For 2-D ICs, PDNs are usually structured as regular meshes with metal tracks running in perpendicular to each other. Other works have explored the nonregularity of power meshes for reducing voltage droop [34]. Regardless of their structure, PDNs are designed to deliver voltage reliably, such that the underlying circuits can function properly. Any deviation from the supply voltage can impede optimal performance of devices and consequently leading to circuit delay and throughput reduction.

In this paper, we investigate power supply noise and temperature distribution on a three-tier PDN with various clock domains. An illustration of the 3-D system is shown in Fig. 2. In this paper, we include parasitics of package C4 bumps, global PDN, TSVs, switching circuits, decoupling capacitance, and heat sink. Our analyses are based on the *RLC* model representation of the power grid, package, and switching circuits. We utilize the existing physical models for studying power supply noise on 3-D power grids and further enhance them to include the thermal effects [32], [35]–[37].

The granularity of the switching circuits can be represented at die-, core-, block-, gate- or transistor-level. In this paper, as we are interested in exploring multiple clock domains, we utilize core-level modeling, where the core is operating at certain frequency range, which represents its clock domain. There is a lot of work dedicated to the optimal design of clock networks [9], [10], [13]–[17], and this is also a challenging topic for 3-D ICs. In this paper, we do not focus on the structure or the design of clock domains, but make

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the assumption that each core has already an optimal clock network, which allows it to operate at a certain frequency.

A. Package Model

On-chip supply voltage is delivered through the package balls to the global PDN of tier next to the package. In this paper, controlled collapse chip connection (C4) bumps are used for the package, which are an industry standard for the flip-chip technology [38]. The bump sizes are of 100 μm width and 200 μm pitch and its RL parasitics are extracted as 10 mΩ and 60 pH [38]. We assume an array of C4 bumps where half are used for supplying power (V_{DD}) and ground (GND), respectively.

B. TSV Model

In this paper, we study high-density TSVs with dimensions as 15 μm length, 3 μm diameter, and 60 μm pitch [39]. Please note that such TSV dimensions are simply used as case studies, and our analysis is general enough to handle TSVs with different geometries. TSV RLC parasitics have been extracted as $R_{\mathrm{tsv}} = 100$ mΩ, $L_{\mathrm{tsv}} = 10$ pH, and $C_{\mathrm{tsv}} = 40$ fF [39]. In this paper, we assume that TSVs are inserted in an array and uniformly distributed. TSVs can serve for both signaling and power/ground connections. As this paper is focused on the analysis of PDNs, we only consider TSVs for power and ground connections, where half of TSVs are used for power and ground, respectively.

C. PDN Model

RLC models for 3-D PDNs have been presented in [27], as regular mesh networks for each tier that are connected together using TSVs. In this paper, we assume that the power grids are uniform, meaning that each power track has a uniform width throughout its length, whereas the width of each track can vary, as shown in Figs. 1 and 2. In addition, we consider that the topology of PDN on each tier can vary due to the heterogeneous die stacking. RLC parasitics, R_{grid}, L_{grid}, and C_{grid} of each power track can be extracted based on its dimension. Furthermore, we investigate the power grids that are shared among all cores on the same die even though each core would have its own clock domain. From power supply noise analysis perspective, it is of interest to study the shared PDNs among the cores for investigating the noise transfer between them. In this paper, we consider the power tracks of 1000 μm length and 10–30 μm widths.

D. Switching Circuit Model

Each working core or functional block can represent the circuits of different functionalities, power demands, and operating frequencies. From the power grid analysis perspective, these switching circuits draw current from the power grid and are commonly modeled as switching current sources with specific parameters to represent the characteristics of the underlying circuits [18], [21]–[25], [27]. Switching circuits are commonly modeled as the triangular current sources to represent peak current, leakage current, peak time, rise time, and fall time as I_{peak}, I_{leak}, t_{peak}, t_{rise}, and t_{fall}. To represent multiple clock domains, the operating frequencies of the functional blocks are varied such as to represent various switching clock frequencies. Time period of a switching clock for a block i can be represented as $t_{\mathrm{period}_i} = 2(t_{\mathrm{rise}_i} + t_{\mathrm{fall}_i})$ and clock frequency as $\mathrm{freq}_i = 1/t_{\mathrm{period}_i}$. The switching source current and its frequency are based on previous work for the PDN analysis [40].

E. Decoupling Capacitance

Nonswitching circuits also provide some of the intrinsic decoupling capacitance to sustain the voltage fluctuations of the power supply. In this paper, we consider the intrinsic decoupling capacitance and the intentionally inserted decoupling capacitance as of 5 fF/μm^2. On-chip decoupling capacitors can be implemented in ICs in a number of ways. Typically, MIM capacitors are utilized and their capacitance density between 1 and 10 fF/μm^2 is reported [41]. Please note that this model is flexible enough to represent various amounts of inserted decoupling capacitances within each tier.

F. Thermal Model

Heat is generated from switching circuits and gets dispersed primarily through conduction and convection and to a lesser degree by radiation. Frequent switching circuits consume dynamic power, which consequently generates heat, and worsen the voltage droop. Simultaneous switching circuits on a tier and neighboring tiers lead to nonuniform power and heat distributions. Parasitics of power and ground networks may vary due to nonuniform thermal distribution, as resistivity is a function of temperature. Thus, at nodes with high temperature, voltage droop worsens. In addition, a large amount of currents flowing through power and ground networks elevate temperature even more, which over long periods of time can cause Joule heating and/or electromigration [42], [43]. Hence, voltage droop and thermal distributions are correlated and we consider them simultaneously.

We perform simultaneous electrical and thermal analyses to determine the voltage droop and temperature distribution on each tier. To do so, a thermal model of the three-tier system is built, where the principle of electrical–thermal duality is exploited. Duality is based on the equivalence of electrical current through an electrical resistor to heat flow through a thermal resistor and voltage difference equivalence to temperature difference. Thermal resistance models obtained from [25], [36], [37], and [43] are applied to represent PDNs, TSVs, and C4s. Heat generated from switching circuits is modeled by current sources to represent their power consumption. Temperature at heat sink is assumed 27 °C. A thermal analysis is based on 1-D static analysis, and combined with electrical analysis, we recompute voltage droop on each tier. In Table I, we list the parameter values of the models used in this paper.

IV. Analysis of 3-D Power Delivery Network With Multiple Clock Domains

Here, we summarize the electrothermal analyses technique that is utilized for computing voltage droop and temperature

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TABLE I
DETAILED SUMMARY OF THE PARAMETER VALUES USED IN THIS PAPER

Element	Geometries	Parasitic
Power Grid Mesh	1mm by 1mm	
Package C4 bumps	100μm width, 200μm pitch	$R = 10m\Omega$, $L = 60pH$
TSV	3μm diameter, 15μm length, 60μm pitch	$R_{tsv} = 100m\Omega$, $L_{tsv} = 10pH$, $C_{tsv} = 40fF$
Power grid track	1000μm length, 10μm to 30μm width	$R_{grid} = 45m\Omega$, $L_{grid} = 3.5pH$
Inserted decoupling capacitance		$5fF/\mu m^2$
V_{DD}		1V
Power Density	High	$3\mu W/\mu m^2$
	Mid	$1.5\mu W/\mu m^2$
	Low	$0.7\mu W/\mu m^2$

on each tier of 3-D PDNs. In addition, we apply the presented analytical method on a sample circuit to illustrate the electrothermal analysis of 3-D PDNs with multiple clock domains.

A. Electrical Analysis

To perform multiple clock domain power grid analysis [32], we first describe how power grid node voltages are mathematically computed applying a modified nodal analysis (MNA). Current flow on power grid branches and node voltages on power grid intersections respect the Kirchhoffs current and voltage rules, i.e., KCL and KVL. Thus, the equations of each node voltage can be devised in matrices as

$$V = AU = G^{-1}U \tag{1}$$

where G is the modified conductance matrix of the power grid, U is the vector of current sources, and V is the vector of node voltages. A node voltage, v_i can be expressed as

$$v_i = \sum_{j=1}^{n} a_{ij}\, g_{ij}\, V_{\mathrm{DD}} - \sum_{k=1}^{n} a_{ik}\, I_k \tag{2}$$

where n is the number of voltage nodes on the PDN, $g_{ij}\,V_{\mathrm{DD}}$ is the conductance term, where j is the neighboring node to node i, I_k is the current source at node k, and a_{ij} and a_{ik} are the elements of matrix A.

Please note that node voltage v_i can represent both power and ground node voltages. Solving for node equations (2) would rely on computing inverse matrix, which can be computationally expensive. There are several efficient and accurate linear algebra-based methods for the MNA analysis. Discussion of MNA solvers is not the scope of this paper and perusal on these methods is left to the reader [44], [45].

Based on the node voltages, one can easily compute the final node voltage using the superposition principle. The superposition applies to linear networks, where the response of each frequency is combined together as

$$V_i = V_i^{\mathrm{freq}_1} + V_i^{\mathrm{freq}_2} + \cdots + V_i^{\mathrm{freq}_m} + V_o = \sum_{r=1}^{m} V_i^{\mathrm{freq}_r} + V_o \tag{3}$$

where $V_i^{\mathrm{freq}_m}$ is the node voltage for each frequency domain, m is the number of different clock frequency domains, and V_o is the initial conditions node voltage. Based on the node voltages for each frequency, the amount of power supply noise can be derived by computing the voltage droop during a given time period as [40]

$$\mathrm{PSN}_i^{\mathrm{freq}_j} = \int_{\mathrm{ts}}^{\mathrm{te}} \left(V_{\mathrm{DD}} - V_i^{\mathrm{freq}_j}\right) dt \tag{4}$$

where ts and te are starting and end time for computing the amount of voltage droop, which can be user specific, i.e., being and end time of a single clock cycle or several cycles. Similarly, the total amount of power supply noise induced from different clock domains can be computed as

$$\mathrm{PSN}_i = \sum_{j=1}^{m} \mathrm{PSN}_i^{\mathrm{freq}_j} + \mathrm{PSN}_i^{o} \tag{5}$$

where PSN_i^{o} is the initial condition of power supply noise. Here, we also introduce the notion of self-noise and transferred noise.

Definition: Self-noise is the amount of noise that a block i with clock frequency, freq_k introduces on itself as

$$\mathrm{PSN}_i^{\mathrm{self}} = \mathrm{PSN}_i^{\mathrm{freq}_k} + \mathrm{PSN}_i^{o}. \tag{6}$$

Definition: Transferred noise is the amount of noise that block i experiences from other switching blocks with different clock frequencies (different from freq_k) as

$$\mathrm{PSN}_i^{\mathrm{transferred}} = \sum_{r=1, r\neq k}^{m} \mathrm{PSN}_i^{\mathrm{freq}_r}. \tag{7}$$

B. Thermal Analysis

Similarly, temperature distribution on 3-D PDNs can be computed by applying superposition principle. There are several works that discuss in-depth PDN thermal modeling [25], [32], [36], [37]. In this paper, we utilize these models to perform simultaneous electrical and thermal analysis of 3-D PDNs. By exploiting the principle of electrothermal duality, 3-D PDN thermal networks can be devised as electrical networks and accurately solved for node temperatures similarly as node voltages. Based on 1-D treatment of temperature distribution, temperature on PDN segments can be derived as

$$T = G_{\mathrm{th}}^{-1}\, Q_{\mathrm{th}} = H_{\mathrm{th}}\, Q_{\mathrm{th}} \tag{8}$$

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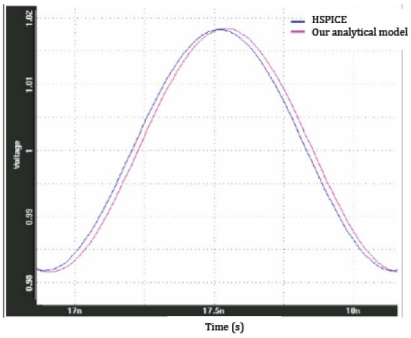

Fig. 3. Comparison of HSPICE and our model voltage transient response on a power network node.

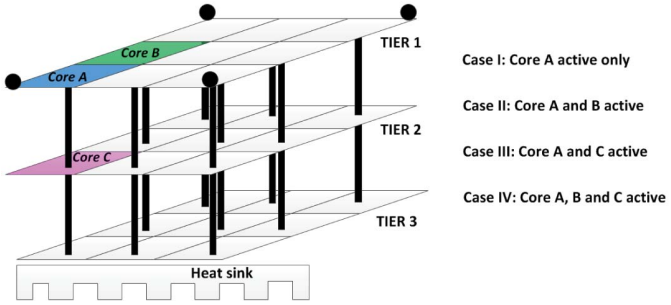

Fig. 4. Illustration of sample circuit.

where G_{th}^{-1} is thermal impedance matrix and Q_{th} is the heat source vector based on derived power consumption from electrical network. Node temperature can be expressed as

$$t_i = \sum_{j=1}^{n} h_{\text{th}_{ij}} q_{\text{th}_j}. \tag{9}$$

Overall, node temperature due to multiple clock domains can be derived as

$$T_i = \sum_{j=1}^{m} T_i^{\text{freq}_j} + T_i^o \tag{10}$$

where T_i^o is the initial temperature. Accuracy of the mathematical formulations for power supply noise and temperature is compared with HSPICE simulations. Fig. 3 shows the comparison of the voltage response at a node on the power grid with respect to our analytical model, and the results show up to 92% accuracy of the proposed method for deriving power supply noise distribution on 3-D PDNs with multiple clock domains. Moreover, experiments indicate that excessive noise and temperatures can be induced due to various clock frequencies. For example, some results are shown for a sample circuit in Section IV-C. Overall, such analyses motivate deeper investigations into the optimal design of 3-D PDNs with multiple clock domains.

C. Sample Circuit Analysis

Here, we provide a sample circuit where we perform all the mathematical aforementioned steps in order to illustrate the analysis flow. Fig. 4 shows an illustration of the sample three-tier multicore system that we utilize for this paper. All cores are identical; however, their switching frequencies vary. For this sample circuit, we set the switching frequencies as 500, 750, and 600 MHz for cores A, B, and C, respectively. Please note that these are simply taken as the case studies to show the analysis flow. We consider four different working cases. In case I, only core A is active and we can compute the power supply noise that only core A generates or its self-induced noise. In case II, both cores A and B are active and here we can compute the amount of noise that working core B transfers to core A, thus transferred noise. Similarly, in case III, cores A and C are active and we can derive the amount of noise that is transferred through the TSVs from core C to core A. In last case IV, all cores A, B, and C are active, and we derive the total amount of noise on core A due to neighboring cores B and C. We also derive the worst case temperature distributions on each tier for each case in order to understand the impact of working neighboring cores and TSVs.

In Fig. 5, we show both the worst case power supply noise (i.e., maximum dc voltage droop) and temperature (i.e., highest temperature based on the largest dc voltage droop) distributions for all cases. The worst case supply noise map is shown for each tier for each case to visualize the evolution of noise between tiers. We notice that for case I, the worst case noise peaks at core A as

$$\text{PSN}_A^{\text{self}} = \text{PSN}_A^{\text{freq}_A} + \text{PSN}_A^o = 167 \times 10^{-12}\ \text{V} \cdot \text{s} \tag{11}$$

where Vs is the unit for supply noise in voltage per seconds. In case II, we derive the worst case noise at core A as

$$\begin{aligned} \text{PSN}_A^{\text{caseII}} &= \text{PSN}_A^{\text{freq}_A} + \text{PSN}_A^{\text{freq}_B} + \text{PSN}_A^o \\ &= 230 \times 10^{-12}\ \text{V} \cdot \text{s} \end{aligned} \tag{12}$$

where the transferred noise can be derived as

$$\begin{aligned} \text{PSN}_A^{\text{caseII}} - \text{PSN}_A^{\text{self}} &= (230 - 167) \times 10^{-12} \\ &= 63 \times 10^{-12}\ \text{V} \cdot \text{s} \end{aligned} \tag{13}$$

which represent the additional amount of supply noise induced by working neighbor core B on core A. In case III, cores A and C are active and the supply noise at core A is derived as $\text{PSN}_A^{\text{caseIII}} = 261 \times 10^{-12} Vs$ and the transferred noise is derived as

$$\begin{aligned} \text{PSN}_A^{\text{caseIII}} - \text{PSN}_A^{\text{self}} &= (261 - 167) \times 10^{-12} \\ &= 94 \times 10^{-12}\ \text{V} \cdot \text{s} \end{aligned} \tag{14}$$

which is the additional amount of supply noise induced from core C to A through the TSVs. We notice that the amount of supply noise transferred from core C to A is larger than noise transferred from core B to A, which is due to the switching frequency difference between cores B and C. In case IV, the total amount of noise when all cores A, B, and C are active is derived as $\text{PSN}_A^{\text{caseIV}} = 272 \times 10^{-12}$ V · s, and the total amount of noise transferred is derived as

$$\begin{aligned} \text{PSN}_A^{\text{caseIV}} - \text{PSN}_A^{\text{self}} &= (272 - 167) \times 10^{-12} \\ &= 105 \times 10^{-12}\ \text{V} \cdot \text{s} \end{aligned} \tag{15}$$

which is the additional supply noise induced by cores B and C. We note that the total amount of noise from cores B and C

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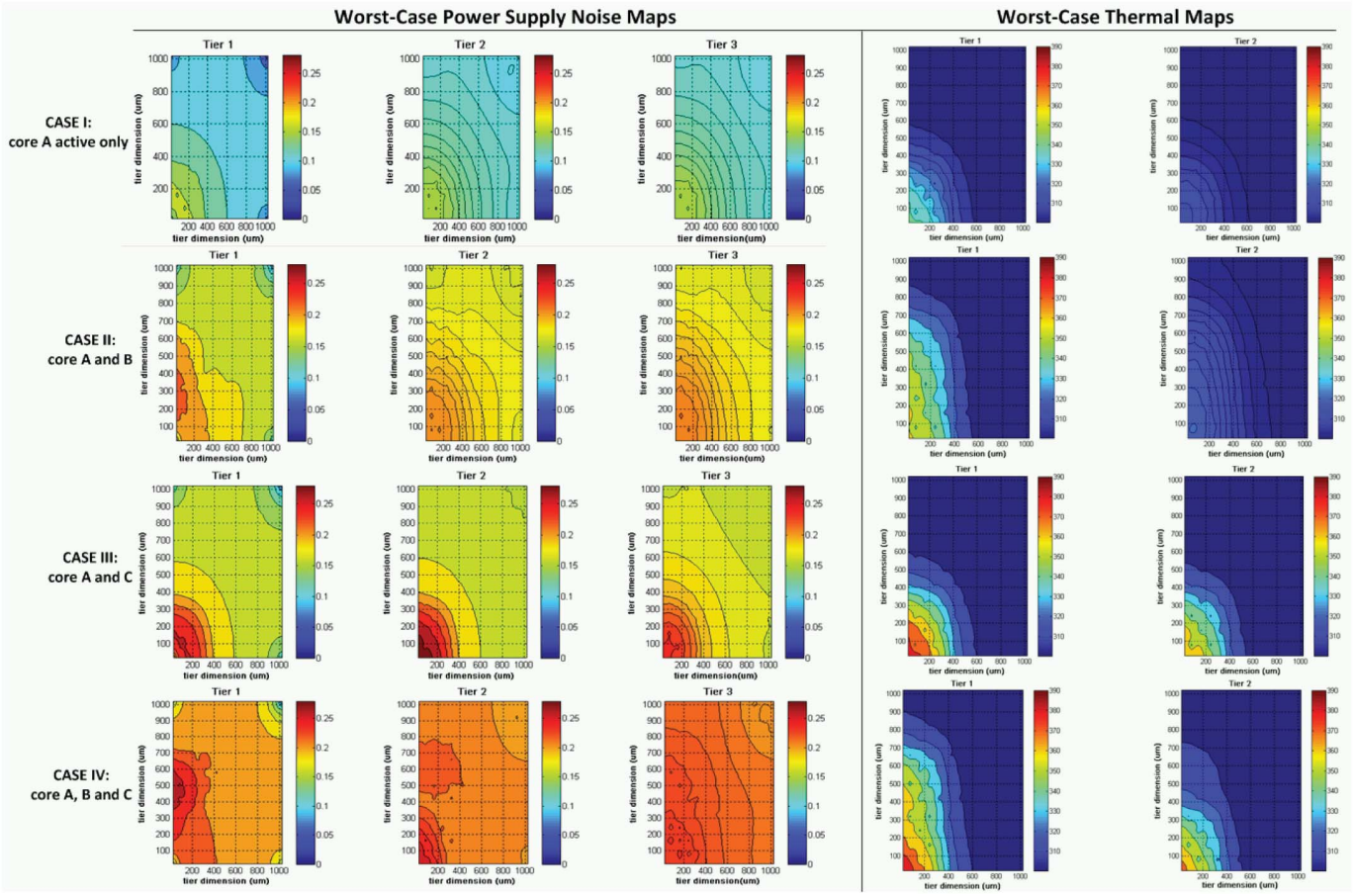

Fig. 5. Power supply noise and temperature distribution for all cases on all tiers. We note that there is a strong relation between worst case voltage droop and temperature maps.

is not accumulative of their individual supply noise. This is due to the amount of decoupling capacitance available in the system to sustain some of the supply noise when several cores are active. Previous works notably [46], [47] have shown that decoupling capacitors located in close distance (or effective distance) to switching circuits are helpful in suppressing power supply noise. The effective distance in our test case is the Manhattan distance from core to core. Thus, for each case, the amount of effective decoupling capacitance varies depending on the location of the switching core and the idle cores around it that can serve as decoupling capacitance. Fig. 6 shows the amount of voltage droop derived on each tier for each case.

Temperature distributions for each tier and for each case are shown in Fig. 5 (right-hand side). Only tiers 1 and 2 are shown as the temperature on tier 3 does not vary significantly from the heat sink temperature (∼300 K). In case I, a worst case temperature of 341 K was obtained, where only core A is active. In case II, we derive a worst case temperature of 372 K in tier 1, and we note a temperature increase by 372 K − 341 K = 31 K on core A due to the impact of working neighbor core B. Similarly, in case III, a temperature increase on core A is observed as 382 K, where the temperature impact of core C on A is derived as 382 K − 341 K = 41 K. Such impact also demonstrates the thermal distribution through the TSVs from one tier to the next. When all three cores are

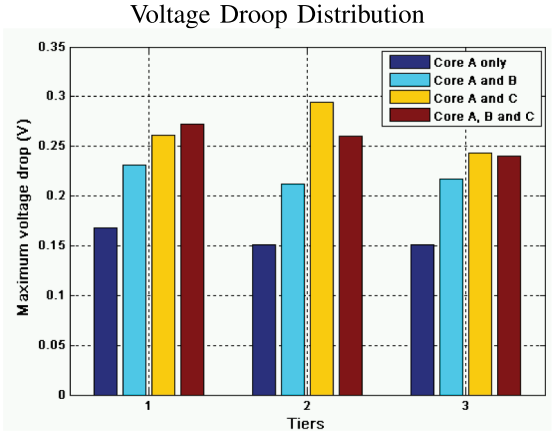

Fig. 6. Power supply noise distribution for all cases and each tier.

active, the temperature increase on core A reaches 384 K, and the overall impact of cores B and C on core A is as 384 K − 341 K = 43 K, which is less than the total impact of individual cores of 72 K (i.e., where effect of core B on A is 31 K and core C on A is 41 K, a total of 72 K).

Fig. 7 shows the maximum temperature distributions on each tier for each case. Overall, we notice that the highest temperatures occur on tier 1, which is due to the activity

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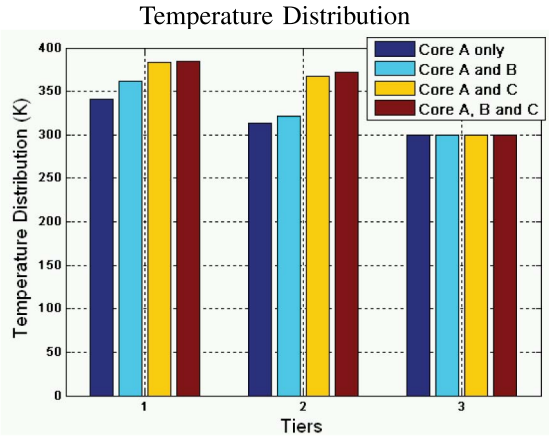

Fig. 7. Temperature distribution for all cases and each tier. Note that Tier 3 is next to heat sink and benefits from immediate cooling.

of cores A and B. In addition, we note that in tier 1, the largest temperature is obtained for case IV when all cores are active and some of the heat is transferred through the TSVs. Such observation reveals that the TSVs have an important role on overall thermal distribution and we will investigate how their sizing and placement can further impact voltage droop and temperature.

V. Experiments

To perform a meaningful electrothermal analysis, if every individual switching device is represented, a system model containing a 3-D PDN can easily reach a complication level that is hard to be implemented and simulated. For this reason, we devise several exhaustive 3-D power delivery benchmarks with many switching cores and various stacking orders. The objective is to have a wide representation of 3-D power delivery benchmarks with multiple cores that can be meaningful for voltage droop and temperature analysis purposes. We devise benchmarks with a three-tier system, where each tier has nine cores. Tier 1 (T1) is the closest to the package bumps, whereas tier 3 (T3) is next to heat sink and benefits from immediate cooling. From a wide range of operating frequencies, we select three frequency ranges to represent low (i.e., $L = 500$ MHz, frequency <1 GHz), mid (i.e., $M = 1$ GHz), and high (i.e., $H = 3$ GHz) clock frequencies. The total number of TSVs is 288, where 16 TSVs are used for each core for power and ground, respectively. We apply various clock frequencies and investigate the voltage droop and temperature on the 3-D PDN. In Sections V-A–V-E, we perform the following experiments.

A. Impact of Identical Dies With Single Clock Domain

For this study, we apply the same clock frequency to all the tiers and their cores. We study three setups (i.e., $s1$, $s2$, and $s3$). In setup $s1$, all the cores operate in low-frequency clock domain (L), in setup $s2$, all the cores operate in mid clock frequency (M), and in setup $s3$, all the cores operate in high clock frequency (H), as shown in Fig. 8. For each setup, we compute the worst case power supply noise (voltage droop on power and ground tracks) and temperature on each tier, as listed in Table II.

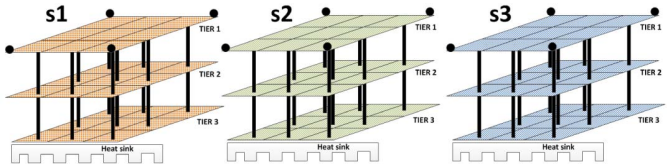

Fig. 8. Experimental setup for $s1$, $s2$, and $s3$.

TABLE II
Worst Case Voltage Droop and Temperature With Single Clock Domain on Identical Tiers

Setup	Voltg. Droop (mV)			Temp. (^{o}C)		
	T1	T2	T3	T1	T2	T3
s1	74.52	95.50	98.53	73.5	75.80	32.00
s2	75.18	97.42	101.30	73.90	76.60	32.20
s3	78.05	108.58	119.03	76.40	81.60	33.10

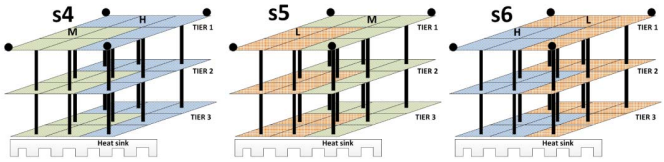

Fig. 9. Experimental setup for $s4$, $s5$, and $s6$.

We note that in general, the worst voltage droop is measured on tier 3 (furthest from package), and worst temperature is measured on tier 2 (middle of stack). We also note that high-frequency clock domain (setup $s3$) introduces the most voltage droop and temperature rise. This is due to increased inductive parasitic impedance ($j\omega L$) with frequency increase and reduced effectiveness of decoupling capacitances, as they cannot be recharged in time before the next transition. Tier 2 located in the middle of the stack suffers from heat dissipation from both the top and bottom tiers; hence, it experiences the highest temperature.

Such results are interesting as they indicate that a system can satisfy the power and thermal constraints when it is running applications or task below a given frequency (i.e., 1 GHz); however, it can suffer from larger voltage droop and temperature when its cores run applications or tasks operating at a higher frequency (i.e., 3 GHz). Hence, the characteristics of applications to run on a 3-D multicore system should be carefully analyzed, such that no critical power and thermal integrity issues are introduced.

B. Impact of Identical Dies With Multiple Clock Domains

To investigate the impact of multiple clock domains, we devise three setups $s4$, $s5$, and $s6$. For the sake of clarity, we choose these three cases; however, more cases can be envisioned. Each setup is shown in Fig. 9, where setup $s4$ has operating cores with M and H clock domains, setup $s5$ has cores with L and M clock domains, and setup $s6$ has cores with H and L clock domains, respectively.

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TABLE III
WORST CASE VOLTAGE DROOP AND TEMPERATURE WITH MULTIPLE CLOCK DOMAINS ON IDENTICAL TIERS

Setup	Voltg. Droop (mV)			Temp. (^{o}C)		
	T1	T2	T3	T1	T2	T3
s4	62.35	87.63	97.02	63.00	68.00	32.00
s5	60.08	77.70	80.90	60.20	62.70	31.10
s6	72.76	95.68	101.50	71.64	74.48	32.20

We note that the assignment of clock domains on each tiers result into different voltage droop and temperatures. The results are listed in Table III. The worst voltage droop and the temperature are measured on setup $s6$, where there is up to 10 mV and 12 °C difference from setup $s4$. The voltage droop is worse on $s6$ than $s4$ mainly due to the chip-package resonance frequency effect. The resonance is computed as in [48] with formula $f = 1/(2\pi(L_{\text{pkg}}C_{\text{decap}})^{1/2})$ and derived as 290 MHz, which is close to the L low-frequency workload of 500 MHz. When the switching frequency of the circuit is close to the chip-package resonance frequency, it causes additional voltage fluctuations on the supply voltage, which further detriments voltage droop. The inductance of the package and on-chip decoupling capacitance creates an LC tank effect, which worsens voltage droop for $s6$ compared with $s4$. To avoid resonance frequency issues, designer should be careful on the choice of package and amount of inserted decoupling capacitance. Previous works [41] have shown that inserting too much decoupling capacitance lowers the resonance frequency, which worsens on-chip power supply noise.

Such results indicate the importance of stacking order for identical dies with different clock domains. In addition, results demonstrate that the stacking of identical dies might not necessarily be of interest for the operating cores (i.e., applications running on cores) with frequencies above 1-GHz range. For example, in case $s6$, 3-D PDNs can experience a large amount of voltage droop and high temperatures, which can cause further performance degradation to the underlying cores.

C. Impact of Heterogeneous Dies With Multiple Clock Domains

In this scenario, we study the impact of heterogeneous dies with different clock domains and we devise three setups $s7$, $s8$, and $s9$. We assume that each tier can have cores operating with clock domains as: 1) low-mid (LM); 2) mid-high (MH); and 3) high-low (HL), as shown in Fig. 10. Please note that more clock domain combinations can be derived. The results for each setup are listed in Table IV.

Results indicate that setup $s7$ has the worst voltage droop and temperature on tier 3 with clock domains HL. We note that when clock domains HL are inserted on tier 1 as in setup $s9$ (or tier 2 as in setup $s8$), up to 12 mV and 6 °C less voltage droop and temperature are observed. This reveals the importance of workload assignment and stacking order of dies. While, overall, the same type of workloads is applied to all three setups, only their stacking order varies. We observe up to 5% and 7.5% difference in worst case voltage droop and temperature, respectively, due to stacking order difference. Such variations on voltage droop and temperature could be critical on the performance and reliability of 3-D multicore systems, where the voltage droop margins are already very tight. Such results further motivate investigation on workload assignment while taking into account stacking order and core's operating frequencies.

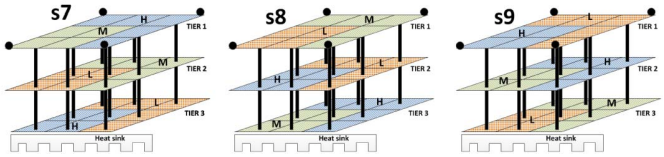

Fig. 10. Experimental setup for $s7$, $s8$, and $s9$.

TABLE IV
WORST CASE VOLTAGE DROOP AND TEMPERATURE WITH MULTIPLE CLOCK DOMAINS ON HETEROGENOUS TIERS

Setup	Voltg. Droop (mV)			Temp. (^{o}C)		
	T1	T2	T3	T1	T2	T3
s7	72.78	95.70	101.52	71.65	74.50	32.20
s8	62.35	87.64	97.02	62.90	67.95	31.90
s9	65.57	85.80	89.70	66.10	68.86	31.60

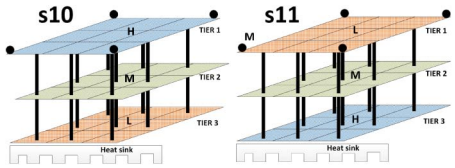

Fig. 11. Experimental setup for $s10$ and $s11$.

TABLE V
WORST CASE VOLTAGE DROOP AND TEMPERATURE WITH MULTIPLE CLOCK DOMAINS ON HETEROGENOUS TIERS

Setup	Voltg. Droop (mV)			Temp. (^{o}C)		
	T1	T2	T3	T1	T2	T3
s10	120.07	121.06	122.12	65.42	61.87	56.12
s11	126.10	122.62	123.68	68.26	62.51	55.07

In practical cases, each tier would have a single clock domain that could vary from tier to tier. We also investigate the scenarios where heterogeneous dies are stacked together and each die has a single clock domain. We investigate experimental setup $s10$, where workloads with clock frequencies H is in tier 1, M in tier 2, and L in tier 3. Both setups are shown in Fig. 11. Setup $s11$ has workloads with clock frequency L on tier 1, M on tier 2, and H on tier 3. Please note that more setups can be envisioned. We aim to capture the dependence of workload frequency and stacking order for heterogeneous dies with a single clock domain.

We observe that voltage droop values are higher up to 4.7% for T1 in benchmark $s11$ than in $s10$, as shown in Table V. The main difference between these two benchmarks is the stacking order of workloads H and L. We observe that allocating top tier (T1) for high-frequency workloads gives slightly less voltage droop and temperature increase. Workloads on tier T1 benefit from package closeness, hence less voltage droop,

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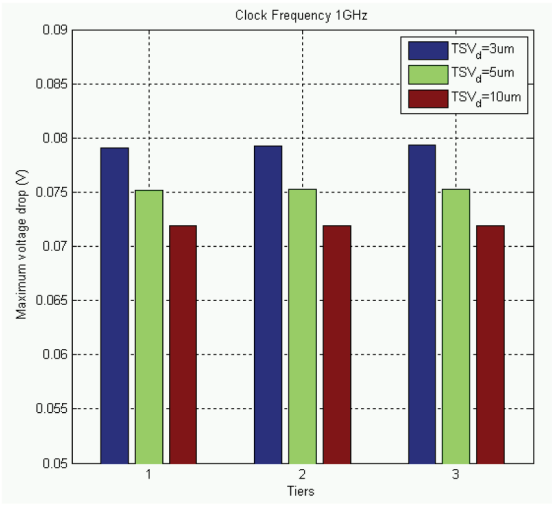
whereas allocating workloads with low frequency on the bottom tier (T3) weakens chip-package resonance effects due to the longer distance from package to low-frequency switching cores and also benefits from immediate cooling of heat sink. On benchmark $s11$, locating high-frequency workloads on T3 helps to mitigate elevated temperatures, however, it worsens its voltage droop. Thus, benchmark $s10$ provides overall less voltage droop, and it has higher temperature on T3 than in $s11$ due to H workload located next to heat sink. Tier T1 on $s11$ has more voltage droop due to resonance effect, which ultimately the additional switching due to resonance increase power consumption and results in higher temperature than T1 in $s10$. This experiment highlights the importance of stacking order and clock domain frequency and points out that to faster switching cores due to their large current demand is better to locate them on the tier next to the package. Such observations also reveal the complexity of the problem for workload assignment as voltage droop and temperature increase in the opposite directions on the 3-D stack.

D. Impact of TSV Sizing

Here, we investigate the impact of TSV sizing on power supply noise and temperature distribution. We use three different types of TSV dimensions. We investigate TSVs with diameter 3, 5, and 10 μm. As we are investigating global interconnects for power and ground delivery, we utilize the TSV parameters from ITRS 2013 [49] on global interconnects based on 3-D-stacked ICs/3-D-SoC roadmap. We evaluate the power supply noise for each type of TSV while applying the same switching activity and frequency to the 3-D system. We apply two different clock frequencies, 1 and 3 GHz, respectively. Please note that all cores on each tier are active and switching with the same clock frequency. As the goal is to capture the impact of TSV sizing, we perform two experiments, first when all cores are switching clock frequency 1 GHz and second with 3 GHz.

In Fig. 12(a), maximum voltage droop for each tier with clock frequency 1 GHz is shown. We note that with increasing TSV diameter, there is up to 6.25% effect on voltage droop for each tier. Increasing TSV diameter results in less resistance parasitic, whereas there is a sharp increase in TSV inductance and capacitance parasitics that overall impact its impedance; hence, we observe a small reduction on the voltage droop as TSV diameter increases. We observe a reduction of 6.25% in voltage droop with an increase of 3–5-μm TSV diameter, whereas only 4% decrease in voltage droop with increase of 5–10-μm TSV diameter. In Fig. 12(b), the maximum temperatures are shown for each tier. We observe almost the same temperature levels on each tier indicating TSV contribution to vertical heat transfer. Note that tier 3 has almost no temperature change (i.e., $\sim$300 K) as it is next to heat sink and benefits from immediate cooling. Results depict that lateral voltage droop is more dominant (i.e., less droop difference between tiers), whereas vertical heat transfer is more crucial (i.e., larger temperature difference between tiers) among tiers. We perform similar experiments when the switching clock frequency in the 3-D system is increased to 3 GHz. We observe that voltage droop worsens with the increase in clock frequency regardless of a TSV diameter size, whereas large diameter TSVs demonstrate to reduce up to 4% of the heat dissipation, as shown in Figs. 12(b) and 13(b).



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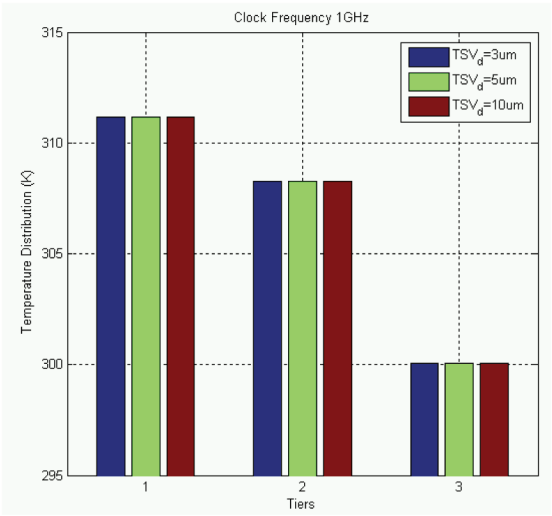

(b)

Fig. 12. Maximum voltage droop and temperature on each tier for different diameter TSVs for the clock frequency of 1 GHz. All cores are active on all tiers. Note that Tier 3 is next to heat sink and benefits from immediate cooling. (a) Maximum voltage droop on each tier. (b) Maximum temperature on each tier.

E. Impact of TSV Placement

Here, we investigate the impact of TSV placement on power supply noise and temperature distribution. We use three different types of TSV dimensions as in the previous experiment. In addition, we investigate uniform and clustered TSV placement. Uniformly distributed TSVs are homogeneously and consistently distributed among cores, where 16 TSVs (both power and ground) are used for each core, thus a total of 288 TSVs in the 3-D system, whereas clustered TSVs are grouped together and placed in the center of chip area while utilizing the same number of TSVs. Thus, the total number of TSVs (288) remains unchanged for both uniform and clustered test cases; however, their placement changes. The objective is

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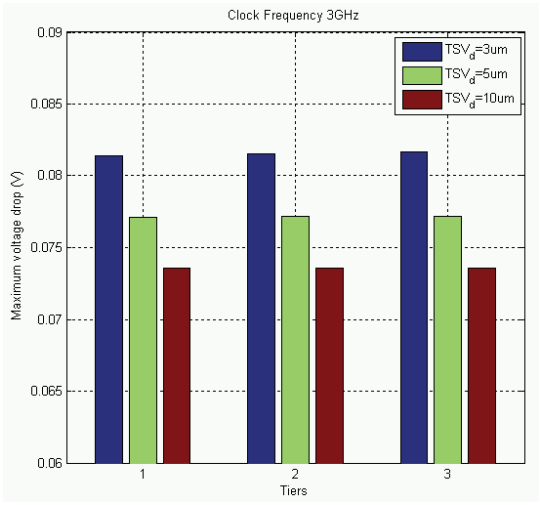
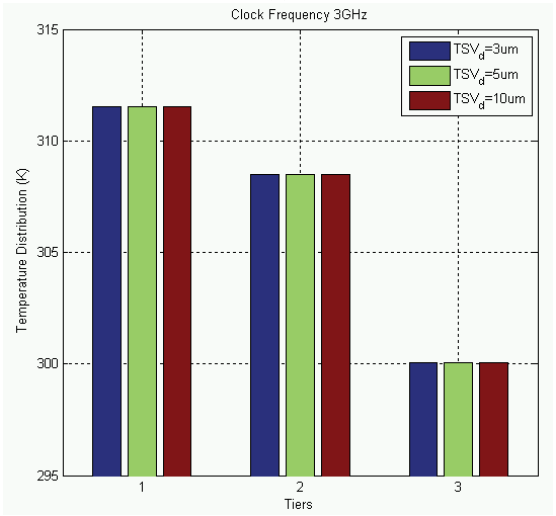
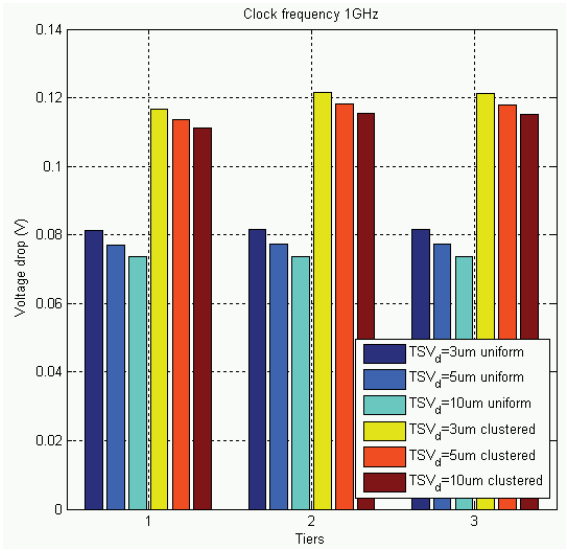


(a)



(b)

Fig. 13. Maximum voltage droop and temperature on each tier for different diameter TSVs for the clock frequency of 3 GHz. Note that Tier 3 is next to heat sink and benefits from immediate cooling. (a) Maximum voltage droop on each tier. (b) Maximum temperature on each tier.



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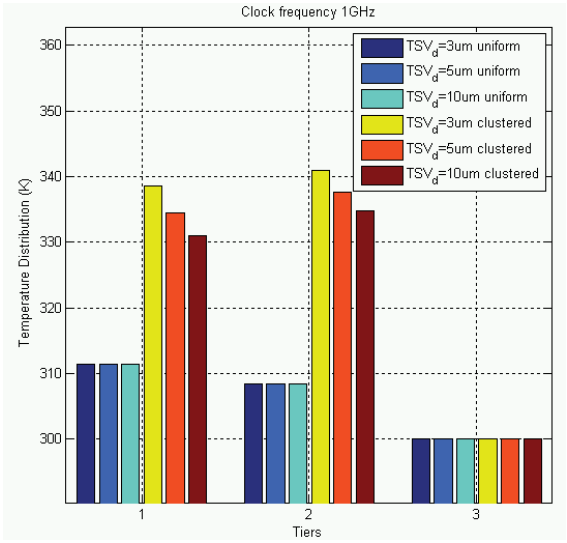

(b)

Fig. 14. Maximum voltage droop and temperature on each tier for different diameter TSVs for the clock frequency of 1 GHz. We investigate uniformly and clustered TSVs. Note that there is almost no temperature variation on Tier 3 as it is next to heat sink and benefits from immediate cooling. (a) Maximum voltage droop on each tier. (b) Maximum temperature on each tier.

to investigate TSV placement impact on worst case voltage droop and temperature.

Similar to the previous experiment, we evaluate the worst case power supply noise for each type of TSV while applying the same switching activity and frequency on the 3-D system, where all cores are active. We apply two different clock frequencies, 1 and 3 GHz, respectively, and compute the worst case voltage droop and temperature on each tier.

In Fig. 14(a), the maximum voltage droop distributions are given for each tier for both uniform and clustered TSV placements. We note that the clustered TSVs induce an overall increase in the voltage droop for each tier compared with uniformly distributed TSVs. Some of the voltage droop increase is lowered when TSV diameter increases. Results show that the distribution and the sizing of TSVs can have up to 32% effect on the worst case voltage droop even when the same number of TSVs is utilized.

In Fig. 14(b), the maximum temperature distribution on each tier is shown when both the uniform and clustered TSVs are used. Similarly, we note that the clustered TSVs elevate the temperature drastically than uniformly distributed TSVs up to 9.6%; however, there is some alleviated heat with the increase in TSV diameter. This is due to the thermal blockage effect that clustered TSV create between cores. This phenomenon was also observed in [50]. The local thermal build-up around the TSVs leads to increase lateral heat distribution, which consequently increase intratier voltage droop. We perform similar experiments when the switching clock frequency in the 3-D system is set to 3 GHz. We observed a similar trend for both voltage droop and temperature, as shown in Fig. 15(a) and (b).

Overall, these experiments demonstrate the criticality that multiple clock domains induce on voltage droop and temperature on 3-D PDNs. They further motivate dedicated analysis

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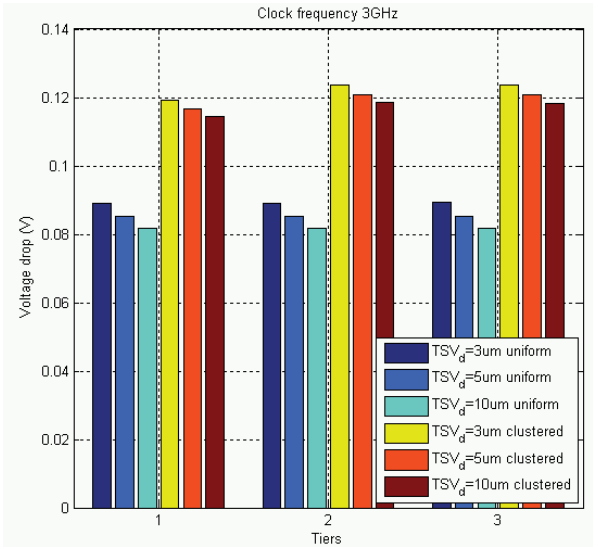
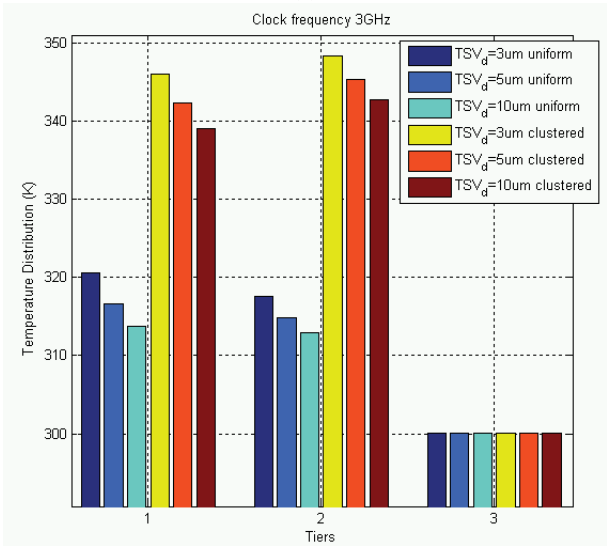


(a)



(b)

Fig. 15. Maximum voltage droop and temperature on each tier for different diameter TSVs for the clock frequency of 3 GHz. We investigate uniformly and clustered TSVs. Note that there is almost no temperature variation on Tier 3 as it is next to heat sink and benefits from immediate cooling. (a) Maximum voltage droop on each tier. (b) Maximum temperature on each tier.

and optimization methods for addressing power supply noise and excessive temperatures on 3-D PDNs due to multiple clock domains.

VI. Observations and Practical Design Guidelines

Based on the results obtained from the above experiments, we deduce several observations that can be utilized during the early design phase to ensure power and thermal integrity of 3-D PDNs with multiple clock domains.

We draw the following observations.

A. Observation 1: Clock Frequency and Supply Noise

Core frequency has a significant effect on the amount of supply noise induced. We observe that when the 2-D power delivery for a multicore system (i.e., a single tier with nine cores) is utilized to build a 3-D PDN, as shown in Fig. 8, it might no longer be optimal (i.e., voltage droop $\geq 10\% V_{DD}$). In other words, PDNs that were initially designed for a 2-D multicore system might not necessarily be optimal when reutilized for 3-D PDNs. For low-frequency switching cores (i.e., $\leq$1 GHz as in benchmark $s1$), simple reutilization of 2-D PDNs to 3-D PDNs might be sufficient. However, if the frequency of cores is higher than 1 GHz (i.e., as in benchmarks $s2$ and $s3$), then a redesign of 3-D PDN is needed to minimize the amount of voltage droop and high temperatures. Stacking of identical dies for more processing power can be exploited with minor design effort depending on the core operating frequencies.

B. Observation 2: Multiple Clock Domains and Supply Noise

Depending on the frequency of multiple clock domains, they can adversely affect supply noise. For example, when identical dies with cores operating with two different clock frequencies, *MH* and *LM*, such as benchmarks $s4$ and $s5$, then simple stacking of PDNs does not lead to excessive voltage droop or temperatures, whereas identical dies with cores operating with high-low *HL* clock frequencies (i.e., benchmark $s6$) would lead to exacerbated noise and temperature, requiring a redesign of 3-D PDNs. These results also show that the worst case noise would occur when high- and low-frequency cores are operating simultaneously. This observation can be important during the runtime application of multicore system in order to avoid excessive noise and heat, and parallel workload assignment of high and low frequencies can be avoided.

C. Observation 3: Multiple Clock Domains and Stacking Order

Benchmarks $s7$, $s8$, $s9$, $s10$, and $s11$ represent the same circuit but with different stacking orders of cores. We observe that clock domain frequency and stacking order have a significant effect on the amount of voltage droop and temperature on each tier. We note that minimal voltage droop is obtained when high-frequency switching cores are located next to the heat sink or in middle tier as in benchmark $s8$, whereas large voltage droop and temperatures are obtained when high-frequency switching cores are located next to the package or T1. This can also be explained by the effect of high-frequency switching noise due to coupling of decoupling capacitance with package inductance that creates an *LC* resonance effect at high frequencies, as observed in [41]. In addition, high-frequency cores also lead to excessive temperatures on T1, which is farthest from heat sink and further exacerbates voltage droop.

D. Observation 4: Multiple Clock Domains and Workload Assignment Order

Another angle to view the combined results from benchmarks sets ($s4$, $s5$, and $s6$) and ($s7$, $s8$, and $s9$) is the effect that workload frequency and assignment order have on 3-D PDNs voltage droop and temperature. From benchmarks $s4$, $s5$, and $s6$, we deduced that 3-D PDNs remain reliable as long as cores with *MH* and *LM* frequencies are

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operating simultaneously. From benchmarks $s7$, $s8$, and $s9$, we deduced that the location of switching cores plays a crucial role on reliability of 3-D PDNs. Overall, one can conclude that taking into account core switching frequency, location, and assignment order, excessive voltage droop and temperature issues can be mitigated. For example, for a given set of workloads to be executed, deciding to simultaneously operate *MH* or *LM* workloads and selecting cores next to heat sink for *HL* workloads can be crucial for alleviating power supply noise and thermal issues, or assigning middle tier or tier next to heat sink for high-frequency workloads can be an alternative to reducing noise.

E. Observation 5: Multiple Clock Domains and TSV Sizing and Placement

We observe that dense clustered TSV regions around the cores alter voltage droop and thermal profile on each tier. Moreover, this effect worsens with the increase in core frequency and smaller TSV diameters. Experiments show that TSV clustered structures can affect thermal profile of tiers despite that each tier might have cores operating at the same switching frequency. Thus, the amount of heat transfer from TSVs (i.e., intratier and intertier) has an effect on the total amount of voltage droop per tier, which can also lead possible thermal blockage effects [50]. Such observation raises concerns on thermal-aware placement and sizing of TSVs while taking into account workload assignment, core switching frequency, and their stacking order.

VII. Conclusion

In this paper, electrothermal simulations are performed to derive the worst case power supply noise and temperature distributions on 3-D PDNs with multiple clock domains. This is the first work that targets 3-D PDN resiliency in the presence of various switching frequencies. We provide a guideline on modeling efforts for 3-D PDNs with multiple clock domains and describe mathematical formulations to derive the amount of self-induced and transferred power supply noise and temperature on each tier. We conduct experiments on several 3-D multicore benchmarks to investigate power supply noise and thermal issues. Our experimental results show that TSVs contribute to the amount of noise and heat transfer intratier and intertier. Certain combinations of clock domains cause severe voltage droop and elevated temperatures. Some mitigation techniques are explored, such as investigating workload assignment placement, stacking order, and TSV sizing and placement. Based on observations derived from the experiments, we present a list of observation and practical guidelines for ensuring power and thermal integrity of 3-D PDNs with multiple clock domains.

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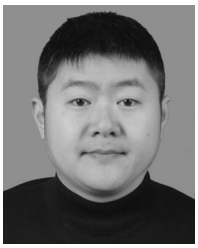
Aida Todri-Sanial (M'03) received the B.S. degree in electrical engineering from Bradley University, Peoria, IL, USA, in 2001, the M.S. degree in electrical engineering from Long Beach State University, Long Beach, CA, USA, in 2003, and the Ph.D. degree in electrical and computer engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2009.

She was an RD Engineer with the Fermi National Accelerator Laboratory, Batavia, IL, USA. She has held visiting positions with Mentor Graphics, Wilsonville, OR, USA, Cadence Design Systems, San Jose, CA, USA, STMicroelectronics, Geneva, Switzerland, and the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA. She is currently a Research Scientist with the French National Center of Scientific Research, Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, Montpellier, France. She has authored over 100 papers in VLSI design area.

Dr. Todri-Sanial is a member of the Association for Computing Machinery. She was a recipient of the John Bardeen Fellowship in Engineering at the Fermi National Accelerator Laboratory in 2009. She served as the General Chair of ISVLSI 2015 and participates on the Technical Program Committee of the IEEE Design, Automation and Test in Europe Conference and Exhibition, the IEEE International Symposium on Quality Electronic Design, the IEEE International NEW Circuits and Systems, the IEEE ISVLSI, and the IEEE Great Lakes Symposium on VLSI. She also serves as a Technical Reviewer of the IEEE TRANSACTIONS ON COMPUTERS, *Computer-Aided Design*, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, the IEEE TRANSACTIONS ON NUCLEAR SCIENCE, and the Institution of Engineering and Technology. She is an Associate Editor of the IEEE TRANSACTIONS ON VLSI. She is also engaged with European agencies, such as the European Platform of Women Scientists and the European Association for Women in Science, Engineering and Technology.



Yuanqing Cheng (S'11–M'13) received the Ph.D. degree from the Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China.

He spent one year in post-doctoral studies with the Centre National de la Recherche Scientifique, Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, Montpellier, France. He joined Beihang University, Beijing, China, in 2013, as an Assistant Professor. His current research interests include VLSI design for 3-D integrated circuits and spintronics computing system architecture.

Dr. Cheng is a member of the Association for Computing Machinery.