On Analysis of On-chip DC-DC Converters for Power Delivery Networks

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Abstract— **This paper explores the benefits and costs of integrating an on-chip DC-DC converter as voltage regulator module for reliable power delivery networks (PDNs). We perform detailed time-domain and frequency analyses on PDNs to assess the impact of on-chip DC-DC converter on PDN impedance and overall supply noise behavior. As results show, the reliability of PDNs depends on the DC-DC converter design and its efficiency. Various switching scenarios are analyzed for multiple voltage distributions on circuits of different sizes to explore the benefits of on-chip DC-DC conversion.**

Keywords— DC-DC converter, power delivery network, voltage drop

I. INTRODUCTION

Many systems (cellular phones, laptops, MP3 players which are using batteries as their power supply) require that the primary source of DC power be converted to other voltages. Such systems usually include several sub-circuits that need to be supplied with different supply voltage levels (*i.e.* different voltage potentials might be needed for memory, disc drives, display and operating logic), which may not be the same as battery's voltage level. Employing DC-DC converters is a method to generate multiple voltage levels from a single DC supply voltage to be fed to different sub-circuits on a chip. This method of generating multiple voltage levels from a single source can reduce the chip area substantially [1]. However, DC voltage provided by battery or rectifier contains high voltage ripples and it is not constant enough, thus it is not applicable for most devices. This is where, DC-DC regulators are employed to attenuate the ripples regardless of change in the load current or input voltage. Thus, not only they allow providing different levels of voltage but they also ensure more stability on the supply voltage.

There exist several types of DC-DC converters such as linear regulators, buck converters and switched capacitor converters which are some of the most well-known and used converter circuits. A buck converter requires large passive elements for inductance and capacitance (*LC*) as an output filter, however it also has higher power efficiency than a linear regulator. A switched-capacitor converter also needs a large capacitors and one more drawback is that the output voltage levels are limited by the ratios of the capacitors, which makes them not very suitable for low-power systems using dynamic voltage scaling method.

Based on existing literature, inductive converters tend to have better performance and efficiencies [2], [3] and fast response control over wide load range [4]. DC-DC converters with faster switching frequencies are becoming popular due to their ability to decrease the size of the output capacitor and inductor to save chip space. Meanwhile, the demands from the power supply increase as processor core voltage drops below 1V, making lower voltage level difficult to achieve at faster frequencies due to the lower duty cycle. In this paper, a DC-DC buck converter for low power applications is designed and implemented in 45nm CMOS technology based on PTM models [5], with input and output voltage of 1.8V and 1.1V, respectively.

One of the objectives of this paper is to first study the switching-mode power supplies (SMPS) and different controlling methods, which are commonly used in SMPS. Second, we implement a buck converter and analyze its power efficiency on power delivery networks. Overall, we develop a framework for analyzing the benefits and cost of on-chip DC-DC converters, their efficiency and impact on power delivery network's reliability. Figure 1 illustrates the concept of such analysis framework. Such framework allows us to investigate the downsizing of passive components like inductor's size without sacrificing the system's overall performance. As a case study circuit, we utilize a 35-stage ring oscillator that is designed in 45nm CMOS technology using Cadence Virtuoso tool.

The rest of the paper is organized as follows. Section II describes briefly the model of on-chip power delivery networks that we use in this work. Section III describes the DC-DC converter design and parameter selection that is used on our analysis framework. In Section IV, we present the simulation results based on time-domain and frequency analyses on PDN to assess the changes in PDN impedance and overall supply noise behavior. Section V, concludes the paper.

I. PDN MODELING

In order to develop an analysis framework for on-chip DC-DC converters, we start by establishing a power delivery network model that can serve as reference for studying the efficiency of the converter. To do so, a distributed power model is developed for a chip size of 1µm-by-1µm. As a switching circuit, we apply a 35-stage ring oscillator designed in 45nm technology node that draws current from the power delivery network.

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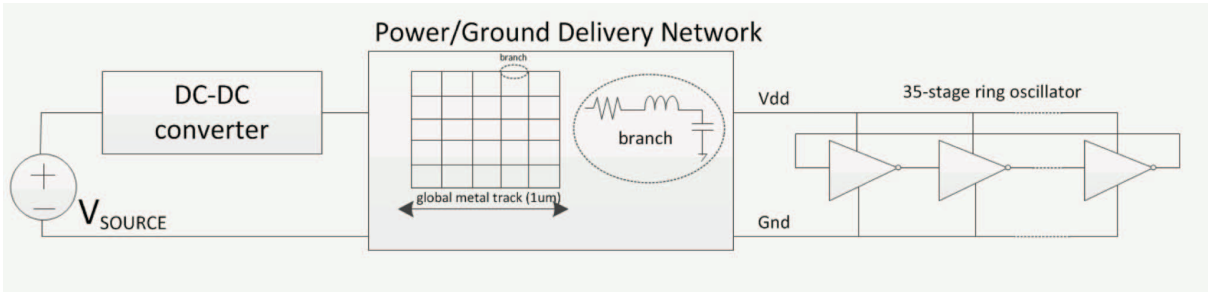

Figure 1. Overall description of analysis framework for investigating on-chip DC-DC conversion.

Power delivery networks are usually modeled as a mesh structure to represent their actual layout design with global metal tracks (i.e. top two metal layers) running in parallel and perpendicular where vias are inserted in their cross-sections. The mesh structure is represented as a distributed *RLC* network. Table I provides the electrical parameters used for the distributed power delivery model based on the PTM [5] interconnect model.

Table I: The electrical parameters used for the distributed power delivery mesh structure [5].

Typical wire dimensions	***RLC* values**	***RLC* (per mm)**
W=0.45µm s=0.45µm l=2500µm t=1.2µm h=0.2µm K=2.2	R=101.851 Ohms L=4.258nH M12=3.811nH M13=3.465nH M14=3.262nH (k12=0.895 k13=0.813 k14=0.766) C_{ground}=205.0775fF C_{couple}=183.055fF C_{total}=571.1875fF	R=40.7404 Ohm/mm L=1.7032 nH/mm Cg=82.031 fF/mm Cc=73.222 fF/mm Ctotal=228.48 fF/mm

The physical dimensions of the metal tracks for a chip size of 1µm-by-1µm are listed in Table II. The mesh size is represented as a 6-by-6 grid where each branch has the following *RLC* parasitics.

Table II: Power grid branch *RLC* parasitics used in this work.

PDN Branch Length	**Resistance**	**Inductance**	**Capacitance**
180 nm	7.2 m Ohm	306nH	0.4fF

II. DC-DC BUCK CONVERTER

In this section, we describe the design and chosen parameters for the DC-DC converter that we utilize for our analysis. A DC-DC contains two main blocks, a power processor and a feedback control part as shown in Figure 2. The feedback control loop is needed to assure the stability of the system and regulate the output voltage level by adjusting the switching duty cycle. Additionally, the feedback control consists of two main parts, a voltage error-amplifier (with compensation circuit) and voltage comparator to keep close the output voltage to a reference voltage. A circuit level representation of Figure 2 is shown in Figure 3.

The error-amplifier compares the feedback voltage (applied to inverting input) to a reference voltage (applied to non-inverting input) then their difference, which is called voltage error signal, is applied to non-inverting input of voltage comparator. The comparator circuit, which is simply $1/V_{osc}$ where V_{osc} is the peak-to-peak amplitude of the oscillator voltage, compares this error voltage to saw tooth ramp that is generated by ramp generator. If the error voltage is large then the output voltage of the comparator goes high but when the error voltage is small (i.e. negligible) then the output of the comparator goes low. According to this voltage, the driver determines the corresponding modulated signal duty cycle for control of the power switches.

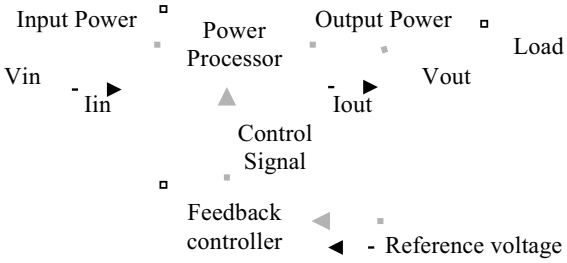

Figure 2. Block diagram of DC-DC regulator.

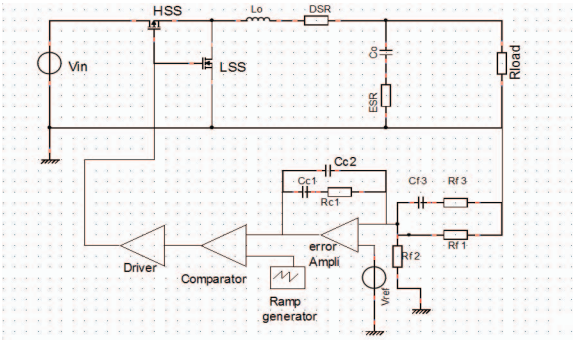

Figure 3. DC-DC converter circuit schematic.

In order to assure the stability of the system and derive the parameters of the converter, we modeled the circuit shown in Figure 3 with three blocks as presented in Figure 4. The power stage $G_p(s)$ includes the switches, the drivers and the output inductor and capacitor. The compensator block $H(s)$ represents the error-amplifier with the compensation network.

For simulation purposes, we implement a DC-DC converter design procedure for typical synchronous buck converter with voltage-mode control and voltage-mode error-amplifier based on 45nm CMOS technology. Such converters tend to improve noise immunity and efficiency, but require a certain amount of loop compensation to achieve an acceptable performance. By selecting such design, the DC-DC converter can provide a loop gain function with a high bandwidth (high zero-crossover frequency) and adequate phase margin. As a result, fast load response and good steady state output can be achieved which is an important criterion for on-chip DC-DC conversion. We apply an appropriate compensation network based on [6] in order to assure this stability.

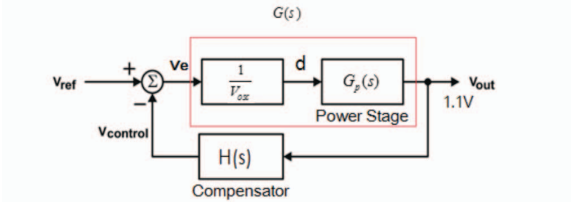

Figure 4. Block diagram model of the DC-DC converter.

Initially, the power and control stages are reviewed with respect to the small-signal model and relevant transfer functions. In the next subsections, we describe how the crossover frequency of the loop gain is significant in the context of the frequency range where feedback is effective in attenuating the closed-loop characteristics, followed by a detailed description of the compensator design procedure.

A. Power stage

The transfer function of the power stage can be represented as a second order system with a double pole at the resonance frequency F_{LC} of the LC filter and a zero produced by the ESR of the output capacitor as follows:

$$G_p(s) = \frac{V_{out}}{d}(s) = \frac{R_{Load}(C_0.ESR.s+1)}{L_0C_0.s^2(R_{Load}+ESR)+s.(L_0+R_{Load}.C_0.ESR)+R_{Load}} \times V_{in} \quad (1)$$

$$G(s) = G_p(s).\frac{1}{V_{osc}} \quad (2)$$

where L_o, C_o and R_{load} are the inductance, capacitance and load resistance values, respectively. ESR is the equivalent series resistance of the output capacitor. The parameter values are derived and chosen to optimize the buck converter design following the design theory described in [7].

B. Loop gain

The loop gain of system is defined as the product of transfer functions along the closed control loop. Based on the model shown in Figure 4, we derive:

$$M(s) = \frac{1}{k} \times H(s) \times G(s) \quad (3)$$

where $1/k$ represents the gain of the resistor divider which is used in the feedback loop when $V_{out}>V_{ref}$. The cross-over frequency, also called bandwidth of the loop is when the loop gain equals unity. It determines F_0, the speed of the system response to load transients. Typically F_0 can be set between 1/10 to 1/5 of the switching frequency where the higher the crossover frequency, the faster the load transient response would be. However, the crossover frequency should also be low enough to allow attenuation of the switching noise. The slope of the loop gain at 0Hz should be about –20dB in order to ensure a stable system. The phase margin should be greater than 45º for overall stability. As the double pole of the power stage causes the gain to fall within a slope of -40dB/dec up to the zero frequency (or F_{ESR}), which compensates one of the poles, a compensation network is needed to compensate the slope of -40dB to -20dB, so we can ensure a stable system.

C. Compensator

To have a stable closed loop buck converter with appropriate performance, a properly designed compensator is required. We utilize a Type III compensator as it provides enough phase margin by adding an extra zero to the system's closed loop transfer function to keep it stable, also shown in Figure 5.

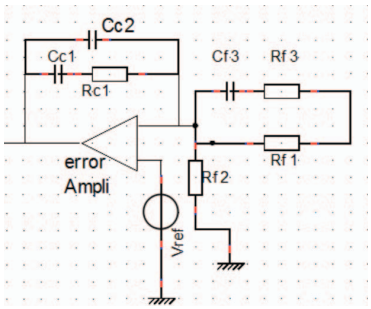

Figure 5. Type III compensation network.

The transfer function of type III compensator is given by:

$$H(s) = \frac{V_e}{V_{out}} = \frac{Z_c}{Z_f} \quad (4)$$

The pole generated by C_{c1} and R_{c1} is usually set at a much higher frequency as compared with the frequency of the zero generated by C_{c2} and R_{c1}. This means $C_{c1}<C_{c2}$. Therefore:

$$H(s) = -\frac{(1+R_{c1}.C_{c1}.s).\left[1+s.C_{f3}.(R_{f1}+R_{f3})\right]}{R_{f1}.s.C_{c1}.(R_{c1}.C_{c2}.s+1).(1+s.R_{f3}.C_{f3})} \quad (5)$$

The conventional compensation strategy [8], [9] employed with voltage mode control is to use two compensator zeros to counteract the LC double pole, one compensator pole to nullify the output capacitor ESR zero and one compensator pole located at one half switching frequency to attenuate high frequency noise. By performing the computations, $F_{z2}=F_{LC}$=4.6MHz, $F_{z1}=0.75F_{LC}$=3.45MHz, $F_{p2}=F_{ESR}$=0.4GHz, and $F_{p1}=F_s/2$=1GHz are obtained.

III. Simulations and Results

Here, we perform two types of analyses: (1) with DC-DC converter, and (2) without DC-DC converter where an ideal supply source is used to supply voltage to the 35-stage ring oscillator. The ring oscillator has a 2GHz operating frequency based on 45nm CMOS technology.

A. Jitter and phase noise in ring oscillators

In general, CMOS circuits are sensitive to power supply fluctuations, as well as to noise generated in nearby switching

circuits (such as noise transferred through power grid and substrate). Hence, the propagation delay t_d, is a function of supply voltage. Delay variations can be created due to variations on the rising and falling edges, which are also referred as jitter [10]. Figure 6 depicts a comparison between the transient analysis of the ring oscillator when powered by an ideal supply voltage and the DC-DC converter. It shows an operating frequency of 2GHz for the ring oscillator and no additional delay or phase noise is observed due to converter.

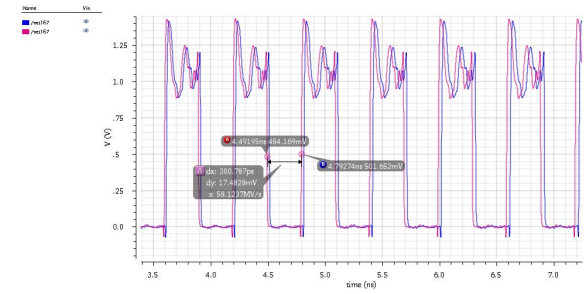

Figure 6. Output transient analysis of ring oscillator with and without DC-DC converter.

B. PDN impedance

Figure 7 shows the impedance plot of the PDN using an ideal voltage source versus using the DC-DC converter. The most noticeable is a resonant peak in the crossover frequency; this is due to the bandwidth of the converter. The converter has to have low bandwidth since parasitics appear at low frequencies.

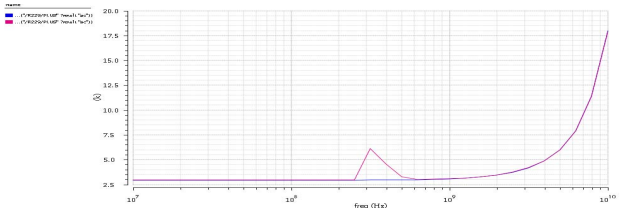

Figure 7. Comparison of the PDN impedance with and without DC-DC converter.

C. Voltage drop

Voltage drop is an important PDN metric because it is directly related to the delay increase and frequency degradation. Figure 8 shows the DC-DC converter output voltage supplied to the ring oscillator on various PDN nodes. The worst-case voltage drop is determined from the supply voltage transients. Figure 9 shows the voltage drop map on each PDN node when using the DC-DC converter versus the ideal voltage supply. The comparison between the two distributions shows a higher voltage drop when DC-DC converter is used.

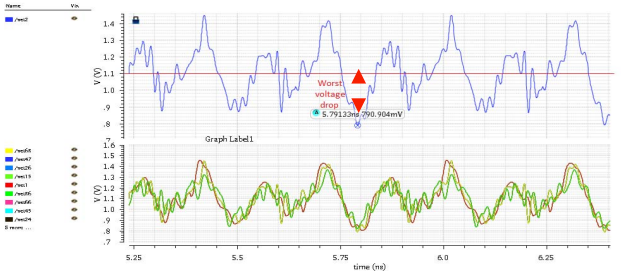

Figure 8. Worst-case voltage drop with DC-DC converter.

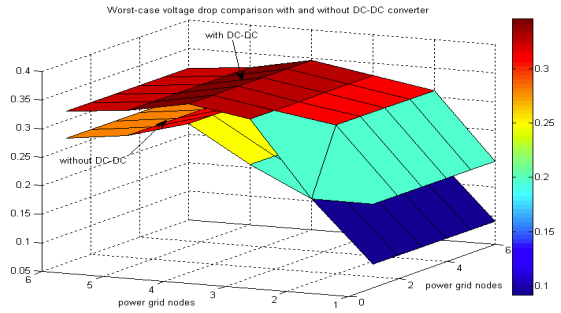

Figure 9. Voltage drop map on each PDN node with DC-DC converter versus ideal supply voltage.

IV. Conclusion

In this paper, an analysis framework was described for studying on-chip DC-DC converters for reliable power delivery. Simulation results show that while implementing on-chip DC-DC converter still requires research on downsizing of discrete inductive and capacitive components to be able to implemented on-chip, nevertheless it presents a viable solution for future low-power high-performance embedded systems. Integrating DC-DC converter shows no additional delay or phase noise on the system. As future work, we will investigate larger and more complex circuits with various on-chip DC-DC converters for multiple voltage domains and their impact on systems performance and PDN reliability.

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