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Present and Future Prospects of Carbon Nanotube Interconnects for Energy Efficient Integrated Circuits

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Abstract

Carbon nanotubes (CNTs) due to their unique mechanical, thermal and electrical properties are being investigated as promising candidate material for on-chip and off-chip interconnects. The attractive mechanical properties of CNTs, including high Youngs modulus, resiliency and low thermal expansion coefficient offer great advantage for reliable and strong interconnects, and even more so for on-chip and off-chip integration. High bandwidth interconnects are required for achieving denser, faster and energy-efficient circuits. Due to their unique properties, CNTs present an opportunity to address the current challenges of copper interconnects and provide solutions for reliable efficient and smart system integration. In this work, we give an overview on the current advancements on CNT interconnects and the future prospects for energy efficient integration.

1. Introduction

While scaling into deep nanometer regime is improving transistor performance, the reverse is happening for the interconnects. Copper (Cu) interconnects were introduced in 1998 and since 2001 International Technology Roadmap for Semiconductors (ITRS [1]) highlighted problems with resistivity increase as line widths approached electron mean free paths due to scaling. To slow this pace, by 2003 low-κ insulator dielectrics were introduced, however Cu resistivity continued to rise due to electron scattering. Additionally, yield issues associated with integration of low-κ materials with copper proved to be more challenging than expected. ITRS reports that current density limits for copper will be exceeded by 2017.

Smaller cross-sectional area of interconnects increase its resistance, hence degrade performance and power consumption. ITRS reports state that circuit performance is no longer limited by transistors but the interconnects are becoming the bottleneck. With continuous aggressive scaling on device nodes, interconnects have not kept pace and proven very difficult to scale down as dies sizes have shrunk. Accelerated technology scaling has aggravated copper resistivity increase due to electron scattering and, even more severely, introduced electromigration issues. Due to the increasing miniaturization the trenches and vias have become smaller thus increasing current density. Consequently, electromigration will lead to drastic challenges in terms of the reliability of the whole system. Mass transport along interfaces and grain boundaries in copper interconnects is among the most important issues to be solved for future technology nodes.

While some solutions have been found for the logic and memory applications up to 14nm node, there is an on-going race on contenders for replacing copper interconnects. Thinner barrier and adhesion layers, doping of metals to enhance the grain boundary resistance, and selective capping are some of the adopted solutions for coping with the copper interconnects [1]. As we go beyond 10nm and 7nm nodes, novel interconnect material and integration approaches are needed and are currently under investigation.

In digital logic design, local interconnects (interconnects closer at device level) and intermediate interconnects tend to shrink with scaling, thus the impact on their delay is minor. Global interconnects (usually used for power/ground and clock) have the greatest wire lengths and widths, and are the most impacted by scaling. The problem is even more severe for memories. Bit-line (local metal layer) in memory cell has the most aggressive metal pitch and its contact layer has the highest aspect ratio in all semiconductor devices. Therefore, they face the largest delay due to electron scattering. To date, research has not identified any potential solutions to these problems. Hence, the interconnect problem is acute and the limits of copper interconnects are fast approaching.

Carbon nanotubes (CNTs) have drawn a lot of interest over the last decade due to the favorable electrical, mechanical, chemical and thermal properties. There are many on-going research efforts on carbon nanotube devices, sensors and photodectectors - their application for back-end-of-line interconnect material is also gaining momentum. One essential application of the nanotubes in microelectronics is as interconnects due to their ballistic (without scattering) transport of electrons and the extremely high thermal conductivity along the tube axis. Electronic transport can go over long nanotube lengths, 1μm (compared to a few nm in copper), enabling CNTs to carry very high currents (i.e. $\geq 10^9$ Acm^2, compared to 10^7 Acm^2 in copper) with essentially no heating due to

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2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems

nearly 1D electronic structure.

In this paper, we provide an overview on the recent advancements of carbon nanotubes as interconnect material for back-end-of-line. The rest of the paper is organized as follows. Section II presents some of the research work related to CNT on-chip interconnects covering aspects from doping, and composite CNTs for enhancing current density and lowering resistance. Section III provides an overview on CNT based through-silicon vias. Section IV covers some of the on-going efforts on the chip design efforts with CNT devices and interconnects for energy efficiency. Section V provides an overview on the prospective research problems related to CNT interconnects and Secton VI concludes the paper.

2. CNTs for On-Chip Interconnect

CNTs can be either single-wall (SWCNT) or multi-wall (MWCNT). Research papers on CNT interconnects date as early as 2002 by [21]. It has been reported that SWCNT bundles with same dimensions as Cu/low-κ interconnects can provide significant improvement for replacing Cu/low-κ long interconnects [29], [28], [34], [25]. An arrangement of few-layer SWCNTs has shown to reduce the CNT-based interconnects by as much as 50% and help reduce the delay and power consumption which can be particularly interesting for local interconnects [24]. As for MWCNTs, it was proven both theoretically and experimentally that all inner shells can conduct if properly connected [23], [16], [5], [27], [37] and can potentially outperform Cu and SWCNTs. Recently MWCNTs interconnects operating in gigahertz frequency range have been demonstrated, however their conductivity is considerably lower than the theoretical models predict due to large defect density [10], [7]. More recently, researchers from Stanford University have designed and fabricated the first carbon nanotube computer [4], which operates on only 1 bit of information and uses a single instruction. While a simple computer design approach, it revealed a significant advance on fabricating a circuit using only CNT field effect transistors (CNFETs).

Fig. 1 illustrates a cross-sectional view of integrated circuits with devices (font-end-of-line), local and global metal layers (back-end-of-line). There are still several process and reliability related challenges that need to be addressed before CNTs can enter as mainstream VLSI interconnects. At this time, challenging steps are directional growth of CNTs, achieving high fraction of metallic, high-density integration and low-contact resistance. Although some progress has been made to control the horizontal growth of CNTs [22], a large number of publications report on large contact resistance indicating technological challenges in making good contact. It is also reported that carbon molecules on the surface of CNTs affect electrical resistance imposing additional technical challenge to producing defect-free CNTs. Due to technological challenges, CNT interconnects are unlikely to replace all copper interconnects at once but rather gradually — introducing hybrid structures such as doped and metal composite CNTs.

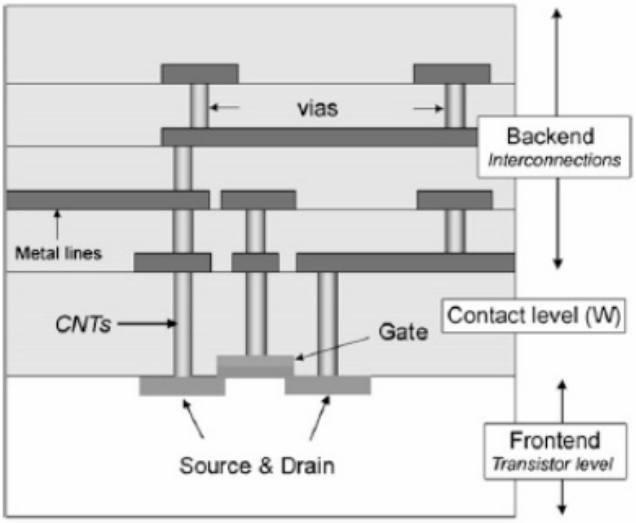

Figure 1. Illustration of a two-tier 3D power delivery network with several blocks representing multiple clock domains.

A. Doped CNTs

As already mentioned above, over the recent years there have been many advancements on process and growth of CNTs interconnects and more specifically for vertical lines. Currently, several growth techniques have been established to synthesize carbon nanotubes at workable temperature levels for microelectronics process (i.e. below 450^oC) with the ability to control nanotube dimensions, density (i.e. up to 10^{13} CNTs cm^{-2}) and patterning at specific locations [19], [41], [36], [32], [14], [33], [15]. However, the design of catalyst to control nanotube chirality and especially for metallic nanotubes is very challenging [31], [20]. It is one of main challenges for CNT interconnects, to design catalyst and process conditions that simultaneously give ultrahigh area densities, chiral selectivity and growth on conductive support layers [13]. Unselective growth (i.e. little control on chirality) would result in CNT interconnects with resistivity values up to 3 orders of magnitude higher than that of copper (Cu) [17], [12], [26].

Hence, doping carbon nanotubes (i.e. by using evaporated MoO_3) an alternative to reducing resistivity while maintaining high density and growth of metallic CNTs. Significant decreases in resistivity were obtained up to $50\mu\Omega cm$ which the lowest resistivity measured value to date on nanotube bundles while maintaining a highly ordered alignment [13]. The improved electrical resistivity due to doping was attributed to the shift of the Fermi energy of semiconducting nanotubes along with the conversion of the oxide into a layer of metallic character [13]. Doped CNTs might be potential candidates

for replacing on-chip local interconnects due to lower resistivity for short interconnect lengths typically used for local interconnects.

B. Composite CNTs

To overcome electromigration issues currently facing copper interconnects; carbon nanotubes are promising due to their high current carrying capacity. Meanwhile, to ensure fast performance (minimal interconnect delay), interconnects should also have high conductance (low resistivity). However, high conductance and high current carrying capacity are mutually exclusive properties. Hence, researchers have turned their attention to copper-carbon nanotube composite that overcomes this mutual exclusivity. The incentive behind the metal-CNT composite is to obtain high current densities by exploiting the properties of CNTs and high contact conductance from the metal properties. In [6] achieved 100 times higher current carrying capacity than copper interconnects.

Cu-CNT composite interconnects can be potential replacements of global copper interconnects. Global interconnects for supply voltage delivery are susceptible to electromigration issues due to large amount of unidirectional current flowing for long period of times, which ultimately cause atoms to migrate by creating voids and hillocks. Electrical measurements have shown up to 50% reduction in electrical sheet resistance and 2 order of magnitude increase in current density in Cu-CNTs which can lead to significant performance gain and reliability enhancement of integrated circuits.

3. CNTs for Through-Silicon Vias

Another important aspect of interconnects is off-chip interconnects. As future high performance systems will demand large memory bandwidth accessible next processors, the state of the art of off-chip interconnects (i.e. 25pJ/bit) needs to be further improved to allow for low-power, fast and high bandwidth interconnects. Three-Dimensional (3D) integration is one of the most promising technologies for System-on-Chip (SoC) developments and as a viable solution for heterogeneous integration (i.e. processors, memory, digital, analog, mems, sensors, harvesters, etc.). Through-Silicon-Vias (TSVs) are the key enablers of 3D integration by providing continuous connections between different stacked dies. TSVs are etched on silicon substrate and filled either with copper or Tungsten (W). However, these materials have limitations due to highly demanding fabrication process, reliability, manufacturability and performance. In the recent years, a lot of research efforts have been dedicated to development of carbon nanotube based TSVs for 3D integration. CNT TSVs present an opportunity to further progress packaging technology and enable high-density interconnects [8].

CNT TSVs are extensively investigated and several research groups have successfully implemented growth and realized functional integration of multi-wall CNT bundles as high aspect ratio TSVs. In [18], CNT TSV bundles were grown in sub-5μm diameter on top of metal lines in a bottom-up approach which is compatible with CMOS process temperatures. In [35], integration scheme for CNT-based TSVs are demonstrated for two scenarios – connecting on TSV to another and connecting a TSV to a metal pad. Authors reported on integration scheme for vias 100μm in diameter and 132μm deep and the obtained via and contact resistance values of 46Ω and 9.8Ω, respectively. In [42], CNT TSV bundles with 50μm length and aspect ratio 5 or 10 were demonstrated. CNT bundle resistance of 69.7Ω were reported. Further improvement on integration scheme and lowering contact resistance of vias are required for enabling seamless integration of CNT TSVs as off-chip interconnects.

4. Design Methods

To overcome the challenges of processing highly aligned CNTs (i.e. either for devices or interconnect), there is also a lot of on-going research efforts on circuit design methods that take into account misalignment and mispositioned CNTs to design functionally correct and reliable circuits. Thus, circuit designers are looking into efficient methods to design reliable, energy efficient and high performance for CNT based circuits. One effective method that has been applied by [30] is that after transferring CNTFETs or CNT interconnects, regions of misalignments are identified and are etched away by using lithography. These techniques are known as CNT removal after CNT growth by electrical burning [11] or selective etching [43].

A strong motivation for this work is that disregarding defective chips with misaligned or mispositioned CNTs or reconfiguring around defective cells and interconnects after testing may be very expensive and simply not feasible due to complexity in processing methods. Moreover, traditional fault-tolerance techniques (i.e. redundancy) might not be applicable due to large area and power overhead. Hence, many research efforts are focused on defective CNT-immune design techniques while having a minimal impact on existing design flows. Additionally, considerable progress has been made toward full wafer-level CNTFET based digital systems. Recently, researchers [4] have demonstrated the first processor design with CNTFETs and developed VLSI-compatible design techniques to overcome the challenges of CNT imperfections [3].

Carbon nanotubes present as well interesting thermal properties as interconnect material. Theoretical and experimental analyses have also shown negative thermal coefficient of resistivity (TCR) for MWCNTs [9], [40]. Negative TCRs can be explained from the fact that there are more channels in MWCNTs contributing to conductance at higher temperatures as per Fermi-Dirac distribution. Larger number of channels lowers both scattering resistance and contact resistance. The negative TCR is opposing with other metals (i.e. copper) conductors,

which presents an advantage for carbon nanotubes to be implemented as on-chip interconnect material.

To explore energy efficiency of carbon nanotube based circuits and recent advancements on nano-engineering, researchers [2] have presented a design approach that capitalizes on several recent nanotechnology breakthroughs aka N3XT. The main thrust of N3XT is to include high performance and energy efficient devices based on CNTs, combined with large amount of nonvolatile memory (such as low-voltage resistive RAM and magnetoresistive memories as spin-transfer torque magnetic RAM, STT-MRAM) and new microarchitectures for scalable computing that are all implemented in fine-grained (monolithic) 3D integration with ultra dense interconnects between logic and memory layers. Exploiting the progress on each technology enables new system integration that promises high energy-efficiency and high performance yet scalable and reliable [38], [39].

5. Research Prospects

Carbon nanotubes present viable solutions to overcome the current challenges with copper interconnect. The main challenge of bringing CNTs to circuits is not just in the technology. The scientific community still lacks the know-how to exploit CNTs both as devices and interconnects. Understandings such as to what extent CNTs can be exploited for reliable and efficient interconnect architectures: are certain device (i.e. CNTFETs, deeply scaled bulk CMOS, FinFET, FDSOI, etc) technologies more suitable to be integrated with CNTS and give best performance, and how to design optimal circuits despite of having non-perfect CNTs are significant challenges to be addressed and if we are to truly find a replacement material for copper. Research problems related to physical modeling, physical design, design space exploration and chip-package interactions with CNTs interconnects are gaining momentum and will provide a clearer picture to the costs and benefits of integrating CNTs as on- and off-chip interconnects.

6. Conclusions

In this paper, we provide an overview on the advancements of carbon nanotube based interconnects. There are many on-going researches focused on the processing and growth of carbon nanotube interconnects for achieving high density, directional growth and well aligned carbon nanotubes. To allow integration of CNT interconnects as on-chip interconnects, there are two short term solutions being explored by the community. Doped CNTs present interesting properties to be used as local interconnects by reducing their contact resistance. Metal-CNT composite materials are also being explored as potential replacement of global copper interconnects to allow high current densities. To further increase package density and bandwidth, carbon nanotube based through-silicon-vias allow faster, denser and reliable off-chip interconnects. Moreover, advancements in nano-technologies manufacturing such as CNTs, non-volatile memories, 3D integration bring new opportunities for designing energy efficient, high bandwidth and high performance circuits and systems.

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