# A clustering technique for fast electrothermal analysis of on-chip power distribution networks

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*Abstract*—**This paper presents an equivalent self-consistent electrothermal circuit model for power integrity analysis of large on-chip power distribution networks. Two coupled circuits are used to co-simulate the electrical and thermal behavior of the power grid. After a steady-state analysis, the order of the circuit is strongly reduced by means of a node clustering technique. The obtained low-order circuit allows a cost-effective complete power integrity analysis, including dynamic analysis and evaluation of time-domain features like voltage droop. As a case-study, a 45-nm chip power grid is analyzed: the full circuit for the electrothermal model with 4 million nodes is reduced by a factor of about 3500x, with a relative error on the solution below few percent.**

*Keywords— On-chip power distribution networks; IR-drop; model order reduction; electrothermal analysis, power integrity.*

## I. INTRODUCTION

The temperature increase related to power dissipation in on-chip Power Distribution Networks (PDNs) may strongly affect the electrical performance of such networks in conventional VLSI architectures (*e.g.* [1]) or innovative 3D ICs (*e.g.* [2]). In addition, it is well-known that the PDN thermal behavior is strictly related to reliability issues like electromigration [3]. As a consequence, a self-consistent electrothermal modeling is needed to get accurate power integrity analysis and a reliable design of PDNs.

The thermal problem is coupled to the electric one via the heat production term, which depends on electrical power dissipated for device activity and for joule effects in the grid conductors. On the other side, the electrical problem is related to the solution of the thermal one since the electrical parameters, such as the resistance, depend on temperature. Usually the electrothermal co-simulation system consists in solving these coupled problems with a relaxation approach:
(i) the heat production term is evaluated at initial temperature;
(ii) solving heat equation provides the temperature distribution;
(iii) the temperature-dependent electrical parameters are updated and the electrical problem is solved;
(iv) the heat production term is updated.
Reaching the convergence to a fixed accuracy stops the cycle.

In principle, the solution of the thermal model may require a full-3D numerical simulation of the problem (via FD, FEM or BEM methods, for instance). This approach accurately describes 3D geometries and accounts for air convection or cooling effects, but at extremely high computational cost [4]. However, in many cases of practical interest, in PDN structures, materials are homogeneous and the heat mainly flows along the grid conductors (grids and vias), being negligible the heat exchange between copper and dielectric. In such a case, a simple equivalent electrical network is used (see Fig.1), where an equivalence is established between temperature and voltage, heat flow and electrical current, thermal and electrical resistance and capacitance, heat production and current source, initial temperature and voltage source. The main advantage of this approach resides, of course, in the possibility of handling the electro-thermal modeling in the common frame of SPICE-like simulators. However, PDNs are very complicated structures including power planes, metal traces, chips, packages, decaps, vias and controlled collapse chip connection (C4) bumps [2], and thus even describing each subpart with a simple electrical RLC model and with the equivalent thermal model in Fig.1, the size of an equivalent network describing PDNs easily reaches the order of several millions of nodes. Dynamic analysis (for instance noise analysis) of such large networks is likely to be unaffordable, hence reducing the computational cost of simulations has become a major issue.

Unlike the signal interconnects, where the propagation plays a fundamental role, hence any accurate circuit model must handle a huge number of poles, a PDN is usually characterized by a huge number of nodes, but at a low number of poles. Therefore, modest results can be achieved for PDNs when using popular model-order reduction techniques suitable for signal interconnects, such as those based on subspace projections [5]-[7]. Recently, new reduction approaches have been proposed for electrical networks, based on the concept of node reduction [8]-[9].

In [10] the Authors have proposed a novel model-order reduction technique based on the concept of *node clustering*. A preliminary steady state solution of the Electrothermal (ET) problem provides the distributions of temperature and voltage drop values at each node of the PDN. Choosing a quantization for temperature and voltage drop the nodes are then clustered
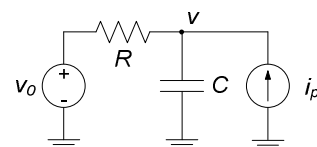


Fig.1 Simple equivalent electrical model for the thermal problem.

into supernodes and a reduced order circuit is obtained where the thermal and electrical interactions take place between supernodes. In [10] the model was limited to steady state analysis, and thus only the resistive elements were taken into account. In the present paper the work has been completed by including the dynamic parts and by extending the study to AC and to time domain noise analysis, thus providing a complete tool for PDN power integrity.

In Section II the electro-thermal model is briefly revised, whereas Section III introduces the clustering technique. A case study is provided in Section IV, referring to a 45nm chip PDN.

## II. ELECTRO-THERMAL MODEL

We consider a standard PDN structure as the one depicted in Fig.2, where two conductor grids are connected to VDD and GND supply pins, respectively. The VDD grid is connected to package by a series impedance $Z_{supply}$ (not shown here), whereas the GND grid nodes are connected to a heatsink, for heat dissipation purposes. The electrical model describing the interaction of each single node with neighborhood is depicted in Fig.3a: each interconnect between the node and any adjacent node in the same grid is modeled as an R-L series, whereas the connection between corresponding nodes of different grids is modeled by a capacitor in parallel with a current source $I_0$. The latter represents the circuit *switching activity*, i.e. the current demand of a circuit connected between VDD and GND pins. The solution of the electrical problem provides the so-called *voltage drop* at any generic node $i$, namely:

$$V_d(i) = V_{DD} - (V_n(i) - V_g(i)), \quad (1)$$

being $V_n(i)$ and $V_g(i)$ the node potentials with respect to the power and ground plane references, respectively.

The temperature distribution over the grid nodes is obtained by solving the thermal problem, modeled by the equivalent circuit in Fig.3b. In the following we assume that the grid discretization is fine enough that the branch lengths are smaller than or equal to the characteristic thermal length: in this case, we can adopt the same grid for the electrical and thermal problems [9]. The thermal resistances $R_{TH}$ and $R_{HS}$ correspond to the PDN segments in the same grid, and to the connections to heatsink, respectively. Note that the thermal capacitor in Fig.1 is omitted, which means that the dynamic behavior of thermal solution is neglected, which is a realistic assumption in the considered problem, being the time scales of the thermal problem much greater than those of the electrical one.

As pointed out in the introduction, the thermal circuit solution depends on the electrical solution via the equivalent controlled current source in Fig.3b, which models the heat generation produced by: (*i*) the switching activity, $P_S(i)=I_0V_d(i)$; (*ii*) the Joule effect into the conductors connected to such a node, $P_J(i)$. The electrical circuit solution depends on the thermal solution by means of the classical relation between conductor resistivity and temperature:

$$\rho(T) = \rho_0(1 + \alpha_0 T_r), \quad (2)$$

where $T_r = T - T_0$ is the *temperature rise* with respect to a reference value $T_0$. For copper conductors and $T_0 = 300$ K, it is $\rho_0 = 1.72 \times 10^{-8}\Omega m$ and $\alpha_0 = 0.0039$ K$^{-1}$. The two problems are coupled in a classical relaxation approach.
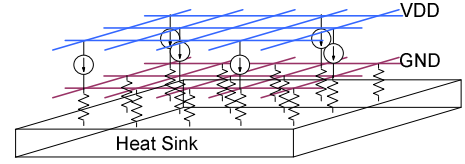


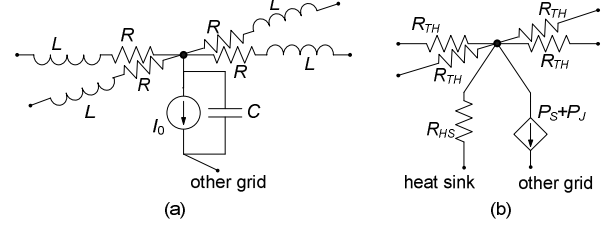Fig.2 The considered power delivery network structure.



Fig.3 Electrical (a) and thermal (b) circuit model at each grid node.

## III. ORDER REDUCTION BY NODE CLUSTERING

The ET model consists in an electrical and a thermal network, each of them containing two grids (VDD and GND) of $N$ nodes. The clustering technique proceeds as follows:

*STEP 1.* Solve ET problem for the full model in steady-state condition. This provides the distributions of voltage drop on electrical nodes and of temperature on thermal ones.

*STEP 2.* Define a quantization $V_{dk}$, with $k=1,..N_V$ ($T_{rh}$, with $h=1,..N_T$) for the voltage drop $V_d$ (the temperature rise $T_r$). For uniform quantization, the levels are separated by:

$$\Delta V_d = (V_{d,\max} - V_{d,\min})/(N_V - 1),$$
$$\Delta T_r = (T_{r,\max} - T_{r,\min})/(N_T - 1). \quad (3)$$

If necessary, different quantization steps $N_V$ and $N_T$ can be chosen for the electrical and thermal problem, respectively, due the different nature of the two physical problems.

*STEP 3.* Cluster in the $k$-th electrical supernode each electrical node $i$ such that: $|V_d(i) - V_{dk}| \leq \Delta V_d$. Cluster in the $h$-th thermal supernode each thermal node $j$ such that: $|T_r(j) - T_{rh}| \leq \Delta T_r$.

*STEP 4.* Build the incidence matrices $\mathbf{A}_e$ and $\mathbf{A}_t$ and the admittance matrices $\mathbf{Y}_e$ and $\mathbf{Y}_t$ of the reduced electrical and thermal networks, respectively. Matrix $\mathbf{A}_e$ is easily obtained by checking the correspondence between original nodes and final supernodes. The generic element $(k,m)$ of $\mathbf{Y}_e$ (corresponding to supernodes "$k$" and "$m$") is obtained by summing up all the admittances $\overline{Y}_{ij}$ of the original electrical network, such that $i \in k$, $j \in m$. Finally, the equivalent current sources to be inserted between supernodes $k$ and $m$ are obtained by summing all the sources terms $I_0$, inserted between a pair of nodes $(i,j)$, being $i \in k$, $j \in m$. After this step, we obtain the circuit model:

$$\mathbf{Y}_{er}\underline{V}_d = \underline{I}_0, \quad \mathbf{Y}_{er} = \mathbf{A}_e^T\mathbf{Y}_e\mathbf{A}_e, \quad (4)$$

The same approach is applied for the thermal network.

*STEP 5.* Synthesize (4) into a SPICE netlist. ♦

The final electrical circuit contains $2N_V$ nodes; such a number depends, of course, on the chosen quantization, *i.e.*, on the desired accuracy. The great advantage of the proposed procedure resides in the fact that the analysis of the complete networks is performed only in steady state condition, whereas the power integrity analysis is performed with the SPICE reduced circuit. In principle, the steady state analysis can be also carried out at a frequency different from zero. Nevertheless, since the power in PDNs is mainly associated to the DC component, and assuming that the physical dimensions are such that no resonance falls into the frequency band of interest, we verified that the clustering obtained by using the DC solution did not change if an AC signal was superimposed.

## IV. RESULTS

The analyzed case-study was a standard PDN with the structure as in Fig.2, referred to a core of dimensions 20 mm x 20 mm. A 1020×1020 grid was assumed for each PDN plane (VDD and GND planes), which means that each electrical grid contains about 1 million nodes. As pointed out in Section 3, the same grid was used for the equivalent thermal circuit, thus the total number of nodes is about 4 millions. The structure was obtained by a 20×20 replica of a basic stamp made of 2601 (51×51) nodes. The basic stamp was fed at its four corners, where it was connected through C4 bumps to the package through a package impedance $Z_{supply}$. Each grid branch was made by a copper conductor with section $WxH$ and length $l$. We investigated the 45nm technology, whose typical parameters are reported in Table I [11]. Note that the range of values for $I_0$ corresponds to chip power density 1.5 µW/µm$^2$ , which is a typical value for such a technology [11]. The electrical and thermal circuit parameters reported in Table II were estimated through the Predictive Technology Model [12].

The temperature and voltage drop distributions on the basic stamp (51×51 nodes), provided by the preliminary full DC analysis, are reported in Fig.4. Assuming uniform quantization with $N_V$ =55 and $N_T$ =77, (which correspond to $\Delta T_r = 0.32$ K and $\Delta V_d = 0.74$ mV ), the clustering procedure provides a reduced electrical circuit of 55 nodes (instead of 2601) for each VDD and GND plane, with a reduction factor of 47x. As a proof of consistency for the DC solution, the synthesized low-order SPICE circuit was used to reproduce the

map in Fig.4b: the relative error distribution provided in Fig.5 clearly proofs the consistency.

To check also consistency for transient solutions, we compared the maximum *voltage droop* provided by the full and reduced circuits, see Table III. The voltage droop at each node was evaluated by stimulating the PDN with a periodic triangle-wave current, integrating each voltage over a period, and dividing for the period itself. The stimulus triangular waveform was characterized by base level of 0.577 mA, peak $I_{peak}$=0.769 mA, $t_{rise}$=50 ps, $t_{peak}$=10 ps, and $t_{fall}$=100 ps [2].
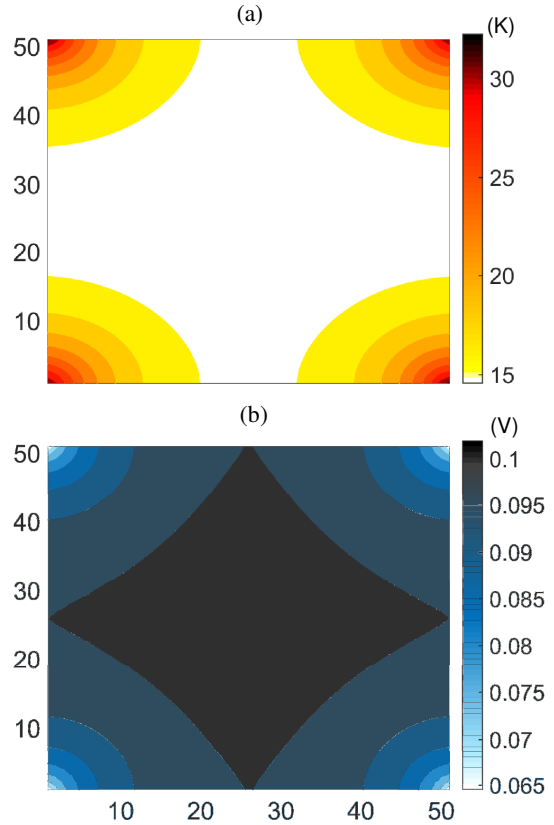


Fig.4 Steady-state maps: (a) temperature rise (in K); (b) and voltage drop (in V) for the 51x51 PDN.
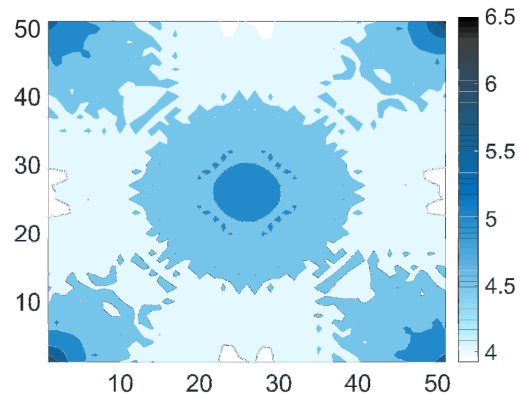


Fig.5 Percent relative error in the voltage drop distribution estimated by the SPICE reduced order circuit, for the basic stamp 51x51 PDN.

### TABLE I
#### TYPICAL PARAMETERS FOR A 45-NM PDN [11]

| $W$ [µm] | $H$ [µm] | $l$ [µm] | $V_{DD}$ [V] | $I_0$ [mA] |
|---|---|---|---|---|
| 10 | 1 | 1000 | 1 | 0.577 |

### TABLE II
#### CIRCUIT PARAMETERS FOR ELECTRICAL AND THERMAL MODELS

| $R$ [mΩ] | $C$ [pF] | $L$ [nH] | $R_{supp}$ [Ω] | $L_{supp}$ [nH] | $R_{TH}$ [kK/W] | $R_{HS}$ [MK/W] |
|---|---|---|---|---|---|---|
| 21.56 | 3.845 | 0 | 0.01 | 60 | 2545 | 0.25 |

### TABLE III
#### VOLTAGE DROOP ESTIMATED WITH FULL AND REDUCED CIRCUITS

| Stimulus (waveform) | Full circuit | Reduced circuit | Relative error [%] |
|---|---|---|---|
| *Triangular* | 95.938 mV | 90.502 mV | 5.67% |

After the consistency check on the basic stamp, the clustering procedure was applied to the full ET model of the chip with 4 million nodes. The preliminary steady state analysis provided the temperature and voltage drop distributions, as shown in Fig.6. Assuming the same quantization as for the basic stamp, the clustering procedure provides a reduced electrical circuit of 300 nodes for each plane, with a reduction factor of 3468x. A consistency proof showed that the reduced circuit is able to reproduce the maps in Fig.6 with a maximum error of about 0.4% in voltage and 2.5% in temperature (see Fig.7). The reduction factor may be lowered when a better accuracy is required, as shown in Fig.7.

The reduced SPICE circuit was synthesized and used to perform noise analysis on PDN to retrieve the voltage droop, which was estimated to be 75.53 mV for the same feeding conditions as in Table III.

Finally, to have a quantitative measure of the computational cost, we used a PC with 32GB RAM and a quad-core processor, equipped with HSPICE version G-2012.06 [13]. With such a configuration, the full chip cannot be simulated by HSPICE because of the too large number of dynamic elements. The preliminary steady-state solution (including several iteration of the relaxation cycle) took 60 s, while additional 10s are needed for the reduction process. The HSPICE simulation on the reduced circuit took 6.2s.

## V. CONCLUSIONS

The paper presented a clustering technique able to strongly reduce the computational cost of the electrothermal analysis of large chip power distribution networks, both for the DC and dynamical cases. The full network analysis is limited to a steady-state simulation, much less costly than the full dynamic solution of the electrothermal problem. The dynamic analysis of the PDN is then carried out with the obtained SPICE reduced order circuit. The analyzed case-studies demonstrated the consistency of the technique and its capability of reducing the complexity of a grid of 4 million node by a factor of about 3500.
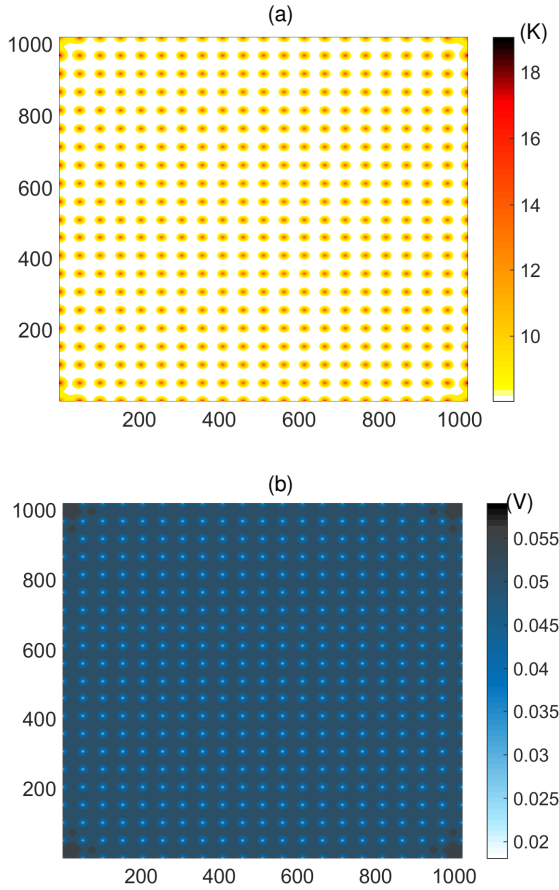


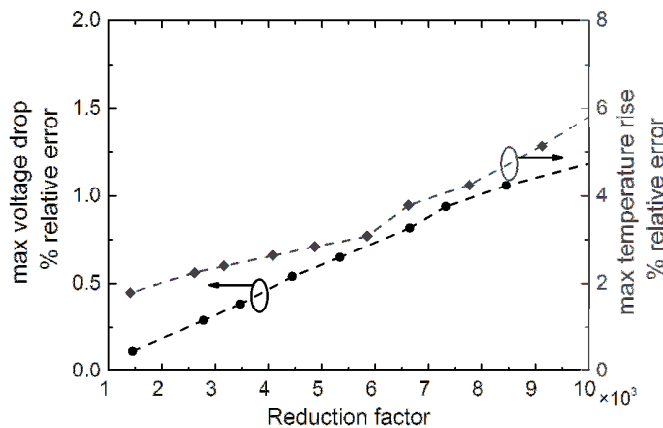Fig.6 Steady-state maps: (a) temperature rise (in K) and (b) voltage drop (in V) for the 1020x1020 PDN.



Fig.7 Percent relative error for temperature rise (right axis) and voltage drop (let axis) for the full chip analysis, as a function of the reduction factor.

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