Carbon-based Power Delivery Networks for nanoscale ICs: electrothermal performance analysis

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***Abstract*—This paper presents the electrothermal analysis of the performances of a Power Delivery Network for nanoscale integrated circuits, comparing standard (copper) with carbon nanotubes and graphene interconnects. Realistic carbon interconnects are considered, with the typical values of electrical and thermal parameters obtainable with the current fabrication technology. A temperature-dependent model for the electrical resistance is adopted, able to describe the case of negative temperature coefficient of the resistance, as it has been theoretically predicted and experimentally proved. The electrothermal analysis of the power network of a standard chip puts on evidence, for the first time, an interesting trade-off between voltage drop and temperature increase, while exploiting carbon nanotube and graphene based interconnects.**

Keywords— Carbon nanotube; Graphene; On-chip power distribution networks; electro-thermal analysis.

I. INTRODUCTION

Nanoscale Integrated Circuits (ICs) will contain billions of transistors, operating at tens of GHz [1]. A big issue for nanoscale Power Distribution Networks (PDNs) is the increase of the power supply current per circuit area, and of the transient current slew rate, yielding an ohmic and inductive voltage drop, respectively. Another major issue is the heat produced either by the Joule effect and by the power switching activity [2]. The heat production not only imposes strong design constraints for its efficient dissipation, but also yields a chip temperature rise. Higher temperature affects the electrical performance, given the temperature dependence of the electrical resistivity [3]. Accurate simulations of the behavior of PDNs are possible only with an electrothermal modeling, where the electrical and thermal behaviors are simultaneously dealt with, *e.g.* [4].

The dramatic increase of copper resistivity at nanoscale has suggested to replace copper in on-chip interconnects with carbon nanotubes (CNTs) or graphene nanoribbons (GNRs) [1]. The performance of carbon-based materials have been intensely investigated for signal interconnects [5]-[7]. Few works have been so far devoted to their use for power grids: in [5] a comparative analysis between Cu and CNT interconnects is carried out for a nanoscale on-chip PDN, whereas in [8]-[9] the analysis is extended to 3-D ICs. The cited works suggest that carbon interconnects may outperform Cu ones at the chip global level, provided that "good quality" interconnects are fabricated. This means: good control of alignment, chirality, dimension, and density, and low contact resistances at the interfaces carbon/metals. For instance, global level power interconnects require a minimum density of 1/2.5 nm^2, if made by single-walled CNTs (SWCNTs) [5], or a minimum length of 20 μm, if made by multi-walled CNTs (MWCNTs) [8].

Due to technological limits, the physical parameters of a realistic carbon interconnect sensibly differ from the remarkable values experimentally obtained for isolated samples. Indeed, isolated CNTs may exhibit ballistic electrical transport for lengths up to some μm, but in real CNT bundles the defects and the contacts may add huge parasitic resistances (of the order of 100 kΩ), hiding the effect of ballistic transport. Similarly, a huge thermal conductivity (3000-5000 W/mK) was reported for isolated CNTs or single GNRs, but this value drops to about 200 W/mK in CNT bundles [10] or GNR arrays [11]. The above considerations lead to the conclusion that the electrical performance of carbon interconnects are often overestimated. However, the greater stability of the resistance over temperature exhibited in some cases by a certain class of carbon lines, could be of great interest for PDNs. Indeed, a Temperature Coefficient of the Resistance (TCR) close to zero or even negative has been theoretically predicted [7] and experimentally reported [12]-[13]. This paper is devoted to study this effect, by means of an electrothermal analysis of a PDN, commonly structured as a multilayer grid, as in Fig. 1.

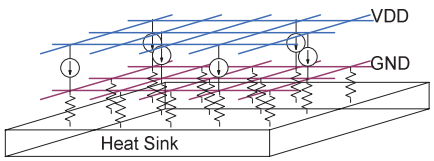

Fig. 1. Schematic of the considered PDN.

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II. Electro-Thermal Model

Let us refer to the two-grids PDN for ICs reported in Fig.1. The ground and power grids, separated by an insulation layer, are connected to VDD and GND supply pins, respectively, through a series resistance R_{supply} at the four corners in the basic stamp element. For heat dissipation, one side of the chip is connected to a heatsink.

The electrical problem is modeled by two regular grids, where the connectivity on a node is depicted in Fig.2(a): the temperature-dependent resistors $R(T)$ connect adjacent nodes of the same grid. The power and ground grids are connected by a current source J_0, which represents the circuit *activity*, i.e. the current demand of a circuit connected between VDD and GND pins. The solution of the electrical problem provides the *voltage drop* at any generic node i, defined as:

$$V_d(i) = V_{DD} - (V_n(i) - V_g(i)), \tag{1}$$

being $V_n(i)$ and $V_g(i)$ the node potentials with respect to the power and ground plane references, respectively.

The main sources of heat in PDNs are associated to the circuit activity and to the joule effects in the metal interconnects. A perfect duality between thermal and electric transport models exists, where the heat flow plays the role of an electrical current and the temperature difference corresponds to the electrical voltage. If we define a grid where the branch lengths are within the characteristic thermal length, we can adopt the same grid for the electrical and thermal problems, and define a unique thermal resistance between the nodes [14]. The generic node of the thermal network is shown in Fig.2(b): thermal resistances connect two nodes of the same grid, and the grids are connected by the equivalent sources modeling the heat generation $P_D(i)=J_0V_d(i)$ modeling the power produced at node "i" by effect of the voltage drop (1) and of the current J_0. An additional thermal resistance connect the node to the heatsink.

The equivalent thermal model is here analyzed in steady-state, assuming negligible heat diffusion in the dielectric. Thus, in each power track of the metal interconnects the temperature distribution $T(x)$ is solution of the 1-D heat diffusion equation:

$$\frac{d^2T(x)}{dx^2} = -\frac{g(x,T)}{k_m}, \tag{2}$$

where $g(x,T)$ is the power density of heat sources [W/m^3] and k_m is the thermal conductivity of the material [W/mK].

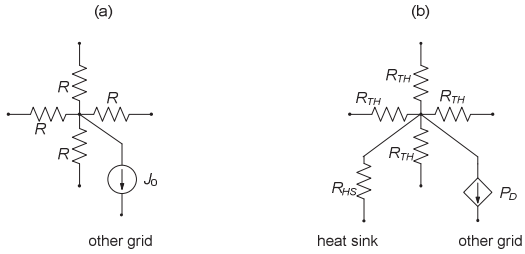


Fig. 2. Generic node of the grids for: (a) electrical, and (b) thermal model.

The coupled problems are solved in a classical relaxation approach: the thermal problem is first solved at room temperature, obtaining the distribution of T. Then the electrical resistances $R(T)$ are upgraded and the electrical circuit is solved, obtaining the voltage drop (1). After upgrading the thermal sources $P_D(i)$, the thermal problem is solved again, and so on. By establishing convergence between the problems, the final temperature and voltage drop distributions are obtained.

III. Temperature-Dependent Electrical Resistances

Let us first analyze the case when the PDN is made by conventional Cu interconnects. The electrical resistance of each track is commonly described by the linear law:

$$R(T) = R_0[1 + \beta(T - T_0)], \tag{3}$$

where $T_0 = 300$ K is the room temperature, R_0 is the resistance at $T = T_0$ and β is the temperature coefficient. Given the cross section dimensions of the conductors analyzed hereinafter in Section IV, we can consider the "bulk" copper parameters, i.e. a room temperature resistivity of $\rho_0 = 1.72 \cdot 10^{-8}$ [Ωm] and $\beta = 0.0039\text{K}^{-1}$. For nanoscale sizes (cross-section diameters smaller than about 100 nm), phenomena like electromigration and boundary and grain scattering lead to different values: at a line width of 14 nm, it would be $\rho_0 = 8.19 \cdot 10^{-8}$[Ωm], and $\beta = 0.012\text{K}^{-1}$ [7], [16].

Let us now consider the case of replacing the copper with a CNTs or GNRs. The electrical resistance of a single CNT or GNR of length l may be put in the form [7], [16]:

$$R(T) = \frac{R_Q + R_{con}}{M(T)} + \frac{R_Q}{2M(T)} \frac{l}{l_{mfp}(T)}, \tag{4}$$

where $R_Q = 12.9\,\text{k}\Omega$ is the quantum resistance, R_{con} is a lumped parasitic resistance due to non-ideal contacts, $l_{mfp}(T)$ is the mean free path and $M(T)$ is the total number of conducting channels. As for Cu, the mean free path $l_{mfp}(T)$ decreases as T increases, leading to increasing values of R. However, for a certain class of CNTs (MWCNTs) and for all the GNRs, the number of channels $M(T)$ is increasing with T. For some values of the line length, this effect counteracts the effect of $l_{mfp}(T)$, leading to negative values of $TCR = dR/RdT$. This theoretical behavior [7], [16] has been demonstrated in [12] and [13]: for instance, in [13] for MWCNT lengths up to some tens of microns it has been reported: $-19\,\text{m}\Omega/\text{K} < TCR < -4\,\text{m}\Omega/\text{K}$.

IV. Results

As a case study we refer to a PDN with the simple structure as in Fig.1, with each of the 4 electrical and thermal grids containing about 1 million nodes (i.e., a total of 4 millions nodes), that is a 20x20 replica of a basic structure of 51x51 nodes, as in [14]. Each single track has a length $l = 5.88\,\mu\text{m}$,

width $w = 2.67$ μm and height $H = 0.668$ μm. In addition, we assume $V_{DD} = 1$ V, R_{supply}=0.01 Ω, R_{HS}=100x R_{TH}.

Let us consider CNT interconnects, assuming that each track is filled by a bundle of MWCNTs, with outer diameter of 50 nm and filling factor of 80%. We assume the realistic case where only 1/3 of the CNT shells are metallic, and the other are semiconducting [10]. In addition, we include the effects of the contact resistance in (4). As for GNR interconnect, we assume an array made of GNRs of width W and length l. Also in this case, the percent of metallic GNRs is assumed to be 1/3.

Assuming the temperature-dependent model for M and $l_{mfp}(T)$ as in [7] and [16], we obtain for the given length a TRC<0 for CNTs and GNRs. However, the room temperature resistance R_0 is smaller for Cu: $R_{0,Cu} = 56$ mΩ, , while $R_{0,CNT} = 152.4$ mΩ, and $R_{0,GNR} = 1.19$ Ω.

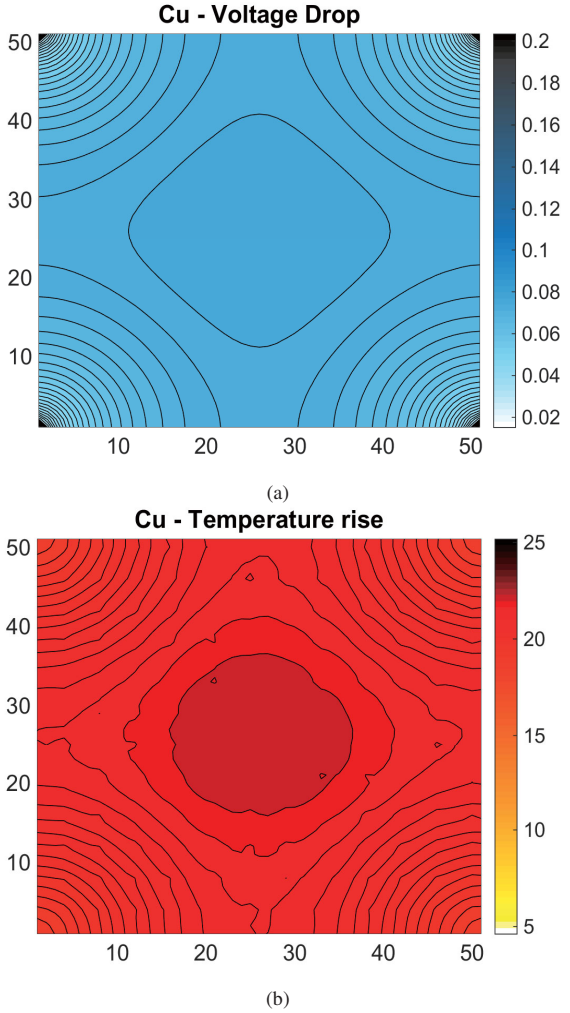
For this case-study, the temperature-behavior of R for carbon lines may be fitted by:

$$R(T) = \alpha_0 + \alpha_1 T + \alpha_2 T^2, \tag{5}$$

with the fitting coefficients a_i given in Table I.

TABLE I. FITTING COEEFICIENTS IN EQ. (5)

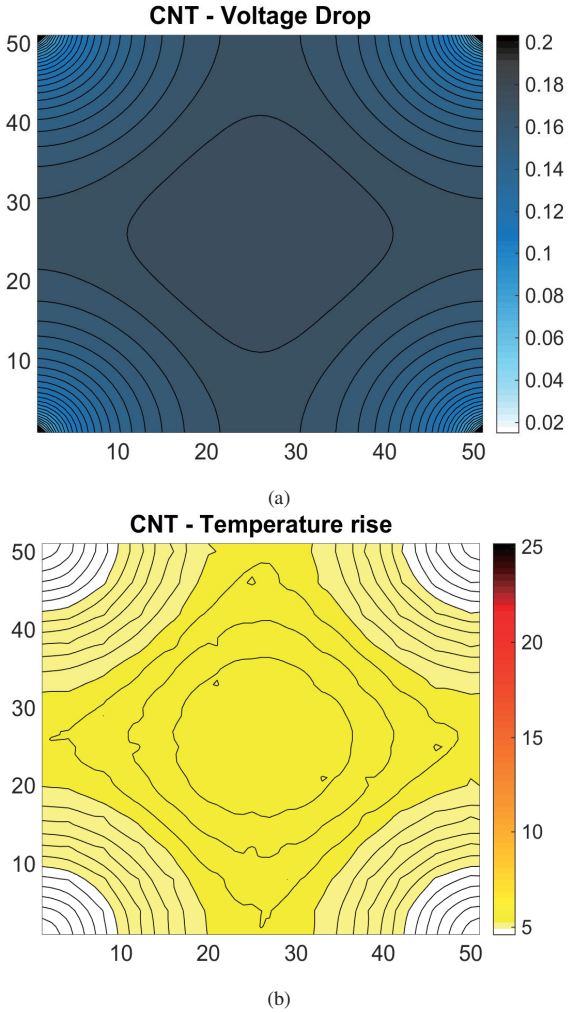
	α_0 [Ω]	α_1 [mΩ/K]	α_2 [μΩ/K^2]
CNT	0.42	-1.42	1.76
GNR	3.30	-10.15	10.42



(a)

(b)

Fig. 3 Maps for voltage drop (a) and incremental temperature (b) in a self consistent electrothermal solution fot the case of Copper.



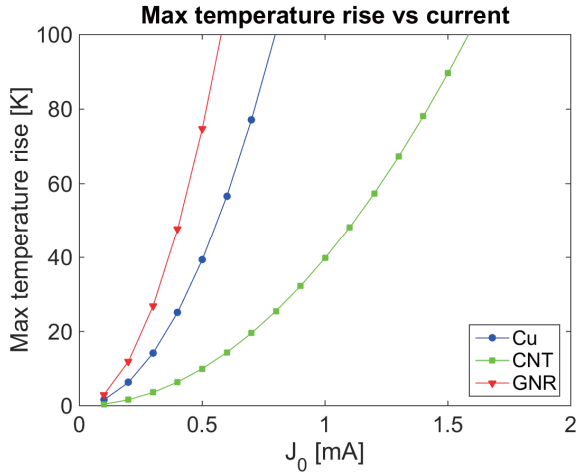
(a)

(b)

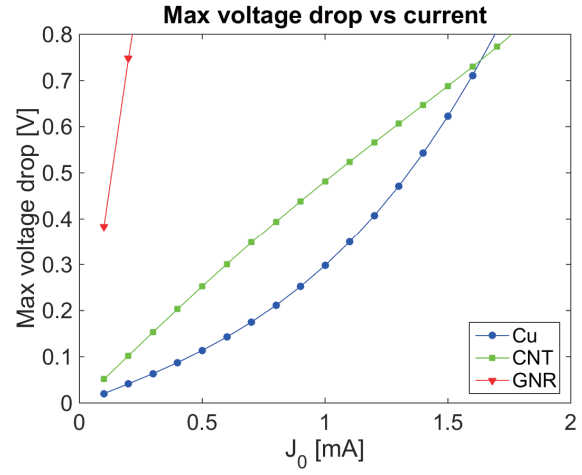
Fig. 4 Maps for voltage drop (a) and incremental temperature (b) in a self consistent electrothermal solution fot the case of Carbon Nanotubes.

As for the thermal resistance, assuming bulk value for thermal conductivity for copper, $R_{TH,Cu}$=8473K/W. Considering a realistic value of thermal conductivity of 200 W/mK, which has been experimentally reported for multi-CNTs or multi-GNRs [10]-[11], we get $R_{TH,CNT}$= $R_{TH,GNR}$ = 850 K/W.

A steady state analysis of the electro-thermal problem has been carried out, based on the efficient solution of the two (linear) sub-problems (electrical network at fixed temperature, thermal problem at fixed heat production rate), in a classical relaxation cycle for the self-consistent solution of the non linear joint problem [14]. As a first result, the voltage drop and thermal maps for the case of Cu (3a and 3b) and for the case of CNT (Fig.4a and Fig.4b) are shown, for the basic stamp structure at the center of the large grid, at the fixed value of the current I_0=0.4 mA.



(a)



(b)

Fig. 5. Max voltage drop (a) and max incremental temperature (b) as functions of current for copper, carbon nanotubes and graphene.

A more extended analysis, with different values of the current, is given in Fig. 5 also for GNR. It reveals, at realistic parameters values, an interesting trade-off between the voltage drop and the temperature rise for Cu and CNTs, leaving the GNR solution still non performant. This may open new scenarios for the design of nanoscale ICs PDNs.

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