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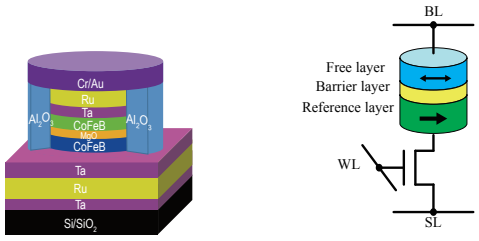
***Abstract*—As the integration density rockets up for contemporary VLSI circuits, power consumption limits the scalability of technology advancement of CMOS. Spin transfer torque-magnetic random access memory (STT-MRAM), as one of the emerging non-CMOS technologies, has the promising prospect of low standby power, fast access speed and compatibility with the CMOS fabrication process. However, with the technology node scaling down, typical 1 Transistor-1 Magnetic Tunnel Junction (1T-1MTJ) STT-RAM cell suffers from severe reliability challenges, especially for read operation under temperature fluctuation. In this paper, we quantitatively analyze the temperature effect on read reliability of STT-RAM cell and propose a novel body-biasing feedback readout circuit design to improve the read sensing margin under different temperatures. The experiments based on 40nm CMOS technology and MTJ compact model validate the effectiveness of the proposed method. The improved sensing margin also permits a smaller sensing current for reading such that higher read energy efficiency can be achieved.**

I. Introduction

Due to the endless pursuit for high performance computing, multi-core or many core system comes into play to exploit parallelism further. However, this design paradigm shifting also introduces well-known "dark silicon" effect and elevated leakage power, especially for memory systems.

Several emerging memory technologies, including STT-MRAM, Phase charge random access memory (PCRAM), memristor, etc., are proposed to mitigate the elevating power crisis. Among them, STT-MRAM is one of the most promising candidates to replace SRAM or DRAM thanks to its fast access speed, extremely low standby power and high integration density. Its promising prospect has already attracted many research efforts on exploring STT-MRAM potentials from device level to architecture level [1]–[5]. Most of them focus on write energy efficiency and write reliability issues. However, as the technology node continuously scales down, read current has to be smaller in order to refrain read disturbances. This makes the read sensing reliability a severe challenge for STT-RAM when the feature size shrinks below 50nm [6]. Moreover, STT-RAM has to meet the wide working temperature requirement ranging from room temperature to 125°C for commercial use. Therefore, it is also imperative to investigate the temperature impact on STT-RAM access behavior to make sure reliable data sensing over the whole temperature range. However, few research papers investigate this point, especially from the circuit design perspective, which motivates the work in this paper.



(a) (b)

Fig. 1: (a) The structure of MTJ (b) A typical schematic of 1T-1MTJ STT-RAM cell

In the paper, we first analyze megneto-resistive tunnel junction (MTJ) and transistor behavior for different temperatures. Then, we evaluate the thermal impact on the typical sensing circuit of 1T-1MTJ cell. Based on the above analyses, we propose a novel body-biasing sensing circuit design to improve the read sensing margin considering the temperature variation. The experimental results show that the sensing reliability can be enhanced compared to the typical read circuit. Moreover, the sensing energy efficiency can be improved significantly under the same sensing margin.

The rest of the paper is organized as follows. The preliminaries of STT-RAM access mechanism and related work are introduced in Section II. Section III analyzes the variations of MTJ and access transistor caused by temperature. After that, the temperature effect on read sensing margin of a typical sensing circuit is evaluated in the same section. Based on above analyses, a novel body-biasing feedback technique is proposed to improve the read sensing margin in Section IV. Experimental results are shown in Section V. Finally, Section VI concludes the paper.

II. Preliminaries and Related Work

MTJ is the core of STT-RAM cell. It mainly consists of an oxide insulating layer (e.g., MgO) sandwiched by two

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ferromagnetic layers (e.g., CoFeB) as shown in Fig. 1a. One of the two ferromagnetic layers is called pinned layer, whose magnetization is fixed. The other one is called free layer as its magnetization can be changed by injected spin-polarized current. Depending on the magnetization direction of free layer, MTJ can have two states. If the magnetization of free layer is the same as that of pinned layer, MTJ manifests low resistance, and stores '0'. Otherwise, it stores '1'. The typical 1T-1MTJ memory cell is plotted in Fig. 1b. When the wordline is activated, the MTJ state can be switched or sensed by applying appropriate spin polarized current between the bitline and source line.

There are already many papers investigating the reliability issues of STT-RAM from both device level and circuit level, such as [1]–[4], [7], [8]. Yue developed a compact model to capture switching behavior of MTJ. Chen et al. quantitatively investigated the process variation impact on the writing operation of 1T-1MTJ memory cell [7]. Shang et al. proposed a novel simulation method for STT-RAM based on SPICE [8]. As the MTJ feature size scales down further, the read margin will get narrower and read reliability will become the new threat for STT-RAM cell [6]. Although a few publications have proposed many circuit design techniques to enhance the read reliability, such as [2], [9], they do not consider the temperature impact on read reliability and may not effectively reduce the read error rate within the whole working temperature range.

III. Temperature Effect on Read Reliability of STT-RAM

Taking the 1T-1MTJ structure into consideration, both access transistor and MTJ device are influenced by temperature. Transistor driving ability degrades when temperature increases. In contrast, tunnel magneto-resistance (TMR), which equals to $(R_H - R_L)/R_L$, reduces with ascending temperature, which degrades reading performance and reliability [10]. Moreover, retention time of STT-RAM memory cell reduces with temperature increase, implying that it is more easier to switch the state of MTJ and incur severe read disturbance. Therefore, it is imperative to propose a read circuit design with thermal consideration such that it can work reliably across the whole operation temperature range. In the following subsections, the temperature effects on MTJ and transistor are analyzed respectively.

A. Temperature effect on MTJ

Temperature can affect switching probability of MTJ, which can be expressed as the following [10],

$$P_{sw} = 1 - e^{-\frac{t_p}{\tau}} \tag{1}$$

$$\tau = \tau_0 e^{\Delta(1-\frac{V}{V_{c0}})} \tag{2}$$

where P_{sw} is the switching probability of MTJ. t_p is the duration of applied voltage pulse. τ_0 is the thermal attempt time at 0K. Δ is the energy barrier of MTJ switching. V is the magnitude of applied voltage pulse. V_{c0} is the critical switching voltage of MTJ.

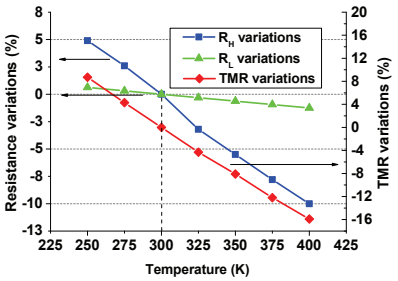

Fig. 2: MTJ resistance and TMR variations with temperature changes

Since Δ deciding the retention time of MTJ is inversely proportional to the temperature, the MTJ can be switched more easily in higher temperature. Therefore, the read disturbance will be more severe with ascending temperature.

As stated in [10], anti-parallel state resistance also varies with temperature while parallel state resistance roughly remains the same. According to [10], TMR is sensitive to the temperature changes as shown in Fig. 2. In the figure, resistance variation (R_v) can be calculated as,

$$R_V = (R_T - R_{T0})/R_{T0} \tag{3}$$

where R_{T0} is resistance at room temperature 300K, so R_V is set to zero for 300K. TMR variation can be calculated similarly. It indicates that anti-parallel resistance can degrade as much as 10% when temperature increases from 300K to 400K, and the TMR value reduces by 15.5%, which may degrade read sensing reliability significantly.

Based on above analyses, both energy barrier and sensing margin reduce with temperature increasing. On one hand, read disturbance may cause sensing error of STT-RAM cell. On the other hand, decreasing sensing margin may prolong sensing time and degrade sensing reliability.

B. Temperature effect on access transistor

Temperature not only affects the MTJ device, but also impacts the drivability of access transistor. Transistor variations with temperature have been investigated intensively. Since read voltage is much smaller than supply voltage, the transistor will work at linear region. Then, the driving current of transistor can be calculated as,

$$I_{ds} = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds} \tag{4}$$

where V_{ds} is the voltage difference between drain and source of access transistor. V_{gs} is the gate-source voltage. V_{th} is the threshold voltage. W is the width of transistor. L is the length of transistor. C_{ox} is gate oxide capacitance per unit area. μ is the carrier mobility of transistor, and depends on the temperature indicated by the following relation:

$$\mu(T) = \mu(T_r)(\frac{T}{T_r})^{-k_u} \tag{5}$$

In the above formula, $\mu(T_r)$ is the carrier mobility at room temperature, and k_u is a fitting parameter. From Eqs. (4) and

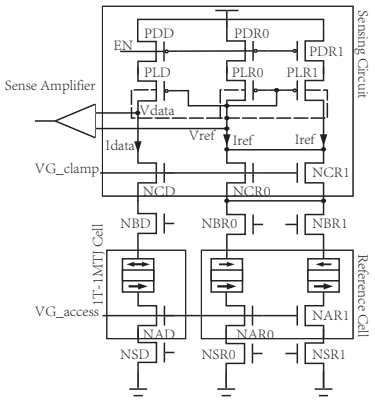

Fig. 3: The typical sensing circuit structure including conversion, clamping and sensing [9]

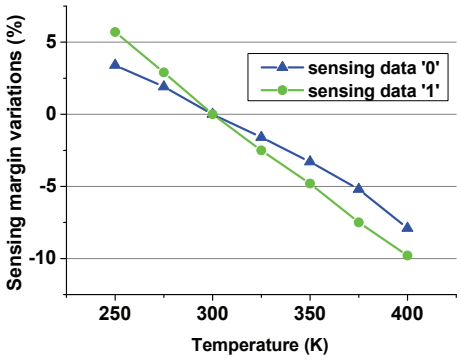

Fig. 4: Read sensing margin in different temperatures of the read circuit proposed in [9]

(5), we can derive that as the temperature increases, the driving current reduces due to the degraded carrier mobility.

C. Thermal induced sensing margin issues

The typical read circuit senses the data either by current or by voltage. In the paper, we take voltage sensing scheme as an example to analyze the temperature impact on sensing margin. The conclusion can also be extended for current sensing case as it also requires to convert sensing currents to voltages in the next sensing stage. As proposed in [9], a voltage sensing circuit usually consists of three basic parts, which is shown in Fig. 3. The first part senses the STT-RAM cell and reference cell. The second part is voltage clamping circuit to make sure the reference cell and memory cell being read have roughly the same voltage to make sure same sensing condition and prevent oxide layer from breaking down. The third part is the upload circuit to convert the sensing current to sensing voltage. After sensing the data and the reference cell, sensing voltages are then input to the secondary amplifier for amplification.

Although the simulation results showed the effectiveness of the proposed body-biasing method (as shown in dashed line in the figure), the authors did not consider the thermal fluctuation effect on MTJ and access transistor. As the temperature

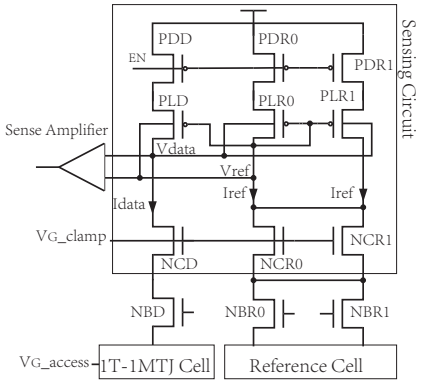

Fig. 5: The schematic of the proposed feedback body-biasing read circuit design

increases, TMR of MTJ and driving ability of access transistor degrade, and the sensing margin also reduces.

Fig. 4 shows the sensing margins of the read circuit proposed by [9] in different temperatures (refer Section V for detailed experimental setup information). As the figure shows, although the proposed sensing circuit can achieve a large read access pass yield in the 65-nm technology [9], the sense margin reduces about 15% when temperature rises from 250K to 400K, implying that read reliability deteriorates with ascending temperature.

IV. Body-biasing feedback circuit to improve read sensing margin

From the above analyses, we observe that sensing margin shrinks significantly with temperature. Note that the threshold voltage and transistor driving current can be tuned by source-body bias voltage. In the paper, we propose a body biasing feedback readout circuit design that can enlarge both reading '1' and '0' sensing margins by adjusting the body bias voltages of upload transistors. The schematic is shown in Fig. 5

In the proposed read circuit, the output data sensing voltage line directly connects to the bodies of the reference load transistors PLR0 and PLR1 whereas the output reference voltage feeds back to the body of data load transistor PLD. Accordingly, considering the body effect, the threshold voltage of upload PMOS transistor is given by the following equation,

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \qquad (6)$$

where V_{th0} is the threshold voltage for $V_{SB} = 0$, γ is the body effect coefficient, Φ_F is the surface potential, and $V_{SB} = V_S - V_B$ is the voltage difference between source and body.

If the data cell stores '0', i.e., the MTJ has a low resistance, I_{data0} will be larger than I_{ref}. Consequently, the voltage drop over branch consists of PLD and PDD is larger than those of PDR and PLR. Hence, V_{data0} will be lower than V_{ref}. Since source-body voltage of PLD is $V_{SBD} = V_S - V_{ref}$ while PLR has the source-body voltage of $V_{SBR} = V_S - V_{data0}$. Considering source voltages of PLD and PLR are roughly the same (approximately equal to V_{dd}), V_{SBD} would be smaller

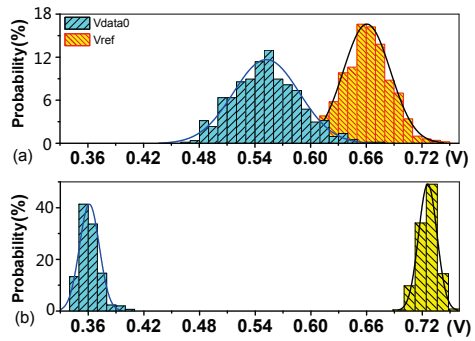

Fig. 6: The read and reference voltage distributions for the read circuit design in [9] and our proposed circuit under 300K

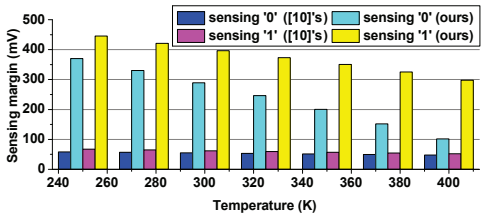

Fig. 7: Read sensing margin improvements by our proposed circuit design in different temperatures

than V_{SBR}. It implies that the increase of the PLR0/1 threshold voltage is larger than PLD. Therefore, PLR0/1 drivability is further reduced by the body-biasing voltage whereas the PDR drivability is relatively enhanced. As a result, the difference between data sensing voltage and reference voltage will be enlarged further. Hence, the read sensing margin is improved. Next, we consider the case when data '1' is stored in the cell. In this case, V_{data1} is larger than V_{ref}. With the body biasing, the sense margin also has a remarkable growth by the similar analysis.

V. Experimental Results

In the paper, the 1T-1MTJ memory cell is constructed using STMicroelectronics 40nm technology library and 40nm MTJ compact model from [4]. Cadence Spectre is the circuit simulation tool. In the simulation, both process and temperature variations are considered. 500 Monte-Carlo simulations are performed for each read circuit design in sensing margin evaluations.

Firstly, the sensing voltage distributions of the circuit proposed in [9] and our proposed circuit are shown in Fig. 6 for 300K temperature. The horizontal axis denotes the sensing voltage. The vertical axis denotes the sensing voltage probability distributions. From the figure, we can clearly observe that there is a significant overlapping between data and reference sensing voltage for the circuit used in [9] while the overlapping is completed eliminated for our proposed circuit, which means that the sensing margin and sensing reliability can be improved effectively.

Then, we plot the sensing margin comparisons in different temperatures in Fig. 7. As shown in the figure, sensing margins of our method are significantly higher than those of [9] over the whole range of temperature in consideration. On average, read '0' sensing margin is enlarged by about 5 times and read '1' sensing margin is improved by over 6 times. The enhanced sensing margin guarantees that the data can be reliably sensed even with the technology node scaling down further. On the other hand, if keep the read sensing margin the same, our method requires much smaller read sensing current compared to [9] (reducing from $14\mu A$ to $6\mu A$), meaning that the read energy efficiency can be improved dramatically under the same read sensing margin constraint.

VI. Conclusion

As the technology node shrinks, leakage power consumptions severely limit the integration density and maximum performance that can be achieved. STT-RAM is attracting much attention as one of the promising candidate for the next generation memory technology. However, it also faces several challenges needed to be dealt with before widespread commercialization. Among them, read reliability issue with thermal consideration is one emerging concern. In the paper, we analyze the thermal impact on 1T-1MTJ STT-RAM cell and propose a body-biasing feedback read sensing circuit design to enlarge the sensing margin and enhance the read reliability. Compared to the typical sensing circuit without thermal aware design, the simulation results validate the effectiveness of the proposed technique.

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