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Trace-driven simulation of multithreaded applications in gem5

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Cambridge, UK – September 11, 2017
Mont-Blanc 1, 2 & 3 projects (FP7, H2020)

- Getting ARM technology ready for HPC: HW, SW & Apps
- Advances in energy efficiency towards Exascale

Initial effort: using gem5 for performance prediction (2011)

- STE Nova A9500 SoC (dual-core Cortex A9)
- Fed publicly available parameters into a gem5 FS model
- 1.5% - 18% error, due to rough DRAM model and interconnect

Background motivations

Background motivations cont’d

- **Calibration against real hardware**
  - Using gem5 for performance prediction
  - And McPAT for power estimation

- **Then onto exploring fancy architecture configurations**
  - Heterogeneous single-ISA multicores à la big.LITTLE
  - Assymetric, 3 levels of heterogeneity etc.
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy? Any sweet spot?
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy?

```
<table>
<thead>
<tr>
<th></th>
<th>High</th>
<th>Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy</td>
<td>Cycle-accurate</td>
<td>Cycle-approximate</td>
</tr>
<tr>
<td>Speed</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>
```

1 core FS simulation

```
- CPU: 69%
- Cache: 15%
- Interconnect: 14%
- Memory: 2%
```

- Idea: Multicore Manycore Design Space Exploration - Simulation

- Mobile/Embedded technology
  - Power efficiency
  - Low cost
  - Performance?

- Supercomputer node
  - Intel Xeon E5 300 GFLOPS

- Samsung Exynos 5 Octa 9 GFLOPS
~ 70% simulation effort goes into CPU

- Abstracting away CPU cores sounds like a good idea
- Between 2 consecutive L1 cache misses (in-order) CPU cores perform « consistently »

![Diagram showing Trace-driven simulation principle](image-url)
**SimMATE: 2-stage process**

- Trace collection: tracing only L1 miss related transactions
- Trace replay: Using trace injectors that initiate transactions as previously recorded
SimMATE for faster DSE

- **Trace collection = freezing**
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- **Trace replay allows exploring the rest**
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed

---

![Diagram showing Trace Collection and Trace Simulation]

**Trace Collection**
- Core 0
- Core n
- Interconnect
- Memory

**Trace Simulation**
- TI 0
- TI n
- Interconnect
- Memory
- L2

**Legend:**
- 1 time
- Multiple times

---

**SimMATE for faster DSE**

- Trace collection = freezing
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- Trace replay allows exploring the rest
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed
Trace replay performs event (re-) scheduling

- Simple « time shifting » approach
- Maintaining constant compute phases
SimMATE Benchmarking

- **Tuning DRAM latency**
  - Collection performed with 30ns
  - TD simulation from 5ns to 55ns
  - FS used as reference

### Execution time error [%]

<table>
<thead>
<tr>
<th>Interconnect Memory</th>
<th>MJPEG</th>
<th>FFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5ns</td>
<td>0.6%</td>
<td>2.8%</td>
</tr>
<tr>
<td>15ns</td>
<td>0.5%</td>
<td>4.5%</td>
</tr>
<tr>
<td>30ns</td>
<td>0.1%</td>
<td>5.8%</td>
</tr>
<tr>
<td>45ns</td>
<td>0.4%</td>
<td>5.1%</td>
</tr>
<tr>
<td>55ns</td>
<td>0.4%</td>
<td>6.0%</td>
</tr>
</tbody>
</table>

Original
Tuning L2 size

- Collection performed without L2
- TD simulation from 0 to 16MB L2
- Errors originate from Cold-start bias / cache warmup

Execution time error [%]

Traces: ET ET+init ET+OS boot

<table>
<thead>
<tr>
<th>L2 cache size</th>
<th>Original</th>
<th>256kB</th>
<th>1MB</th>
<th>8MB</th>
<th>16MB</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2 cache size</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Execution time error</td>
<td>15%</td>
<td>8% 8%</td>
<td>7,5%</td>
<td>18%</td>
<td>14% 10%</td>
</tr>
<tr>
<td>0,1%</td>
<td>8%</td>
<td>7,5%</td>
<td>1% 0,3%</td>
<td>14%</td>
<td>10%</td>
</tr>
</tbody>
</table>

SimMATE Benchmarking
Having these traces collected makes it easy to:

- Perform «Trace replication» i.e. emulate more CPU cores for scalability study
- This corresponds to *weak scaling* experiments, i.e. *per-core* workload remains same
Multithreaded applications

■ Yet synchronizations must be accounted for!
  ● Using whatever API: POSIX threads, OpenMP 3.0 …
  ● Approach: embed synchronizations into traces
  ● Have an arbiter that takes care of locking (when barrier reached) and unlocking TIs
Limitation: in-order only!

- And most ARM AP are OoO (Out-of-Order)
  - Meaning multiple outstanding memory transactions
  - The assumption of constant time btw. 2 misses does not hold

- big-LITTLE & other heterogeneous friends everywhere
  - And there microarchitecture details cannot be overlooked
Elastic Traces: Trace-driven simulation for OoO

- Modeling micro-architecture timing & dependencies
  - Tracing with O3 model + probes, without L2 cache
  - Replay done in a smart « elastic » fashion

One simulation run: capture trace

Design space exploration: replay same trace

http://gem5.org/TraceCPU
Elastic Traces: Trace-driven simulation for OoO

**Smart TraceCPU**

- Updating a dependency graph pushing ready instructions into a queue for issue

http://gem5.org/TraceCPU
SimMATE + Elastic Traces = ElasticSimMATE

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.
Proper tracing of synchronizations

- API-dependant: OpenMP 3.x
- Tracing whenever entering or leaving parallel region, barrier etc.

```c
#pragma omp parallel
for(i=0;i<n;i++) {
  /* do_some work */
}
```

```c
for(i=0;i<n;i++) {
  OMP_runtime_call()
  /* do_some work */
}
```

```
Tick  PC  th_id type  IC  DC
389178 177216 0 1 1081157 165738 ...
```
ESM flow wrapup

- Using BSC Mercurium compiler / Nanos++ runtime
- Tweaked runtime such that custom m5 pseudo instructions produce trace records

```cpp
#pragma omp parallel
for(i=0;i<n;i++) {
    /* do_something */
}
```

**Diagram:**
- **Unmodified sources**
  - #pragma omp parallel
  - for(i=0;i<n;i++) {
  - /* do_something */
  - }

- **Nanos++ runtime**
  - nanos_create_team();
  - /* do_something */
  - nanos_end_team();

- **App Binaries**
  - #pragma omp parallel{
  - for(i=0;i<n;i++){
  - nanos_create_team();
  - /* do_something */
  - nanos_end_team();
  - }
  - }

- **Generated Traces**
  - Instruction
  - Dependency
  - Synchronization

- **gem5 Trace Collection**
  - Trace Replay
Benchmarking

- **Two main use cases:**
  - Fast parameter exploration
  - Scalability study: « trace replication »

- **Speedup & accuracy?**
  - Experiments on Rodinia application kernels

---

**Graphs and Tables:**

- **Execution Time [s] vs L2 Cache Size**
  - FS, ET, ESM

- **Error Percentage [%] vs L2 Cache Size**
  - FS vs ET, FS vs ESM

---

1 core **HOTSPOT**
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

![Graph showing execution time and error percentage vs L2 cache size for different conditions.](image)
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

**Speedup & accuracy?**

- Experiments on Rodinia application kernels

![Graph showing execution time and error percentage for different L2 cache sizes.](image)

**1 core**

**CANNEAL**
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

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**Benchmarking**

- Fast parameter exploration
- Scalability study: « trace replication »

**Speedup & accuracy?**
- Experiments on Rodinia application kernels

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**L2 Cache Miss Rate [%]**

- **L2 Cache Size:** 16kB, 128kB, 512kB, 1MB, 2MB

**L2 Cache Overall Miss Latency [Cycles]**

- **L2 Cache Size:** 16kB, 128kB, 512kB, 1MB, 2MB

---

**KMEANS**
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

Benchmarking

Execution Time [s]

Simulation Time [min]

Blackscholes
Hotspot

128 cores
KMEANS
Perspectives

- **Scalability analysis has limits**
  - Requires additional features s.a. **address offsetting**
  - **Weak scaling** only (replicated per-core workloads)

- **Programming models moving from loops to tasks**
  - OpenMP 4.0, OmpSs
  - Still pragma-based
  - More parallelisms available at run-time … more opportunities for smart job scheduling

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BSC OmpSs: Cholesky decomposition
Unbinding traces from cores

- One trace per Task, not per core!
- Assign traces to cores by emulating runtime behaviour in trace replay
- This is real strong scaling

**Trace collection**

**Trace simulation**
Current ESM prototype
- ~5x - 10x speedup for low core count, probably more for tens / thousands
- Nice solution for fast DSE
- Remaining accuracy issues for some applications
  - Common to ESM & Elastic Traces
  - Under investigation with ARM

Use cases
- Exploration of memory subsystem
- Some microarchitecture parameters (Elastic Traces)
- ...

Future directions
- Ruby compatibility
- Could be combined with other initiatives (dist-gem5)
- Can be extended to other PM / APIs (Tasking, MPI…)

Conclusion

http://montblanc-project.eu