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Trace-driven simulation of multithreaded applications in gem5

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Background motivations

- **Mont-Blanc 1, 2 & 3 projects (FP7, H2020)**
  - Getting ARM technology ready for HPC: HW, SW & Apps
  - Advances in energy efficiency towards Exascale

- **Initial effort: using gem5 for performance prediction (2011)**
  - STE Nova A9500 SoC (dual-core Cortex A9)
  - Fed publicly available parameters into a gem5 FS model
  - 1.5% - 18% error, due to rough DRAM model and interconnect

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Background motivations cont’d

- Calibration against real hardware
  - Using gem5 for performance prediction
  - And McPAT for power estimation

- Then onto exploring fancy architecture configurations
  - Heterogeneous single-ISA multicores à la big.LITTLE
  - Assymetric, 3 levels of heterogeneity etc.
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy? Any sweet spot?
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy?

![Diagram showing tradeoff between accuracy and speed for simulation methods like Cycle-accurate, Cycle-approximate, Distributed, Trace-driven, and JIT.]
~ 70% simulation effort goes into CPU

- Abstracting away CPU cores sounds like a good idea
- Between 2 consecutive L1 cache misses (in-order) CPU cores perform "consistently"
SimMATE: 2-stage process

- Trace collection: tracing only L1 miss related transactions
- Trace replay: Using trace injectors that initiate transactions as previously recorded
SimMATE for faster DSE

- **Trace collection = freezing**
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- **Trace replay allows exploring the rest**
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed

![Diagram showing Trace Collection and Trace Simulation](image)

- **Trace Collection**
  - Core 0 \(\rightarrow\) Interconnect \(\rightarrow\) Memory
  - Core \(n\) \(\rightarrow\) Interconnect \(\rightarrow\) Memory

- **Trace Simulation**
  - TI 0 \(\rightarrow\) Interconnect \(\rightarrow\) Memory
  - TI \(n\) \(\rightarrow\) Interconnect \(\rightarrow\) Memory

- **Misses**
  - Core 0: $\rightarrow$ Misses
  - Core \(n\): $\rightarrow$ Misses
  - TI 0: $\rightarrow$ Misses
  - TI \(n\): $\rightarrow$ Misses

- **Memory traces**
  - Core 0 \(\rightarrow\) Memory
  - Core \(n\) \(\rightarrow\) Memory
  - TI 0 \(\rightarrow\) Memory
  - TI \(n\) \(\rightarrow\) Memory

- **Simulation**
  - 1 time
  - Multiple times
Trace replay performs event (re-) scheduling

- Simple « time shifting » approach
- Maintaining constant compute phases

Memory & Interconnect

$TI$

$T_{R1}$

$T_{A1}$

$T_{A1}'$

$T_{R2}'$

Time

communication
SimMATE Benchmarking

- **Tuning DRAM latency**
  - Collection performed with 30ns
  - TD simulation from 5ns to 55ns
  - FS used as reference

![Diagram showing execution time error in different scenarios](image)

**Execution time error [%]**

- **MJPEG**
  - 0.6% at 5ns
  - 0.5% at 15ns
  - 0.1% at 30ns
  - 0.4% at 45ns
  - 0.4% at 55ns

- **FFT**
  - 2.8% at 5ns
  - 4.5% at 15ns
  - 5.8% at 30ns
  - 5.1% at 45ns
  - 6% at 55ns

Original
Tuning L2 size

- Collection performed without L2
- TD simulation from 0 to 16MB L2
- Errors originate from Cold-start bias / cache warmup

Execution time error [%]

Traces: ET ET+init ET+OS boot

<table>
<thead>
<tr>
<th>L2 cache size</th>
<th>ET</th>
<th>ET+init</th>
<th>ET+OS boot</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original</td>
<td>0.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>256kB</td>
<td>8%</td>
<td>8%</td>
<td></td>
</tr>
<tr>
<td>1MB</td>
<td>7.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8MB</td>
<td>18%</td>
<td>14%</td>
<td>10%</td>
</tr>
<tr>
<td>16MB</td>
<td>15%</td>
<td>8%</td>
<td>7%</td>
</tr>
</tbody>
</table>

SimMATE Benchmarking
Multithreaded applications

- Having these traces collected makes it easy to:
  - Perform « Trace replication » i.e. emulate more CPU cores for scalability study
  - This corresponds to weak scaling experiments, i.e. per-core workload remains same

![Diagram of Trace Collection and Trace Simulation]

**Number of Cache Misses**

- Core 0/Thread 0
- Core 1/Thread 1
Multithreaded applications

- Yet synchronizations must be accounted for!
  - Using whatever API: POSIX threads, OpenMP 3.0 …
  - Approach: embed synchronizations into traces
  - Have an arbiter that takes care of locking (when barrier reached) and unlocking TIs
Limitation: in-order only!

- And most ARM AP are OoO (Out-of-Order)
  - Meaning multiple outstanding memory transactions
  - The assumption of constant time btw. 2 misses does not hold

- big-LITTLE & other heterogeneous friends everywhere
  - And there microarchitecture details cannot be overlooked

![Diagram showing different CPU frequencies and their performance aspects]
Elastic Traces: Trace-driven simulation for OoO

- Modeling micro-architecture timing & dependencies
  - Tracing with O3 model + probes, without L2 cache
  - Replay done in a smart « elastic » fashion

http://gem5.org/TraceCPU
Smart TraceCPU

- Updating a dependency graph pushing ready instructions into a queue for issue

http://gem5.org/TraceCPU
SimMATE + Elastic Traces = ElasticSimMATE

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**SimMATE + Elastic Traces = ElasticSimMATE**

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**ElasticSimMATE (ESM)**

- SimMATE + Elastic Traces = ElasticSimMATE
- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**SimMATE + Elastic Traces = ElasticSimMATE**

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**SimMATE + Elastic Traces = ElasticSimMATE**

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.
ElasticSimMATE (ESM)

- Proper tracing of synchronizations
  - API-dependant: OpenMP 3.x
  - Tracing whenever entering or leaving parallel region, barrier etc.

```c
#pragma omp parallel
for(i=0;i<n;i++) {
  /* do_some work */
}
for(i=0;i<n;i++) {
  OMP_runtime_call()
  /* do_some work */
}
```

```
Tick   PC  th_id  type  IC    DC
389178 177216 0   1    1081157 165738 ...
```
ESM flow wrapup

- Using BSC Mercurium compiler / Nanos++ runtime
- Tweaked runtime such that custom m5 pseudo instructions produce trace records
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels
### Benchmarking

- **Two main use cases:**
  - Fast parameter exploration
  - Scalability study: « trace replication »

- **Speedup & accuracy?**
  - Experiments on Rodinia application kernels

![Graph showing execution time vs L2 cache size](image)

![Graph showing error percentage vs L2 cache size](image)
Two main use cases:

- Fast parameter exploration
- Scalability study: «trace replication»

Speedup & accuracy?

- Experiments on Rodinia application kernels
**Two main use cases:**
- Fast parameter exploration
- Scalability study: « trace replication »

**Speedup & accuracy?**
- Experiments on Rodinia application kernels

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**Benchmarking**

![Graphs showing L2 Cache Miss Rate and Overall Miss Latency](image_url)
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

Benchmarking

![Graph showing execution time vs. number of cores for Blackscholes and Hotspot.]

128 cores KMEANS
Scalability analysis has limits
- Requires additional features s.a. **address offsetting**
- **Weak scaling** only (replicated per-core workloads)

Programming models moving from loops to tasks
- OpenMP 4.0, OmpSs
- Still pragma-based
- More parallelisms available at run-time … more opportunities for smart job scheduling

**BSC OmpSs: Cholesky decomposition**
Unbinding traces from cores
- One trace per Task, not per core!
- Assign traces to cores by emulating runtime behaviour in trace replay
- This is real strong scaling

Trace collection

Trace simulation
Current ESM prototype

- ~5x - 10x speedup for low core count, probably more for tens / thousands
- Nice solution for fast DSE
- Remaining accuracy issues for some applications
  - Common to ESM & Elastic Traces
  - Under investigation with ARM

Use cases

- Exploration of memory subsystem
- Some microarchitecture parameters (Elastic Traces)
- …

Future directions

- Ruby compatibility
- Could be combined with other initiatives (dist-gem5)
- Can be extended to other PM / APIs (Tasking, MPI…)

Conclusion