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Trace-driven simulation of multithreaded applications in gem5

Gilles SASSATELLI
sassatelli@lirmm.fr

Alejandro NOCUA, Florent BRUGUIER, Anastasiia BUTKO

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Background motivations

- **Mont-Blanc 1, 2 & 3 projects (FP7, H2020)**
  - Getting ARM technology ready for HPC: HW, SW & Apps
  - Advances in energy efficiency towards Exascale

- **Initial effort: using gem5 for performance prediction (2011)**
  - STE Nova A9500 SoC (dual-core Cortex A9)
  - Fed publicly available parameters into a gem5 FS model
  - 1.5% - 18% error, due to rough DRAM model and interconnect

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Background motivations cont’d

- Calibration against real hardware
  - Using gem5 for performance prediction
  - And McPAT for power estimation

- Then onto exploring fancy architecture configurations
  - Heterogeneous single-ISA multicores à la big.LITTLE
  - Assymetric, 3 levels of heterogeneity etc.
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy? Any sweet spot?
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy?

![Diagram showing the trade-off between accuracy and speed for different simulation methods.](image)

1 core FS simulation

- CPU: 69%
- Cache: 15%
- Interconnect: 14%
- Memory: 2%

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- Mobile/Embedded technology
  - Power efficiency
  - Low cost
  - Performance
- Samsung Exynos 5 Octa 9 GFLOPS
- Supercomputer node
  - Intel Xeon E5 300 GFLOPS

Idea
- Multicore Manycore
- Design Space Exploration - Simulation State-of-the-art

Accuracy vs. Speed

- RTL: Cycle-accurate, Low Speed, High Accuracy
- Distributed: Trace-driven, High Speed, Low Accuracy
- JIT: High Speed, High Accuracy

10s MIPS 1 core FS simulation
Trace-driven simulation principle

- ~ 70% simulation effort goes into CPU
  - Abstracting away CPU cores sounds like a good idea
  - Between 2 consecutive L1 cache misses (in-order) CPU cores perform « consistently »

Diagram:
- Memory
- Cache
- CPU
- Time
- Trace
- FS simulation

MONTBLANC
SimMATE: 2-stage process

- Trace collection: tracing only L1 miss related transactions
- Trace replay: Using trace injectors that initiate transactions as previously recorded
SimMATE for faster DSE

- **Trace collection = freezing**
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- **Trace replay allows exploring the rest**
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed

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[Diagram showing trace collection and simulation processes]

**Trace Collection**

- Core 0
- Core n
- Interconnect
- Memory

**Trace Simulation**

- TI 0
- TI n
- Interconnect
- Memory
- L2

I time  
Multiple times
Trace replay performs event (re-) scheduling

- Simple « time shifting » approach
- Maintaining constant compute phases

Memory & Interconnect

$\text{TI 0} \quad ... \quad \text{TI n}$

Interconnect

Memory

L2

Time

$T_{R1}$

$T_{A1}$

$T_{A1}'$

$T_{R2}'$

communication

delay

delay
Tuning DRAM latency

- Collection performed with 30ns
- TD simulation from 5ns to 55ns
- FS used as reference

Execution time error [%]

<table>
<thead>
<tr>
<th></th>
<th>MJPEG</th>
<th>FFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5ns</td>
<td>0.6%</td>
<td>2.8%</td>
</tr>
<tr>
<td>15ns</td>
<td>0.5%</td>
<td>4.5%</td>
</tr>
<tr>
<td>30ns</td>
<td>0.1%</td>
<td>5.8%</td>
</tr>
<tr>
<td>45ns</td>
<td>0.4%</td>
<td>5.1%</td>
</tr>
<tr>
<td>55ns</td>
<td>0.4%</td>
<td>6.0%</td>
</tr>
</tbody>
</table>

Original
Tuning L2 size

- Collection performed without L2
- TD simulation from 0 to 16MB L2
- Errors originate from Cold-start bias / cache warmup

Execution time error [%]

Traces:  
- ET
- ET+init
- ET+OS boot

Original | 256kB | 1MB | 8MB | 16MB
---|---|---|---|---
ET | 15% | 18% | 15% | 8% | 7%
ET+init | 8% | 10% | 8% | 8% | 7%
ET+OS boot | 1% | 0.3% | 1% | 0.1% | 1%
Having these traces collected makes it easy to:

- Perform « Trace replication » i.e. emulate more CPU cores for scalability study
- This corresponds to weak scaling experiments, i.e. per-core workload remains same
Yet synchronizations must be accounted for!

- Using whatever API: POSIX threads, OpenMP 3.0 …
- Approach: embed synchronizations into traces
- Have an arbiter that takes care of locking (when barrier reached) and unlocking TIs
Limitation: in-order only!

- And most ARM AP are OoO (Out-of-Order)
  - Meaning multiple outstanding memory transactions
  - The assumption of constant time btw. 2 misses does not hold

- big-LITTLE & other heterogeneous friends everywhere
  - And there microarchitecture details cannot be overlooked
Modeling micro-architecture timing & dependencies

- Tracing with O3 model + probes, without L2 cache
- Replay done in a smart « elastic » fashion

Elastic Traces: Trace-driven simulation for OoO

One simulation run: capture trace

Design space exploration: replay same trace

http://gem5.org/TraceCPU
Smart TraceCPU

- Updating a dependency graph pushing ready instructions into a queue for issue
SimMATE + Elastic Traces = ElasticSimMATE

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**ElasticSimMATE (ESM)**

**SimMATE + Elastic Traces = ElasticSimMATE**

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.
Proper tracing of synchronizations

- API-dependant: OpenMP 3.x
- Tracing whenever entering or leaving parallel region, barrier etc.

```c
#pragma omp parallel
for(i=0;i<n;i++) {
    /* do_some work */
}
```

```c
for(i=0;i<n;i++) {
    OMP_runtime_call()
    /* do_some work */
}
```

```
Tick  PC  th_id  type  IC    DC
389178 177216 0  1  1081157 165738
...```

1.bin

OMP runtime + scheduler

MS

MH
ESW wrapup

- ESM flow wrapup
  - Using BSC Mercurium compiler / Nanos++ runtime
  - Tweaked runtime such that custom m5 pseudo instructions produce trace records
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

![Bar chart showing execution time for different L2 cache sizes](chart1.png)

![Line chart showing error percentage for different L2 cache sizes](chart2.png)
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

Benchmarks for KMEANS:

- Execution Time [ms]
- Error Percentage [%]
- L2 Cache Size
Benchmarking

- Two main use cases:
  - Fast parameter exploration
  - Scalability study: « trace replication »

- Speedup & accuracy?
  - Experiments on Rodinia application kernels
Two main use cases:
● Fast parameter exploration
● Scalability study: « trace replication »

Speedup & accuracy?
● Experiments on Rodinia application kernels

**Benchmarking**

<table>
<thead>
<tr>
<th>L2 Cache Size</th>
<th>L2 Cache Miss Rate [%]</th>
<th>L2 Cache Overall Miss Latency [Cycles]</th>
</tr>
</thead>
<tbody>
<tr>
<td>16kB</td>
<td>FS</td>
<td>ESM</td>
</tr>
<tr>
<td>128kB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>512kB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Two main use cases:
- Fast parameter exploration
- Scalability study: «trace replication»

Speedup & accuracy?
- Experiments on Rodinia application kernels

Benchmarking

128 cores KMEANS
Scalability analysis has limits
- Requires additional features s.a. **address offsetting**
- **Weak scaling** only (replicated per-core workloads)

Programming models moving from loops to tasks
- OpenMP 4.0, OmpSs
- Still pragma-based
- More parallelisms available at run-time … more opportunities for smart job scheduling

BSC OmpSs: Cholesky decomposition
Unbinding traces from cores

- One trace per Task, not per core!
- Assign traces to cores by emulating runtime behaviour in trace replay
- This is real strong scaling

Trace collection

Trace simulation
Current ESM prototype

- ~5x - 10x speedup for low core count, probably more for tens / thousands
- Nice solution for fast DSE
- Remaining accuracy issues for some applications
  - Common to ESM & Elastic Traces
  - Under investigation with ARM

Use cases

- Exploration of memory subsystem
- Some microarchitecture parameters (Elastic Traces)
- ...

Future directions

- Ruby compatibility
- Could be combined with other initiatives (dist-gem5)
- Can be extended to other PM / APIs (Tasking, MPI...)