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Trace-driven simulation of multithreaded applications in gem5

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Alejandro NOCUA, Florent BRUGUIER, Anastasiia BUTKO

Cambridge, UK – September 11, 2017
Background motivations

- Mont-Blanc 1, 2 & 3 projects (FP7, H2020)
  - Getting ARM technology ready for HPC: HW, SW & Apps
  - Advances in energy efficiency towards Exascale

- Initial effort: using gem5 for performance prediction (2011)
  - STE Nova A9500 SoC (dual-core Cortex A9)
  - Fed publicly available parameters into a gem5 FS model
  - 1.5% - 18% error, due to rough DRAM model and interconnect

Background motivations cont’d

- **Calibration against real hardware**
  - Using **gem5** for performance prediction
  - And **McPAT** for power estimation

- **Then onto exploring fancy architecture configurations**
  - Heterogeneous single-ISA multicores *à la* big.LITTLE
  - Assymetric, 3 levels of heterogeneity etc.
Background motivations cont’d

- **Not ready for manycores, too slow!**
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- **Trading speed for accuracy? Any sweet spot?**
Not ready for manycores, too slow!

- 1K-1M (simulated) IPS
- Scales bad with system size
- Already much better than RTL though

Trading speed for accuracy?

Background motivations cont’d
Trace-driven simulation principle

~ 70% simulation effort goes into CPU

- Abstracting away CPU cores sounds like a good idea
- Between 2 consecutive L1 cache misses (in-order) CPU cores perform « consistently »
SimMATE

- **SimMATE: 2-stage process**
  - Trace collection: tracing only L1 miss related transactions
  - Trace replay: Using trace injectors that initiate transactions as previously recorded
SimMATE for faster DSE

- **Trace collection = freezing**
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- **Trace replay allows exploring the rest**
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed

---

**Trace Collection**

- Core 0
- Core n

**Trace Simulation**

- TI 0
- TI n

<table>
<thead>
<tr>
<th>Hits &amp; Misses</th>
<th>Memory traces</th>
<th>Memory traces</th>
</tr>
</thead>
<tbody>
<tr>
<td>$ $ $ $</td>
<td>Misses</td>
<td>Misses</td>
</tr>
</tbody>
</table>

1 time

Multiple times
SimMATE for faster DSE cont’d

- Trace replay performs event (re-) scheduling
  - Simple « time shifting » approach
  - Maintaining constant compute phases

<table>
<thead>
<tr>
<th>Memory &amp; Interconnect</th>
<th>$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TI</td>
<td></td>
</tr>
</tbody>
</table>

Time

\[ T_R1 \quad T_A1 \quad T_A1' \quad T_R2' \]

communication delay delay
SimMATE Benchmarking

- **Tuning DRAM latency**
  - Collection performed with 30ns
  - TD simulation from 5ns to 55ns
  - FS used as reference

**Execution time error [%]**

<table>
<thead>
<tr>
<th></th>
<th>MJPEG</th>
<th>FFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5ns</td>
<td>0,6%</td>
<td>2,8%</td>
</tr>
<tr>
<td>15ns</td>
<td>0,5%</td>
<td>4,5%</td>
</tr>
<tr>
<td>30ns</td>
<td>0,1%</td>
<td>5,8%</td>
</tr>
<tr>
<td>45ns</td>
<td>0,4%</td>
<td>5,1%</td>
</tr>
<tr>
<td>55ns</td>
<td>0,4%</td>
<td>6%</td>
</tr>
</tbody>
</table>

**Ti0**

**Trace Collection**

**TD Simulation**
- 5 ns
- 15 ns
- 45 ns
- 55 ns

**FS Simulation**
- 5 ns
- 15 ns
- 45 ns
- 55 ns

**Interconnect**
**Memory**
Tuning L2 size

- Collection performed without L2
- TD simulation from 0 to 16MB L2
- Errors originate from Cold-start bias / cache warmup

Execution time error [%]

Traces: ET, ET+init, ET+OS boot

<table>
<thead>
<tr>
<th>L2 cache size</th>
<th>ET</th>
<th>ET+init</th>
<th>ET+OS boot</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original</td>
<td>15%</td>
<td>8%</td>
<td>7,5%</td>
</tr>
<tr>
<td>256kB</td>
<td>18%</td>
<td>10%</td>
<td>8%</td>
</tr>
<tr>
<td>1MB</td>
<td>14%</td>
<td>8%</td>
<td>7%</td>
</tr>
<tr>
<td>8MB</td>
<td>15%</td>
<td>8%</td>
<td>7%</td>
</tr>
<tr>
<td>16MB</td>
<td>15%</td>
<td>8%</td>
<td>7%</td>
</tr>
</tbody>
</table>

L2 cache size
**Multithreaded applications**

- Having these traces collected makes it easy to:
  - Perform « Trace replication » i.e. emulate more CPU cores for scalability study
  - This corresponds to *weak scaling* experiments, i.e. *per-core* workload remains same

![Diagram of Trace Collection and Simulation](image)

**Number of Cache Misses**

- Core 0/Thread 0
- Core 1/Thread 1
Yet synchronizations must be accounted for!

- Using whatever API: POSIX threads, OpenMP 3.0 …
- Approach: embed synchronizations into traces
- Have an arbiter that takes care of locking (when barrier reached) and unlocking TIs
Limitation: in-order only!

- And most ARM AP are OoO (Out-of-Order)
  - Meaning multiple outstanding memory transactions
  - The assumption of constant time btw. 2 misses does not hold

- big-LITTLE & other heterogeneous friends everywhere
  - And there microarchitecture details cannot be overlooked
Elastic Traces: Trace-driven simulation for OoO

- Modeling micro-architecture timing & dependencies
  - Tracing with O3 model + probes, without L2 cache
  - Replay done in a smart « elastic » fashion

http://gem5.org/TraceCPU
Elastic Traces: Trace-driven simulation for OoO

- **Smart TraceCPU**
  - Updating a dependency graph pushing ready instructions into a queue for issue

[Diagram of TraceCPU operations]

**Fixed I-side Generator**
- `init()`:
  - Read trace
  - Schedule event for first request

- `tryNext()`:
  - Send current request
  - Read next request
  - Schedule event for next tryNext()

**Elastic D-side Generator**
- `init()`:
  - Read trace & populate DepGraph
  - Add root node to the readyList
  - Schedule event for execute() at execute time of the head of the readyList

- `completeMemAccess()`:
  - Update HW resources for store
  - Update DepGraph, child nodes for completed load
  - checkAndIssue() any new dependency-free nodes
  - Add nodes that fail to issue to depFreeQueue
  - Schedule event for next execute()

- `execute()`:
  - checkAndIssue() from depFreeQueue
  - Check HW resource availability and issue, i.e. add to readyList
  - Loop through nodes in readyList
    - If STORE, send request
    - If LOAD, send request
    - If COMP, do nothing
  - Update DepGraph, child nodes for completed nodes
    - checkAndIssue() any new dependency-free nodes
    - Add nodes that fail to issue to depFreeQueue
    - Populate DepGraph by reading from trace
    - Schedule event for execute() at execute time of the head of the readyList

[Diagram of Memory sub-system and I-Cache/D-Cache Port]

http://gem5.org/TraceCPU
SimMATE + Elastic Traces = ElasticSimMATE

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.
Proper tracing of synchronizations

- API-dependant: OpenMP 3.x
- Tracing whenever entering or leaving parallel region, barrier etc.

```c
#pragma omp parallel
for(i=0;i<n;i++) {
  /* do_some work */
}
```

```c
for(i=0;i<n;i++) {
  OMP_runtime_call()
  /* do_some work */
}
```

1.bin
OMP runtime + scheduler

<table>
<thead>
<tr>
<th>Tick</th>
<th>PC</th>
<th>th_id</th>
<th>type</th>
<th>IC</th>
<th>DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>389178</td>
<td>177216</td>
<td>0</td>
<td>1</td>
<td>1081157</td>
<td>165738</td>
</tr>
</tbody>
</table>

...
ESW wrapup

- ESM flow wrapup
  - Using BSC Mercurium compiler / Nanos++ runtime
  - Tweaked runtime such that custom m5 pseudo instructions produce trace records
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

Benchmarks: Execution Time [s] vs L2 Cache Size

Benchmarks: Error Percentage [%] vs L2 Cache Size
**Benchmarking**

- **Two main use cases:**
  - Fast parameter exploration
  - Scalability study: « trace replication »

- **Speedup & accuracy?**
  - Experiments on Rodinia application kernels

---

**Graphs**

- **Execution Time [ms]**
  - L2 Cache Size: 0MB, 16kB, 128kB, 512kB, 1MB, 2MB
  - FS, ET, ESM

- **Error Percentage [%]**
  - L2 Cache Size: 0MB, 16kB, 128kB, 512kB, 1MB, 2MB
  - FS vs ET, FS vs ESM
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels
Benchmarking

Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

![Graph showing L2 Cache Miss Rate and L2 Cache Overall Miss Latency](image)
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

128 cores KMEANS
Scalability analysis has limits
- Requires additional features s.a. **address offsetting**
- **Weak scaling** only (replicated per-core workloads)

Programming models moving from loops to **tasks**
- OpenMP 4.0, OmpSs
- Still pragma-based
- More parallelisms available at run-time … more opportunities for smart job scheduling

BSC OmpSs: Cholesky decomposition
- **Unbinding traces from cores**
  - One trace per Task, not per core!
  - Assign traces to cores by emulating runtime behaviour in trace replay
  - This is real strong scaling

**Trace collection**

**Trace simulation**

Ready Task queue

Scheduler

Task 1 trace

Task 2 trace

Task N trace

Task dependencies

Scheduler / runtime (emulated)

Interconnect

Memory
Current ESM prototype

- ~5x - 10x speedup for low core count, probably more for tens / thousands
- Nice solution for fast DSE
- Remaining accuracy issues for some applications
  - Common to ESM & Elastic Traces
  - Under investigation with ARM

Use cases

- Exploration of memory subsystem
- Some microarchitecture parameters (Elastic Traces)
- ...

Future directions

- Ruby compatibility
- Could be combined with other initiatives (dist-gem5)
- Can be extended to other PM / APIs (Tasking, MPI…)

http://montblanc-project.eu