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To cite this version:

HAL Id: lirmm-01723755
https://hal-lirmm.cnrs.fr/lirmm-01723755
Submitted on 18 Jun 2019

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Trace-driven simulation of multithreaded applications in gem5

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Alejandro NOCUA, Florent BRUGUIER, Anastasiia BUTKO

Cambridge, UK – September 11, 2017
Background motivations

- Mont-Blanc 1, 2 & 3 projects (FP7, H2020)
  - Getting ARM technology ready for HPC: HW, SW & Apps
  - Advances in energy efficiency towards Exascale

- Initial effort: using gem5 for performance prediction (2011)
  - STE Nova A9500 SoC (dual-core Cortex A9)
  - Fed publicly available parameters into a gem5 FS model
  - 1.5% - 18% error, due to rough DRAM model and interconnect

**Sources of error**

- Specification
- Memory & Interconnect

Background motivations cont’d

- **Calibration against real hardware**
  - Using gem5 for performance prediction
  - And McPAT for power estimation

- **Then onto exploring fancy architecture configurations**
  - Heterogeneous single-ISA multicores à la big.LITTLE
  - Assymetric, 3 levels of heterogeneity etc.

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**Results**

- Calibration
  - Exynos
  - Power error ~12%
  - Execution time error ~20%

- 2 L2 caches, Crossbar Bus
  - Independent clock per cluster

- 8 heterogeneous cores

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**Design Exploration For Next Generation High Performance Cores**

- Using McPAT and gem5 for power estimation
- Assymetric, Big.LITTLE, manycore architectures

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**Accuracy assessments**

- Cont’d
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy? Any sweet spot?

```
<table>
<thead>
<tr>
<th>Speed</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Low</td>
<td>Cycle-accurate</td>
</tr>
<tr>
<td>Low</td>
<td>Cycle-approximate</td>
</tr>
<tr>
<td>Low</td>
<td>Distributed</td>
</tr>
<tr>
<td>Low</td>
<td>Trace-driven</td>
</tr>
<tr>
<td>High</td>
<td>JIT</td>
</tr>
</tbody>
</table>
```

**Ideal**
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy?

```
Background motivations cont’d

Not ready for manycores, too slow!
- 1K-1M (simulated) IPS
- Scales bad with system size
- Already much better than RTL though

Trading speed for accuracy?
```
~ 70% simulation effort goes into CPU

- Abstracting away CPU cores sounds like a good idea
- Between 2 consecutive L1 cache misses (in-order) CPU cores perform « consistenly »
SimMATE: 2-stage process

- Trace collection: tracing only L1 miss related transactions
- Trace replay: Using trace injectors that initiate transactions as previously recorded

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**Trace Collection**

1. Core 0
2. Core n

- Hits & Misses
- Misses

**Trace Simulation**

1. TI 0
2. TI n

- Misses

**Memory traces**

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**Time**

- Trace

---

**SimMATE Trace-Driven Approach**

- Main concept: Trace collection, trace simulation

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**Core 0**

- Interconnect

**Core n**

- Interconnect

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**Memory**

- Cache

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**CPU**

- Time
SimMATE for faster DSE

- **Trace collection = freezing**
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- **Trace replay allows exploring the rest**
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed

![Diagram of Trace Collection and Trace Simulation](image)
SimMATE for faster DSE cont’d

- Trace replay performs event (re-) scheduling
  - Simple « time shifting » approach
  - Maintaining constant compute phases

![Diagram showing memory and interconnect with time delays](image-url)
**SimMATE Benchmarking**

- **Tuning DRAM latency**
  - Collection performed with 30ns
  - TD simulation from 5ns to 55ns
  - FS used as reference

![Execution time error (%)](image)

- MJPEG
- FFT

- 5ns: 2.8%
- 15ns: 4.5%
- 30ns: 5.8%
- 45ns: 5.1%
- 55ns: 6%

Original
Tuning L2 size

- Collection performed without L2
- TD simulation from 0 to 16MB L2
- Errors originate from Cold-start bias / cache warmup

Execution time error [%]

Traces: ET, ET+init, ET+OS boot

<table>
<thead>
<tr>
<th>L2 cache size</th>
<th>Original</th>
<th>256kB</th>
<th>1MB</th>
<th>8MB</th>
<th>16MB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execution time error [%]</td>
<td>0,1%</td>
<td>15%</td>
<td>14%</td>
<td>18%</td>
<td>15%</td>
</tr>
<tr>
<td>ET</td>
<td>8%</td>
<td>8%</td>
<td>10%</td>
<td>8%</td>
<td>15%</td>
</tr>
<tr>
<td>ET+init</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ET+OS boot</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SimMATE Benchmarking
Having these traces collected makes it easy to:

- Perform « Trace replication » i.e. emulate more CPU cores for scalability study
- This corresponds to *weak scaling* experiments, i.e. per-core workload remains same

```
Trace Collection
Core 0  Core n
 Trace Simulation
 TI 0   TI n
```

```
Number of Cache Misses
Core 0/ Thread 0
Core1/ Thread 1
```
Yet synchronizations must be accounted for!

- Using whatever API: POSIX threads, OpenMP 3.0 …
- Approach: embed synchronizations into traces
- Have an arbiter that takes care of locking (when barrier reached) and unlocking TIs
Limitation: in-order only!

- And most ARM AP are OoO (Out-of-Order)
  - Meaning multiple outstanding memory transactions
  - The assumption of constant time btw. 2 misses does not hold

- big-LITTLE & other heterogeneous friends everywhere
  - And there microarchitecture details cannot be overlooked
Elastic Traces: Trace-driven simulation for OoO

- Modeling micro-architecture timing & dependencies
  - Tracing with O3 model + probes, without L2 cache
  - Replay done in a smart « elastic » fashion

http://gem5.org/TraceCPU
Smart TraceCPU

- Updating a dependency graph pushing ready instructions into a queue for issue

Elastic Traces: Trace-driven simulation for OoO

[Diagram showing TraceCPU process]

http://gem5.org/TraceCPU
SimMATE + Elastic Traces = ElasticSimMATE

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

ElasticSimMATE (ESM)
Proper tracing of synchronizations

- API-dependant: OpenMP 3.x
- Tracing whenever entering or leaving parallel region, barrier etc.

```c
#pragma omp parallel
for(i=0;i<n;i++) {
  /* do_some work */
}
for(i=0;i<n;i++) {
  OMP_runtime_call()
  /* do_some work */
}
```

```
Tick  PC    th_id type  IC    DC
389178 177216 0   1    1081157 165738 ...
```
ESM flow wrapup

- Using BSC Mercurium compiler / Nanos++ runtime
- Tweaked runtime such that custom m5 pseudo instructions produce trace records
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

### Benchmarking

<table>
<thead>
<tr>
<th>L2 Cache Size</th>
<th>Execution Time [s]</th>
<th>Error Percentage [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0MB</td>
<td>2.5</td>
<td>0</td>
</tr>
<tr>
<td>16kB</td>
<td>2.0</td>
<td>1</td>
</tr>
<tr>
<td>128kB</td>
<td>1.5</td>
<td>2</td>
</tr>
<tr>
<td>512kB</td>
<td>1.0</td>
<td>3</td>
</tr>
<tr>
<td>1MB</td>
<td>0.5</td>
<td>4</td>
</tr>
<tr>
<td>2MB</td>
<td>0</td>
<td>5</td>
</tr>
</tbody>
</table>

**Graph:**
- Comparison of Execution Time across different L2 cache sizes for FS, ET, and ESM.
- Error Percentage comparison between FS vs ET and FS vs ESM.
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

Benchmarking

![Graph showing execution time and error percentage against different L2 cache sizes for FS, ET, and ESM.]

![Graph showing error percentage against different L2 cache sizes for FS vs ET and FS vs ESM.]

1 core KMEANS
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

![Graph showing execution time and error percentage for different L2 cache sizes for 1 core and CANNEAL.]
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

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**Benchmarking**

- L2 Cache Miss Rate [%]
- L2 Cache Overall Miss Latency [Cycles]
Two main use cases:

- Fast parameter exploration
- Scalability study: «trace replication»

Speedup & accuracy?

- Experiments on Rodinia application kernels

Benchmarking

128 cores KMEANS
Scalability analysis has limits

- Requires additional features s.a. address offsetting
- **Weak scaling** only (replicated per-core workloads)

Programming models moving from loops to tasks

- OpenMP 4.0, OmpSs
- Still pragma-based
- More parallelisms available at run-time … more opportunities for smart job scheduling

BSC OmpSs: Cholesky decomposition
Unbinding traces from cores

- One trace per Task, not per core!
- Assign traces to cores by emulating runtime behaviour in trace replay
- This is real strong scaling

Trace collection

Trace simulation

Perspectives
- **Current ESM prototype**
  - ~5x - 10x speedup for low core count, probably more for tens / thousands
  - Nice solution for fast DSE
  - Remaining accuracy issues for some applications
    - Common to ESM & Elastic Traces
    - Under investigation with ARM

- **Use cases**
  - Exploration of memory subsystem
  - Some microarchitecture parameters (Elastic Traces)
  - …

- **Future directions**
  - Ruby compatibility
  - Could be combined with other initiatives (dist-gem5)
  - Can be extended to other PM / APIs (Tasking, MPI…)

http://montblanc-project.eu