Trace-driven simulation of multithreaded applications in gem5
Gilles Sassatelli, Alejandro Nocua, Florent Bruguier, Anastasiia Butko

To cite this version:

HAL Id: lirmm-01723755
https://hal-lirmm.ccsd.cnrs.fr/lirmm-01723755
Submitted on 18 Jun 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L’archive ouverte pluridisciplinaire HAL, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d’enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.
Trace-driven simulation of multithreaded applications in gem5

Gilles SASSATELLI
sassatelli@lirmm.fr

Alejandro NOCUA, Florent BRUGUIER, Anastasiia BUTKO

Cambridge, UK – September 11, 2017
Background motivations

- Mont-Blanc 1, 2 & 3 projects (FP7, H2020)
  - Getting ARM technology ready for HPC: HW, SW & Apps
  - Advances in energy efficiency towards Exascale

- Initial effort: using gem5 for performance prediction (2011)
  - STE Nova A9500 SoC (dual-core Cortex A9)
  - Fed publicly available parameters into a gem5 FS model
  - 1.5% - 18% error, due to rough DRAM model and interconnect

Calibration against real hardware

- Using gem5 for performance prediction
- And McPAT for power estimation

Then onto exploring fancy architecture configurations

- Heterogeneous single-ISA multicores à la big.LITTLE
- Assymetric, 3 levels of heterogeneity etc.
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy? Any sweet spot?
Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy?

```
1 core FS simulation

Accuracy

Speed

High

Low

RTL

Cycle-accurate

Cycle-approximate

Distributed

Trace-driven

JIT

10s MIPS

69%

14%

15%

2%

CPU

Cache

Interconnect

Memory
```

Background motivations cont’d

- Not ready for manycores, too slow!
  - 1K-1M (simulated) IPS
  - Scales bad with system size
  - Already much better than RTL though

- Trading speed for accuracy?

```
1 core FS simulation

Accuracy

Speed

High

Low

RTL

Cycle-accurate

Cycle-approximate

Distributed

Trace-driven

JIT

10s MIPS

69%

14%

15%

2%

CPU

Cache

Interconnect

Memory
```
~ 70% simulation effort goes into CPU

- Abstracting away CPU cores sounds like a good idea
- Between 2 consecutive L1 cache misses (in-order) CPU cores perform « consistently »
SimMATE: 2-stage process

- Trace collection: tracing only L1 miss related transactions
- Trace replay: Using trace injectors that initiate transactions as previously recorded
SimMATE for faster DSE

- **Trace collection = freezing**
  - CPU parameters alongside application SW
  - Private caches sizes, speed etc.

- **Trace replay allows exploring the rest**
  - L2 size, policy etc.
  - Interconnect type & speed
  - Main memory speed

---

**Trace Collection**

- Core 0
- Core n
- Interconnect
- Memory

**Trace Collection**

- TI 0
- TI n
- Memory
- Interconnect
- L2

*I time*  
*Multiple times*
Trace replay performs event (re-) scheduling

- Simple « time shifting » approach
- Maintaining constant compute phases
SimMATE Benchmarking

- Tuning DRAM latency
  - Collection performed with 30ns
  - TD simulation from 5ns to 55ns
  - FS used as reference

---

![Diagram showing execution time error percentages for MJPEG and FFT at different latency values (5ns, 15ns, 30ns, 45ns, 55ns).]
## Tuning L2 size

- Collection performed without L2
- TD simulation from 0 to 16MB L2
- Errors originate from Cold-start bias / cache warmup

### Execution time error [%]

<table>
<thead>
<tr>
<th>L2 cache size</th>
<th>Traces: ET</th>
<th>ET+init</th>
<th>ET+OS boot</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original</td>
<td>0.1%</td>
<td>8%</td>
<td>1%</td>
</tr>
<tr>
<td>256kB</td>
<td>15%</td>
<td>8%</td>
<td>7.5%</td>
</tr>
<tr>
<td>1MB</td>
<td>18%</td>
<td>14%</td>
<td>10%</td>
</tr>
<tr>
<td>8MB</td>
<td>15%</td>
<td>18%</td>
<td>15%</td>
</tr>
<tr>
<td>16MB</td>
<td>8%</td>
<td>10%</td>
<td>7%</td>
</tr>
</tbody>
</table>

**SimMATE Benchmarking**
Having these traces collected makes it easy to:

- Perform « Trace replication » i.e. emulate more CPU cores for scalability study
- This corresponds to weak scaling experiments, i.e. per-core workload remains same

![Diagram showing Trace Collection and Trace Simulation]
Multithreaded applications

- Yet synchronizations must be accounted for!
  - Using whatever API: POSIX threads, OpenMP 3.0 …
  - Approach: embed synchronizations into traces
  - Have an arbiter that takes care of locking (when barrier reached) and unlocking TIs
And most ARM AP are OoO (Out-of-Order)

- Meaning multiple outstanding memory transactions
- The assumption of constant time btw. 2 misses does not hold

big-LITTLE & other heterogeneous friends everywhere

- And there microarchitecture details cannot be overlooked
**Elastic Traces: Trace-driven simulation for OoO**

- **Modeling micro-architecture timing & dependencies**
  - Tracing with O3 model + probes, without L2 cache
  - Replay done in a smart « elastic » fashion

---

[Diagram showing O3 CPU, Elastic Trace, and Design space exploration]

- **One simulation run:**
  - Capture trace

- **Design space exploration:**
  - Replay same trace

---

[Links to resources: http://gem5.org/TraceCPU]
Smart TraceCPU

- Updating a dependency graph pushing ready instructions into a queue for issue

http://gem5.org/TraceCPU
SimMATE + Elastic Traces = ElasticSimMATE

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**SimMATE + Elastic Traces = ElasticSimMATE**

- Enabling both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**Barriers etc.**

**Elastic Trace**

- Instruction trace
  - Header:
  - Req:
- Synchronization trace
  - ... PC Event Inst Data
  - ...
- Data dependency trace
  - Header:
  - ... Inst:
  - ...

**ElasticSimMATE (ESM)**

- Enables both OoO + multithreaded applications
- Key: embed synchronization information @ tracing time.

**Global Stop/go**
ElasticSimMATE (ESM)

- Proper tracing of synchronizations
  - API-dependant: OpenMP 3.x
  - Tracing whenever entering or leaving parallel region, barrier etc.

```c
#pragma omp parallel
for(i=0;i<n;i++) {
  /* do_some work */
}
for(i=0;i<n;i++) {
  OMP_runtime_call()
  /* do_some work */
}
```

```
Tick  PC  th_id type  IC   DC
389178 177216 0   1 1081157 165738...
```
ESW wrapup

- **ESM flow wrapup**
  - Using BSC **Mercurium compiler** / **Nanos++ runtime**
  - Tweaked runtime such that custom m5 pseudo instructions produce **trace records**

```c
#pragma omp parallel
for(i=0;i<n;i++) {
    /* do_something */
}
```

**Unmodified sources**

**gem5 Trace Collection**

**Generated Traces**

**gem5 Trace Replay**

**App Binaries**

```c
#pragma omp parallel{
    for(i=0;i<n;i++){
        nanos_create_team();
        /* do_something */
        nanos_end_team();
    }
}
```

**Nanos++ runtime**

**Ref_Architecture**

**Target_Arch 1**

**Thread creation & such**

`m5_trace(TYPE,th_id)`
Two main use cases:
- Fast parameter exploration
- Scalability study: «trace replication»

Speedup & accuracy?
- Experiments on Rodinia application kernels
Two main use cases:

- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?

- Experiments on Rodinia application kernels

![Graphs showing execution time and error percentage for different L2 cache sizes.](image_url)
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

**Benchmarking**

![Graph showing execution time and error percentage for different L2 cache sizes.](image)
Benchmarking

- Two main use cases:
  - Fast parameter exploration
  - Scalability study: « trace replication »

- Speedup & accuracy?
  - Experiments on Rodinia application kernels

---

### L2 Cache Miss Rate [%]

<table>
<thead>
<tr>
<th>L2 Cache Size</th>
<th>FS</th>
<th>ESM</th>
</tr>
</thead>
<tbody>
<tr>
<td>16kB</td>
<td>70</td>
<td>60</td>
</tr>
<tr>
<td>128kB</td>
<td>60</td>
<td>50</td>
</tr>
<tr>
<td>512kB</td>
<td>50</td>
<td>40</td>
</tr>
<tr>
<td>1MB</td>
<td>40</td>
<td>30</td>
</tr>
<tr>
<td>2MB</td>
<td>30</td>
<td>20</td>
</tr>
</tbody>
</table>

---

### L2 Cache Overall Miss Latency [Cycles]

<table>
<thead>
<tr>
<th>L2 Cache Size</th>
<th>FS</th>
<th>ESM</th>
</tr>
</thead>
<tbody>
<tr>
<td>16kB</td>
<td>1.6E+10</td>
<td>1.4E+10</td>
</tr>
<tr>
<td>128kB</td>
<td>1.2E+10</td>
<td>1.0E+10</td>
</tr>
<tr>
<td>512kB</td>
<td>8E+09</td>
<td>6E+09</td>
</tr>
<tr>
<td>1MB</td>
<td>4E+09</td>
<td>2E+09</td>
</tr>
<tr>
<td>2MB</td>
<td>2E+09</td>
<td>1E+09</td>
</tr>
</tbody>
</table>

---

### L2 Cache Size

- FS
- ESM

---

### KMEANS

- L2

---

23
Two main use cases:
- Fast parameter exploration
- Scalability study: « trace replication »

Speedup & accuracy?
- Experiments on Rodinia application kernels

128 cores \[\text{KMEANS}\]
Scalability analysis has limits

- Requires additional features s.a. **address offsetting**
- **Weak scaling** only (replicated per-core workloads)

Programming models moving from loops to **tasks**

- OpenMP 4.0, OmpSs
- Still pragma-based
- More parallelisms available at run-time … more opportunities for smart job scheduling
Unbinding traces from cores

- One trace per Task, not per core!
- Assign traces to cores by emulating runtime behaviour in trace replay
- This is real strong scaling

Trace collection

Trace simulation

Perspectives
■ Current ESM prototype

- ~5x - 10x speedup for low core count, probably more for tens / thousands
- Nice solution for fast DSE
- Remaining accuracy issues for some applications
  - Common to ESM & Elastic Traces
  - Under investigation with ARM

■ Use cases

- Exploration of memory subsystem
- Some microarchitecture parameters (Elastic Traces)
- …

■ Future directions

- Ruby compatibility
- Could be combined with other initiatives (dist-gem5)
- Can be extended to other PM / APIs (Tasking, MPI…)

http://montblanc-project.eu