Guest Editorial Special Issue on Nanoelectronic Circuit and System Design Methods for the Mobile Computing Era

Aida Todri-Sanial, Saraju Mohanty, Mariane Comte, Marc Belleville

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Special Issue on Nanoelectronic Circuit and System Design Methods for the Mobile Computing Era

This special issue on nanoelectronic circuit and system design method for the mobile computing era covers a wide range of design challenges and solutions facing current designers for fast performing and energy efficient computing platforms. The papers presented in this issue span through various design challenges from devices, circuits and architecture to address some of the most imminent issues for low power computing. It is well known that the use of smart mobile phones, tablets, and notebooks, which are different forms of mobile computing platform, defines the present age social life style. Such heavy demand for ever smaller, portable, low-energy, high-performance, and secure electronic systems has been the primary driver for recent VLSI technology scaling. To continue coping with this trend, and to address new massive markets of the Internet of Things (IoT), high performance with energy constraints, low leakage dissipation, fast sleep and wake-up transitions, as well as reliability and security still remain significant challenges to address in future integrated circuits. In recent years, as the device sizes have reduced below 10nm, the challenges of design and manufacturing engineers have increased multifold. One example is leakage current, which because transistors are so small, now represents a significant proportion of the power consumption. Imagine, battery life of a smartwatch is matter of 24 hours only! Thus, at device level alternate device architecture, for example, thin film devices like FinFET or FDSOI, nanowires or 3D transistor are introduced and proposed for the next nodes. Simultaneously alternative to Flash memory are explored. Most of the proposals are based on resistive devices (e.g., MRAM, PCRAM, ReRAM). Designers have to assess the benefits of these new devices as well as to innovate by exploiting their unique capabilities. Better system-level architectures are also required for high performance at minimum energy and reliability. Finally, circuit- and system-level solutions are needed to improve security of the information being processed by the hardware. This special issue describes six articles covering topics from emerging technologies for devices, memories, architecture to processor design for energy efficiency and high performance. We briefly introduce them in the rest of the guest editorial.

Sartor et al., present several design techniques for very long instruction word (VLIW) processors to mitigate soft errors introduced due to technology scaling. The proposed fault tolerance techniques based on (1) phase-configurable duplication, (2) adaptive duplication, and (3) adaptive with ILP reduction provide fault tolerance at a minimum cost, by using idle resources of the VLIW processor with low area and power overhead. For the first two methods, the area overhead is less than 4% with no performance degradation. The third method based on ILP reduction has shown effective to improve fault tolerance with the cost of 14% area overhead and up to 27% of performance degradation. This is seminal work on exploiting the idle cycles of processor for improving its reliability and fault tolerance.

Fault tolerance is further investigated by Mohammadi et al. on arithmetic logic build based on controllable-polarity transistors. Such devices are very promising for implementing compact logic elements due to their enhanced functionalities such as they can be electrostatically configured to be either n- or p-type device. Authors present fault

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models and analysis unique for controllable polarity transistors in order to forecast the behavior of more complex circuits composed of such devices. Experimental results on an adder architecture indicate that the proposed fault-tolerant design is able to tolerate all possible single faults and up to 99.5% of double faults with minimal impact on area, performance and leakage power. Such large fault tolerance further motivates design of complex arithmetic logic at reduced implementation cost.

Fang et al., present an article on exploring oscillator-based computing systems with emerging nano-devices that can be exploitable for computer vision and pattern recognition applications. Inspired by the interactions between neural oscillations that occur on biological systems, recent advancements on spin torque oscillators, resonate body transistor oscillators and vanadium oxide oscillators have enabled building complex systems that can become the next-generation computing structures used for intelligent information processing. The authors present an in-depth look into the challenges on building complex, energy-efficient, and fast-performing systems based on oscillator devices. They provide models and analysis to understand how to build complex oscillator systems and address some of their fundamental issues such as synchronization/desynchronization, prediction of oscillator frequencies, and their relation to the degree of match function for pattern matching.

In Moreira et al., a new computing system based on digitally controlled delay elements is explored that yields low power and moderate delay quantization error under process, voltage, and temperature variations. They proposed a novel generic delay shift block using the 28nm FD-SOI technology. From the obtained results, the authors show that the process variations' impact on performance can be alleviated and fine-tuned by using the proposed digitally controlled elements, indicating the promise of building larger and more complex system based on such elements.

Exploring nonvolatile memory for novel computing paradigms such as normally-off computing is the scope of the article by Senni et al. The article explores the opportunity of having a nonvolatile memory as reconfigurable logic devices and processor and data storage by the integration of MRAM as register and main memory levels. Investigation on use of MRAM to design a nonvolatile processor is studied and analyzed the backup/restore performance and power consumption.

In Rakshit et al., monolayer heterojunction FETs based on vertical transition metal dichalcogenides (TMDCFETs) and planar black phosphorus FETs (BPFETs) have been explored to design energy-efficient and denser SRAM. The approach relies on an atomistic self-consistent device modeling with SRAM circuit design and simulation. The SRAM has lower static power, smaller read/write delay, and a higher dynamic read/write noise margin at the low operating voltages.

Finally, the guest editors sincerely hope that this special issue will be a great read for contemporary researchers worldwide. The guest editors would like to sincerely acknowledge the Editors-in-Chief of the *ACM Journal on Emerging Technologies in Computing Systems (JETC)* Dr. Krishendu Chakrabarty and Dr. Yuan Xie. The guest editors are extremely thankful to the reviewers for their timely reviews. A majority of the reviewers represent experts in their fields who provided high-quality reviews for the articles. We thank the authors for their patience and dedication at all stages of the review process. Each manuscript was assigned at least to three reviewers and has undergone multiple rounds of peer-review.

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