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# Atomistic- to Circuit-Level Modeling of Doped SWCNT for On-Chip Interconnects

Jie Liang, Jaehyun Lee, Salim Berrada, Vihar P. Georgiev, *Member, IEEE,* Reeturaj Pandey, Rongmei Chen, *Member, IEEE,* Asen Asenov, *Fellow, IEEE* and Aida Todri-Sanial, *Member, IEEE*

***Abstract*—In this article, we present a hierarchical model for doped single-walled carbon nanotube (SWCNT) for on-chip interconnect application. Our model aims to study CVD grown SWCNTs while considering defects and contacts to metal electrodes. Both defects and poor contacts can worsen CNT conductivities and ultimately deteriorate their interconnect performance. We investigate the fundamental physical mechanism of charge based doping with the purpose of improving SWCNT electrical conductivity as well as a potential solution to alleviating the impact of defects and contact resistances. We present an atomistic model to study the number of conducting channels of doped SWCNT with different vacancy defect configurations. Circuit-level electrical modeling and simulations are performed on SWCNT interconnect while considering the impact of doping, defects and contact resistance. Simulation results show up to 80% resistance reduction by doping where 17% of delay increases due to defects. Additionally, we observe doping can mitigate the impact of defects by more than 12%, but there is almost no improvement in the contact resistance.**

***Index Terms*—carbon nanotubes, defective SWCNT, doped SWCNT, on-chip interconnect.**

## I. Introduction

With technology node scaling down, the performance of on-chip interconnects is degrading due to increased parasitics and becoming even more critical for ultra large-scale integrated (ULSI) circuit performance. Conventional copper (Cu) interconnects have started to reach their limits by the continuous shrinking of dimensions and high aspect ratio requirements [1], [2]. The large current flows and elevated on-chip temperatures introduce severe electromigration issues which are worsening with sub 10nm scaling [3]. Finding a new material to replace Cu as on-chip back-end-of-line interconnect material has attracted a lot of research interest and is an on-going quest [4], [5]. Carbon nanotubes (CNTs) due to their ballistic transport and high thermal conductivity are considered as a potential candidate for future on-chip interconnects [6]. Nevertheless, controlling the chirality of CNTs is still not trivial and under many investigations [7]–[9].

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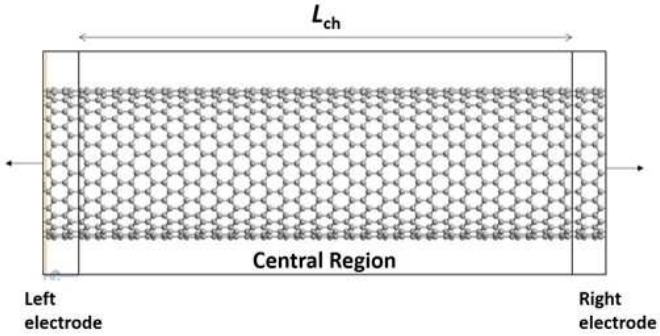



Fig. 1. Atomistic simulation geometry of SWCNT (24,0) for interconnect configuration. Two semi-infinite electrodes, and length of defective region $L_{ch}$ is set as 42.6 nm.

In this work, we investigate charge-based doping of CNTs as a means to alleviate the impact of random chirality distribution. Based on the atomistic simulation, it was shown that doping degenerates semiconducting to metallic CNTs which are suitable for interconnect application [10]. We further investigate doping on CNTs to understand its impact on CNT conductance and performance. Additionally, we study defects which might be introduced during the CNT growth process [11] and consequently can impact the CNT performance and power dissipation for on-chip interconnects. Moreover, the metal-CNT contact resistance is also an essential factor for fast, and reliable interconnect application. In this paper, we investigate doped, and defective SWCNT including contact resistances for back-end-of-line (BEOL) on-chip interconnects.

## II. Hierarchical Model

### A. Atomistic modeling

Atomistix ToolKit (ATK) [12] implemented by the framework of tight-binding (TB) Non-Equilibrium Greens Function (NEGF) has been used for atomistic modeling. An extended TB approach, which includes the third nearest neighbor hopping is used for describing the CNTs Hamiltonian [13]. We use the ballistic approximation for all transport calculations.

Figure 1 shows the geometry of metallic zigzag SWCNT (24,0) for an interconnect configuration. Left and right electrodes are semi-infinite electrodes with the defective region (central region) in between. We only consider vacancy type of defects where several carbon atoms can be missing from the SWCNT. In the central region, we distribute vacancy defects

TABLE I
STATISTICAL VALUES OF DEFECTIVE RESISTANCE FOR SWCNT (24,0)

| Length of SWCNT defective region (nm) | SWCNT Diameter (Ang) | Number of defects | Defective resistance (kΩ) |
|---|---|---|---|
| 42.6 (100UC) | 18.8 | 1 | 4.028 |
| 42.6 (100UC) | 18.8 | 2 | 12.469 |
| 42.6 (100UC) | 18.8 | 3 | 15.241 |
| 42.6 (100UC) | 18.8 | 4 | 26.380 |
| 42.6 (100UC) | 18.8 | 5 | 31.268 |
| 42.6 (100UC) | 18.8 | 6 | 39.499 |

randomly from 1 to 6. We compute the defective resistance as $R_{defect}$=$R_{total}$-$R_{ballistic}$ where $R_{total}$ is calculated by TB-NEGF. Please note that the length of the defective region does not impact the defective SWCNT resistance as was shown in [14]. The length of the defective region is set to 42.6 nm and we observe that distribution of defective resistance varies slightly with the length, however the defective resistance mean values remain almost unchanged. This is because the interaction between defects is shorter than their phase relaxation length in our atomistic configuration.

Fig. 2 shows a statistical analysis and derivation of the median value of defective resistance for each configuration. 80 samples were used for the calculation. Specific values are shown in Table 1. Defective resistance mean value varies from 4 to 40 kΩ with 1 to 6 defects, respectively. In [14], it was shown a small variation of defective resistance mean value for both metallic zigzag and armchair SWCNT. Our models and simulation approach are suitable for both zigzag and armchair type of SWCNTs.

Density Functional Theory (DFT) with Generalized Gradient Approximation (GGA) is used to calculate the conductance $G$ of SWCNT with respect to the different position of Fermi energy level. We assume a) there are no additional states due to dopant; b) there is no change of Density of State (DOS) or energy band structure due to dopant. The number of conducting channels $N_C$ is derived by $G/G_0$, where $G_0$ is the quantum conductance $2e^2$/h ($G_0$ = 7.748 $10^{-5}$ S). Fig. 3 shows the results of DFTGGA calculation for deriving the number of conducting channels as a function of Fermi-level energy.

### B. Electrical compact modeling

Electrical models of CNT for interconnect application have already been developed and widely used by our community. Most notably, [15] and [16] have investigated modeling and simulation of pristine single-walled (SW) and multi-walled (MW) CNTs for on-chip interconnects. Based on their work, we explore here the number of conducting channels $N_C$ on CNTs as an important physical parameter for doped CNTs. We also take into account the resistance due to defects. We develop a hierarchical model and simulation method to assess the performance of fabricated SWCNTs (i.e., defects, impurities, contacts) realistically for on-chip interconnect applications.

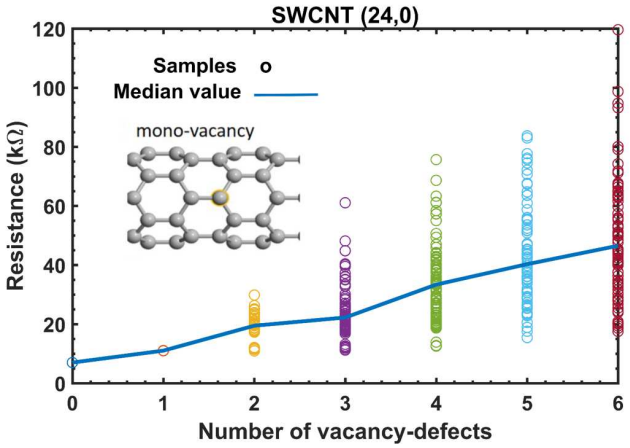



Fig. 2. Dependence of resistance on the number of vacancy defects for a pristine SWCNT (24,0) with 80 samples used for statistical results.

Controlling of the chirality and variability of CVD grown CNTs (i.e., variations on diameter, contacts, number of shells, defects, etc.) remains a challenge. In this paper, we investigate doping as a way to enhance metallic CNTs behavior while alleviating the impact of defects and poor contacts. Large doping concentrations introduce more conducting channels for CNTs [17]. From semiconductor physics and atomistic simulations, we understand that doping shifts the Fermi-level of SWCNT. Moreover, we know from quantum physics that the electron transport (i.e., conducting property) occurs around the Fermi-level. Hence, the Fermi-level shifting by doping introduces more electron subbands available for charge transport on SWCNTs with respect to the particular Fermi-Dirac energy band. From Fig. 3, a pristine metallic SWCNT has two conducting channels (at 0 eV) and after shifting the Fermi-level position to 1 eV (due to doping), up to 8 conducting channels are introduced.

We also consider defects that occur during the CNT growth process. Defects on SWCNT are modeled as a defective resistance. Based on the atomistic simulation results, we incorporate the defective resistance into our compact SWCNT electrical model. We also investigate the contact resistance on SWCNTs. Contact resistance plays a critical role in interconnect performance and reliability. By taking into account, the impact of doping, defects and contact resistance, our compact model for SWCNT electrical resistance is as:

$$R_{SWCNT} = \frac{h}{2e^2 N_C}(1 + \frac{L}{L_{mfp}}) + R_{defect} + R_{contact} \quad (1)$$

where $L_{mfp}$ is the electron mean free path [18]. We model the SWCNT interconnect as a RC-model where parasitic resistance R is given by equation (1), and parasitic capacitance C is modeled as quantum capacitance $C_Q$ connected in series with electrostatic capacitance $C_E$, as shown in equation (2), similar to [15]. Doped $C_Q$ is linearly dependent on $N_C$. If $N_C$ gets larger, $C_E$ will have the tendency to dominate $C_{SWCNT}$.

$$C_{SWCNT} = \frac{C_Q C_E}{C_Q + C_E} \quad (2)$$

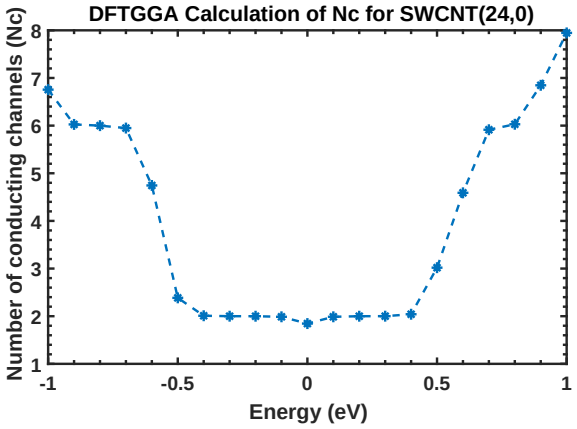



Fig. 3. DFTGGA calculation of number of conducting channels $Nc$ for SWCNT (24,0) over different Fermi-level energy positions.

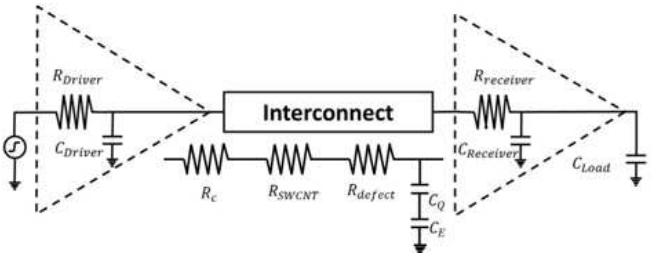



Fig. 4. Circuit level "driver-interconnect-receiver" benchmark for delay simulation.

To evaluate the performance of a defective doped SWCNT with contact resistance, we use a circuit benchmark as shown in Fig. 4. Specific values of $R_{driver}$, $C_{driver}$ and $C_{load}$ used in our simulations are 24 kΩ, 450 aF and 10 fF respectively, which are values extracted from the logic gates implemented in CMOS 45 nm technology node.

## III. Simulation Results

We perform our circuit simulations using the Cadence environment with Verilog-A models to represent the SWCNT interconnects between logic gates. We vary the number of SWCNT conducting channels from 2 to 8 to represent different doping concentrations. We also study vacancy-type defects by varying SWCNT resistance as given in Table 1. Additionally, we include the contact resistance varying from 0 to 10 kΩ to represent side contact with different contacting lengths [19].

Figure 5 shows the pristine SWCNT resistance varying with length and diameter. There are no defects and contact resistance. We note that the resistance increases dramatically with lengths longer than 1 $\mu$m. From theoretical understanding, we know that the mean free path of a SWCNT with $D$ = 1 nm is about 1 $\mu$m; above this length, the scattering resistance starts to impact the total SWCNT resistance. We also see that resistance decreases for larger diameter SWCNTs as larger diameters provide more metallic conducting property.

Figure 6 shows the resistance of doped SWCNT (24,0) with $D$ = 18.8 Ang as a function of length and number of conducting channels $N_C$. With $N_C$ increasing to 8, the

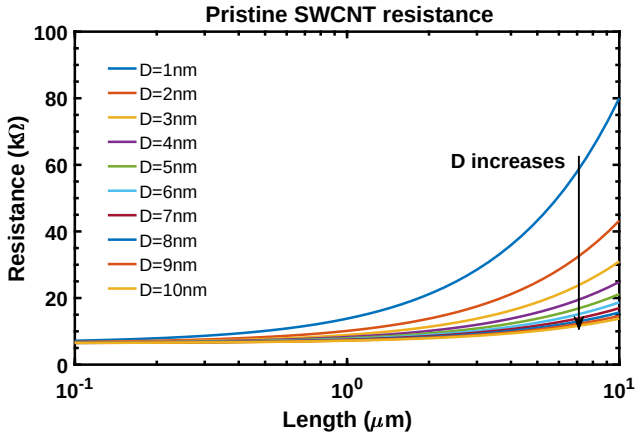



Fig. 5. Resistance of pristine SWCNT varying with length for different diameters.

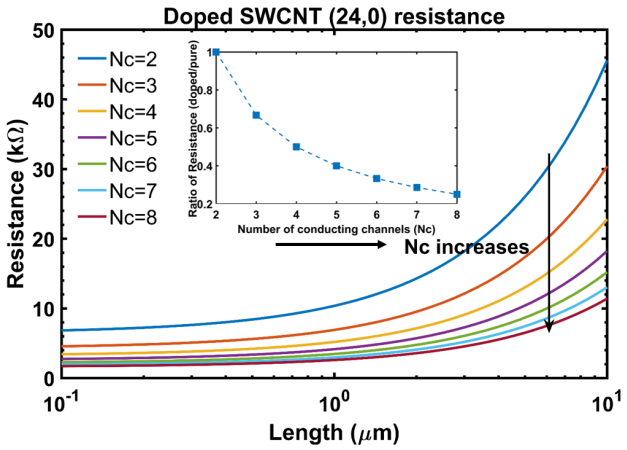



Fig. 6. Resistance of doped SWCNT (24,0) varying with length with different numbers of conducting channels $N_C$. **inset**: resistance ration after increasing $N_C$ (doping level).

resistance is reduced up to 80% (see Fig. 6 inset). Having a fixed diameter over different lengths, we note that doping can reduce the overall resistance. In this plot, we do not consider the defects and contact resistance.

Figure 7 shows the delay ratio of a pristine SWCNT with and without defects over different lengths. Contact resistance is set to 0. This plot is derived based on the values of defective resistance from Table 1. We can see the maximum delay ratio happens on SWCNT length around 15 $\mu$m regardless of the number of defects. Delay ratio increases before $L$ = 15 $\mu$m, but stays steady or decreases when SWCNT lengths get longer. To understand this phenomenon, we note from equation (1), the total SWCNT resistance depends on scattering resistance (first part where $L_{mfp}$ is included) and defective resistance with same impacts on delay. For shorter length, the delay is strongly influenced by defective resistance, while scattering resistance gets more dominant when SWCNT length is much longer than the electron mean free path $L_{mfp}$, where the delay ratio remains steady or decreasing.

In Fig. 8, we compare a doped (24,0) SWCNT ($L$ = 1 $\mu$m) with defects to a pristine SWCNT. No contact resis-

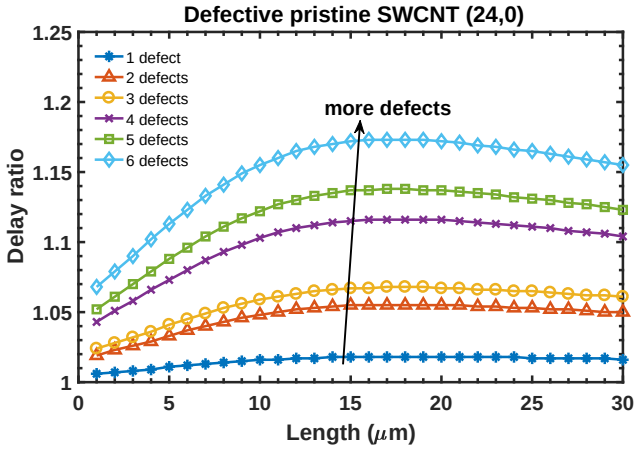



Fig. 7. Delay ratio of pristine SWCNT (24,0) with and without defects over different length.

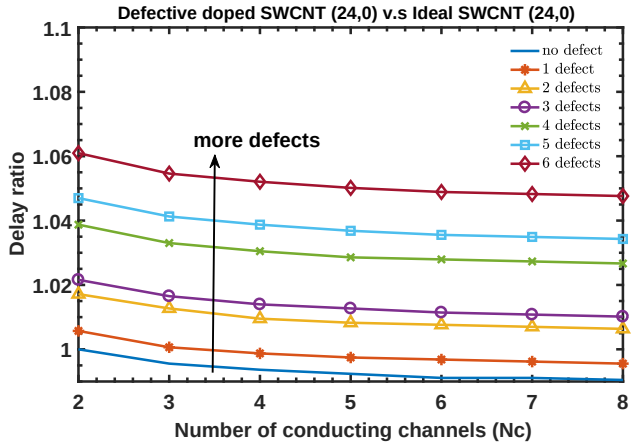
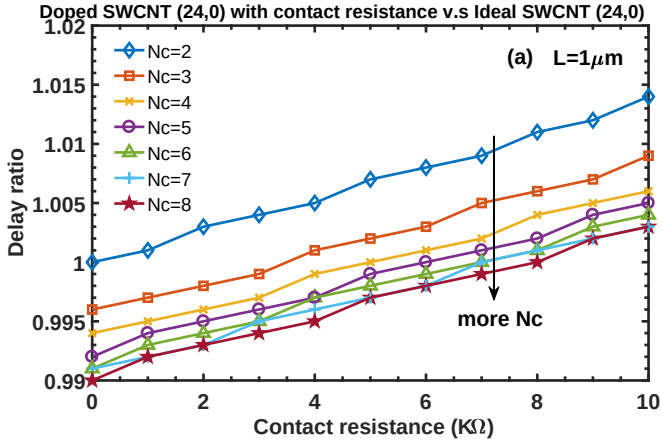



Fig. 8. Delay ratio of defective doped SWCNT vs. pristine ideal SWCNT.



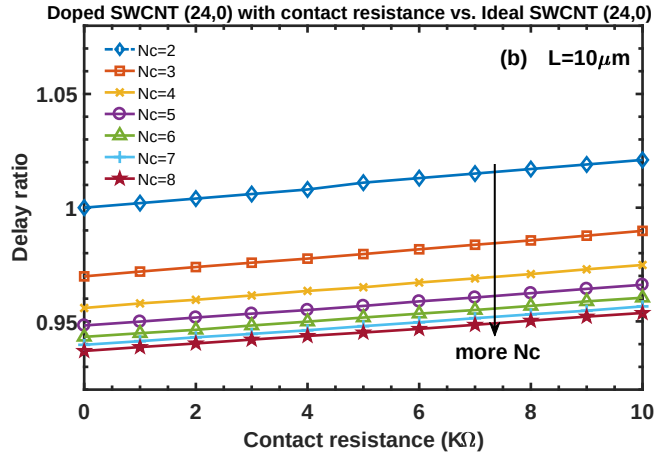




Fig. 9. Delay ratio of doped SWCNT with contact vs. ideal SWCNT without contact. (a) SWCNT length $L$ = 1$\mu$m. (b) SWCNT length $L$ = 10$\mu$m.

tance is used here. Fig. 8 shows the delay ratio. We know that increasing the doping concentration (i.e., larger $N_C$) can reduce the resistance, but it will increase the quantum capacitance $C_Q$, whereas the electrostatic capacitance $C_E$ will remain constant, therefore, the total capacitance remains unchanged. Hence, doping could reduce the propagation delay as shown in the straight blue line where no-defect SWCNT delay ratio decreases with doping concentration. However, additional defective resistance will increase the delay. We can see 6% of delay is increased with 6 defects, but by introducing doping ($N_C$ = 8), delay ratio is reduced by 1%. We also note that occurrence of a single (1) defect with doping of ($N_C$ = 3) can remain the delay ratio equal to 1.

Figure 9 shows the delay ratio between doped (24,0) SWCNT with contact resistance and pristine SWCNT. In these plots, we do not take into account the defects. Fig. 9 (a) shows the delay ratio for SWCNT length $L$ = 1 $\mu$m and we observe some trade-off phenomena. If delay ratio keeps inferior to 1, we can tolerate up to 4 k$\Omega$ of contact resistance with doping of $N_C \geq 3$; whereas we need doping to compensate a contact resistance of 8 k$\Omega$. We observe a few overlapping parts between different configurations, which can be quite interesting for interconnect architecture design with short lengths. Fig. 9 (b) shows the same delay ratio comparison but with a length $L$ = 10 $\mu$m. Overlapping parts are disappearing, but with doping of $N_C \geq 3$ a contact resistance of 10 k$\Omega$ can be tolerated to keep the delay ratio under 1. Comparing to Fig. 9 (a), doping has much stronger impacts on delay for longer SWCNT. With contact resistance as great as 10 k$\Omega$ and doping of $N_C$ = 8, short SWCNT has a delay ratio slightly larger than 1, whereas 5% of delay reduction is observed for longer SWCNT.

Overall, we observe that large diameter SWCNTs ($\geq 5nm$) will be more suitable for on-chip interconnects thanks to its lower resistance. Moreover, doping can be applied to reduce further SWCNT resistance. Presence of vacancy (i.e., mono- or di-vacancies) defects induces a large defective resistance, especially on short SWCNTs. Poor contacts which exhibit a large contact resistance worsen SWCNT interconnect performance. Charge-based doping helps to mitigate some of the impacts of defects and poor contacts. However, as resistance due to defects and poor contacts increases, doping becomes less efficient.

## IV. Conclusion

A hierarchical model, from atomistic- to circuit-level, has been developed and investigated. We study the defective resistance and number of conducting channels by doping for a metallic zigzag (24,0) SWCNT by using TB-NEGF and DFTGGA on atomistic simulations. We investigate circuit-level electrical compact modeling and simulations to evaluate the SWCNT interconnect propagation delay with multiple dependencies (defects, doping, contacts). We observed up to 17% of delay can be increased by defects. However, 80% of SWCNT resistance can be reduced by doping as well as more than 10% of defective SWCNT delay is mitigated by doping. Some trade-offs are also observed between the impact of defects, contact resistance and doping on interconnect performance, which can be of interest for circuit level interconnect architecture design. By introducing doping and carefully choosing SWCNT lengths, interconnect performance can be improved while alleviating defects and contact resistances.

## Acknowledgment

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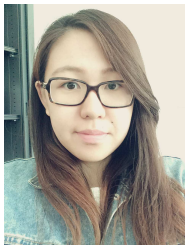

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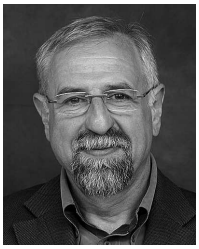

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