Electrical Performance of Carbon-Based Power Distribution Networks with Thermal Effects

A. Magnani, M. de Magistris
DIETI, University Federico II, Naples, Italy
alessandro.magnani@unina.it
m.demagistris@unina.it

S. Heidari
School of ECE, College of Eng., University of Tehran, Tehran, Iran
salomeh.heidari@ut.ac.ir

A. Todri-Sanial
CNRS- LIRMM
University of Montpellier
Montpellier, France
todri@lirmm.fr

A. Maffucci
DIEI, University of Cassino and Southern Lazio, Cassino, Italy
maffucci@unicas.it

***Abstract*—This paper presents a performance analysis of Power Delivery Networks (PDNs) with innovative carbon-based materials, such as carbon nanotubes and graphene nanoribbons. The electrical and thermal performances of such PDNs are described in terms of voltage drop and temperature rise, respectively. The performance analysis is carried out by efficiently solving an electrothermal model, where the electrical and thermal sub-models are coupled in a relaxation approach. Compared to existing studies, a more accurate model for the electrical resistance of CNT or GNR interconnect is here introduced, allowing a more realistic description of the contact resistance and its dependence on the temperature. As a case study, a typical PDN structure for a chip at the 22 nm technology node is considered, and the results are compared to those obtained by using conventional conductors.**

Keywords—Carbon nanotube; on-chip power distribution networks; electrothermal analysis.

I. Introduction

When next generation nanoscale Integrated Circuits (ICs) are considered, Power Delivery Networks (PDNs) design become critical because of higher current density and larger heat dissipation. In fact, no technological solutions are currently known to meet many of the requirements [1].

There is a large body of research on carbon-based materials, such as Carbon Nanotubes (CNTs) or Graphene Nanoribbons (GNRs), that promises to overcome most of such problems in nanoscale interconnects given their outstanding electrical, thermal and mechanical properties [2]. Due to their electron ballistic transport and high thermal conductivity, such technological solution is, at the same time, also promising for the realization of resilient PDNs, carrying high current density and with low voltage drops. As an example, CNTs are reported to be able to carry an electrical current density of up to GA/cm^2, two orders of magnitude higher than the maximum current density allowed for copper [2].

The modeling of transport phenomena along carbon-based interconnects has been the object of significant research effort in the last years. As a byproduct of that, simple circuit models are available where the quantum nature of the transport is taken into account by equivalent circuit parameters, such as kinetic inductance and quantum capacitance, e.g. [3]-[6]. Parallel to this theoretical work, significant effort has also been devoted to assessing efficient and reliable fabrication procedures to obtain CNT/GNR interconnected circuits [7]: this led to the first examples of successful integration between such interconnects and CMOS technologies, [8]. Nevertheless, to the best of our knowledge, no practical applications of CNTs/GNRs to power interconnects have been yet realized.

Due to large current densities, a fundamental issue for carbon-based PDNs is to derive and simulate self-consistent Electro-Thermal (ET) models. Despite that, few scientific works deal with such issue. Early works such as [9] were limited to single-wall CNTs (SWCNTs), with a constant mean free path. The impact of temperature on CNT resistance was introduced in [10], but Cu and CNT interconnects were compared by using an electrical model only. The Authors have presented in [11] a thorough ET analysis of CNT PDNs, allowing to identify the conditions under which such innovative PDNs may outperform conventional ones.

In this paper, we generalize such an analysis by studying two new conditions that are likely to bring the results closer to the real applications: the first case refers to the possibility to fabricate the interconnects with graphene nanoribbons, instead of CNTs. Indeed, the use of GNRs interconnects may be a technological solution to the problem of growing horizontal CNT interconnects. The second case is given by the introduction of the contact resistance at the carbon/metal interfaces. As well known in literature [7], such a term is among the main limiting factors that dramatically reduce the carbon interconnects electrical performance with respect to those predicted in its absence and in ballistic regime. To this end, we improved the previous model, by adding a temperature-dependent parasitic resistance.

The paper is organized as follows: in Section II the electro-thermal model is briefly revised, whereas Section III introduces the electrical and thermal parameters for the PDN equivalent circuits. A case study is analyzed in Section IV, referring to a graphene PDN.

II. Electrothermal Model

We refer to a simple structure for the PDN as depicted in Fig.1. The two conducting networks are separated by an insulation layer and connected to VDD and GND supply pins, respectively at the four corners of the basic element (stamp) of nxn nodes on the grid. The whole chip is obtained as mxm replicas of such stamp. It is thermally connected from one side to an ideal heatsink.

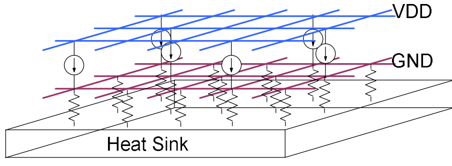

Fig. 1. Schematic of the considered power delivery network structure.

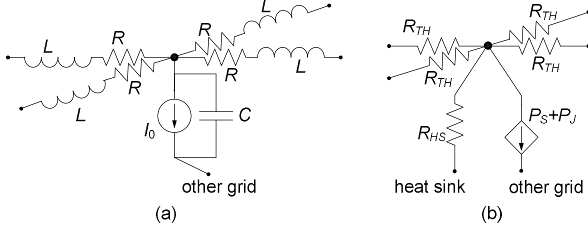

Fig.2 Electrical (a) and thermal (b) circuit model at each grid node.

The electrical and thermal problem are solved jointly, in both the static and possibly dynamic case. The electrical and thermal chip model is provided and explained, with reference to the considered technologies. Heat sources are mainly associated with the switching of the logic gates, as well as Joule heating in the PDN and at its feeding nodes. The use of the classical electrothermal equivalence for the thermal problem [12] allows the joint co-simulation of the physical problem within any standard circuit solver.

A. *Electrical modeling*

The basic electrical (DC) problem is modeled through two regular resistive grids, whose typical elementary portion is depicted in Fig.2b, where temperature-dependent resistors $R(T)$ connect adjacent nodes of the same grid. At each node power and ground grids are connected by a current source I_0, which represents the circuit *switching activity*. At the generic node i, the *voltage drop* is defined as:

$$V_d(i) = V_{DD} - (V_n(i) - V_g(i)), \tag{1}$$

where $V_n(i)$ and $V_g(i)$ are the node potentials on the power and ground plane references, respectively.

As for the dynamical analysis, a first order modeling of the parasitics of the structure is considered, by means of a series parasitic inductance L for each connection between adjacent nodes of the same grid, and a parallel capacitance C between corresponding nodes on the two different grids. An elementary dynamical cell is in this way defined as reported in Fig 2a. The parameters estimation for such equivalents is given in Sect. III.

B. Thermal Modeling

Due to a different order of magnitude for the characteristic times of the electrical and thermal dynamics, we assume a steady state thermal problem for the dynamical analysis of the structure. We can adopt the same grid for the electrical and thermal problems, and define a unique thermal resistance between the nodes [13]. The generic node of the thermal network is shown in Fig.2b: thermal resistances connect two nodes of the same grid, and an additional thermal resistance connects the node to the heat-sink; the two grids are connected by equivalent controlled sources, modeling the heat generation produced at node "*i*". It is due to two fundamental mechanisms: (*i*) the switching activity $P_S(i)=I_0V_d(i)$, as a function of the actual voltage due to the power produced at node "*i*", as affected by the voltage drop given in eq.(1); and (*ii*) the additional Joule contribution $P_J(i)$ due to the dissipated power into the PDN:

$$P_J(i) = \frac{1}{2}\sum_{k=1}^{4}\frac{v_{ik}^2}{R_{ik}}, \tag{2}$$

where the index k spans all the four nodes adjacent to node i.

The steady-state temperature distribution is evaluated with a classical relaxation approach, where the thermal problem is iteratively solved, updating the electrical resistances values, as well as the electrical one, updating the heat production terms, until convergence is achieved. In this way, steady state temperature and voltage drop distributions are obtained.

At this point, all data are available for a dynamic analysis (performed at the steady state temperature distribution). It has the twofold goal of (*i*) investigating the effects of additional voltage drop due to dynamic elements; (*ii*) assessing whether the level of additional thermal power due to electrical dynamic effects is compatible with the supposed steady state thermal equilibrium.

Dynamic analysis is performed in the frequency domain, by considering the corresponding impedances circuit at given frequencies. Such approach bases on two fundamental facts: (*i*) the possibility of superimposing voltages and currents evaluated at different frequencies (including DC); *(ii)* the circumstance that the average electrical powers calculated at different frequencies can be summed up due to their "orthogonality." By properly setting the frequency range of interest for the considered case, an exhaustive analysis is easily carried out, at affordable computation time.

III. TEMPERATURE-DEPENDENT CIRCUIT PARAMETERS

To retrieve the parameters for the circuit models in Figs.2, each branch of the power grid is modeled as a conductor of cross-section *WxH* and length *l*.

The thermal resistance may be simply modeled as:

$$R_{TH} = \frac{1}{k_m}\frac{l}{WH}, \tag{3}$$

where k_m is the thermal conductivity of the given.

The electrical resistance of a carbon-based interconnect of length *l* may be expressed as follows [5]-[7]:

$$R(T) = R_p(T) + \frac{R_0}{M(T)}\left(1 + \frac{l}{l_{mfp}(T)}\right), \tag{4}$$

where l_{mfp} is the electron mean free path, M is the number of conducting channels, $R_0 = 12.9\,\mathrm{k}\Omega$ is the *quantum resistance* and R_p is a parasitic term. The lumped term in (4), *i.e.* the term independent from length *l*, is the so-called *contact resistance*, whereas the distributed term is the *intrinsic resistance*. The latter term vanishes for *ballistic* transport ($l << l_{mfp}$). As for the contact resistance, in theoretical limit of ideal contacts it

reduces to the quantum limit R_0/M. Finally, R_P can be regarded as a *parasitic resistance* strongly dependent on the materials used to realize the terminal electrodes and on the type and quality of the contacts.

Assuming a low-bias condition (longitudinal field $e_z < 0.54$ V/μm) which is always the case for interconnect applications, the following fitting may be used for l_{mfp} [6]:

$$l_{mfp}(T) = D[k_1 + k_2 T + k_3 T^2]^{-1}, \quad (5)$$

where k_1=3.01·10^{-3}, k_2= -2.12·10^{-5} K^{-1} and k_3=4.70·10^{-8} K^{-2}. As for the number of channels M, it can be approximated by [6]:

$$M(D;T) \cong \begin{cases} M_0 & \text{for } D < x_0/T \\ a_1 DT + a_2 & \text{for } D \geq x_0/T \end{cases} \quad (6)$$

with fitting coefficients given in Table 1.

In this paper we adopt a recently proposed expression for the temperature-dependence of the parasitic term [14]:

$$R_p(T) = \frac{r_p}{S_c}\left(1 + \alpha_p\left(T - T_0\right)\right), \quad (7)$$

where $T_0 = 293\,\text{K}$ is the room temperature, r_p is the parasitic resistance at room temperature multiplied by the contact area S_c, and α_p is a thermal coefficient.

Any carbon interconnect of practical use is made of a bundle of CNTs or arrays of GNRs, fed in parallel, to lower the huge value of resistance of single carbon interconnects, [6]-[7]. If no particular care is paid in fabricating the CNTs or the GNRs, statistically 1/3 of them are metallic and the other are semiconducting: the same distribution holds for the shells of a MWCNTs. Therefore, in a bundle of N_b SWCNTs or in an array of N_b GNRs, the resistance may be simply modeled by:

$$R(T) = \frac{3}{N_b}\left(R_p(T) + \frac{R_0}{M} + \frac{R_0}{M}\frac{l}{l_{mfp}(T)}\right). \quad (8)$$

Here, M=2 for metallic SWCNTs and M=1 for metallic GNRs. The case of an interconnect made by a bundle of N_b MWCNTs may be handled by evaluating the total number of channels as

$$M(T) = \sum_{i=1}^{N_b}\sum_{k}^{N_s} M_{i,k}(T), \quad (9)$$

where $M_{i,k}(T)$ refers to the k-th shell of the i-th CNT in the bundle, of diameter $D_{i,k}$, given by (6).

The above models have been recently validated [14], with reference to CNT interconnects. In particular, such models were able to justify the experimental evidence of negative derivative of the resistance with temperature, that can occur in some ranges of the model parameters. Indeed, the model includes two counteracting mechanisms as temperature increases: from one hand, R increases since $l_{mfp}(T)$ decreases and $R_p(T)$ increases; from the other hand, R decreases since $M(T)$ increases. The balance between these counteracting factors can result in a negative or positive derivative, as shown in [14].

IV. Case-Studies

We investigate the behavior of the PDN with the structure given in Fig.1, with a core of dimensions 0.5mm x 0.5mm. In particular, the parameters for the global level interconnect at the 22nm technology nodes are assumed, see Table II. The PDN grid is 250x250, fed at the four corners of each elementary 25x25 stamp. A heatsink thermal resistance is assumed to be 100x the value of the thermal resistance of a single PDN branch. For such a case, the dynamic effects can be neglected, as shown in [11], hence a pure resistive model is assumed.

The reference solution is a conventional PDN where the conductors are made by copper. For its resistivity, we assume the classical model:

$$\rho(T) = \rho_0[1 + \alpha_0(T - T_0)], \quad (10)$$

with the parameter values typical of the 22 nm technology [11]: ρ_0=2.94μΩcm and α_0=0.0026 K^{-1}. The thermal conductivity is assumed to be k_m=193W/mK.

As for the CNT case, we consider the interconnects made by bundles of multi-walled CNTs (MWCNTs) of external diameters of 40nm, with filling factor of 80%, assuming a fraction of 1/3 of the shells to be metallic, and neglecting the contact resistance. For MWCNTs, a thermal conductivity of 200 W/mK was assumed.

Finally, the graphene realization refers to the case where each tract of the PDN is made by an array of GNRs, each of them with width and length equal to those of the tract, namely: W=160 nm and l=1.85 um (Table II). The density of the GNRs and hence the number of GNRs in the bundle are governed by the Van der Waals distance, whereas the fraction of metallic GNRs is again assumed as 1/3.
As for thermal conductivity, for GNRs arrays it is possible to assume higher values with respect to CNT bundles: indeed, experimental values are reported within 1500-2500 W/mK. Hereafter we denote with GNR1 (GNR2) the case corresponding to the minimum (maximum) of such values.

Table I: Fitting Coefficients for the Number of Channels in (6)

	Metallic CNT	*Semicond. CNT*
M_0	2	0
a_1 [nm^{-1}K^{-1}]	3.26·10^{-4}	3.26·10^{-4}
a_2	0.15	-0.20
x_0 [nm^{-1}K]	5600	600

TABLE II
Parameters for a Global Level Interconnects at 22 nm (1)

W [μm]	0.160
H [μm]	0.096
l [μm]	1.85
t_{ILD}[μm]	0.077
ε_r	3.0
V_{DD} [V]	0.9
J_0 [mA]	0.009÷0.178

View publication stats

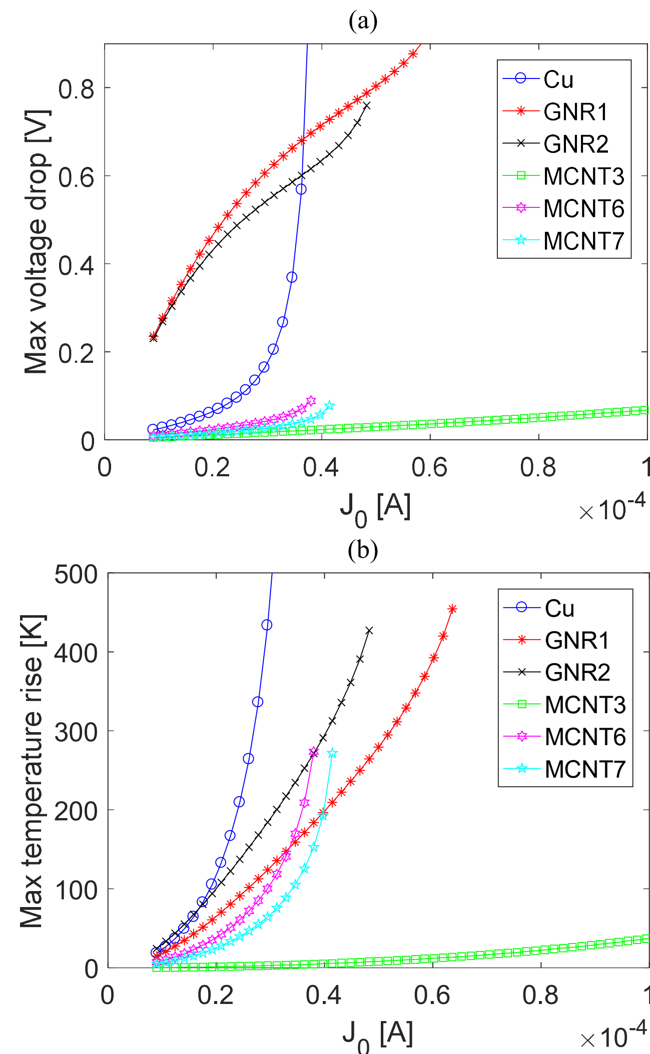

Fig.3 Performance analysis of the PDNs, comparing Cu, CNT and GNR cases: (a) maximum voltage drop, (b) maximum temperature rise, vs current source.

In Fig.3 we report the results of the performance analysis of the considered PDNs, in terms of the maximum voltage drop (Fig.3a) and the maximum temperature rise (Fig.3b) evaluated on the grid nodes, for different values of the current source J_0.

Here, MCNT3 refers to the ideal case, where the contact resistance for CNTs is negligible (in agreement with the simulations in [11]). Instead, MCNT6 and MCNT7 denote the case where such a resistance is present, assuming in (7) that $R_p(T_0)$ is respectively equal to 0.1 and 1 kΩ and $\alpha_P = 10^{-4}$ K^{-1}. These are realistic values for a bundle of CNTs, with standard quality of the contacts [14]. In our simulations, we assumed the contact resistances to be added at any CNT/metal interfaces, namely to the nodes connected to the current sources.

The MCNT3 realization exhibits the best electrical and thermal performance, with a voltage drop always lower than 0.1V and temperature rise not exceeding 50K. Such a realization works in the whole considered range of current J_0. If we take into account the contact resistance (MCNT6 and 7), there is not such a difference in terms of voltage drop (Fig.3a) but a huge difference in terms of temperature increase (Fig.3b), which strongly limits the admissible values of J_0.

The electrical performance for the GNRs is always worse than the CNTs. This behavior is essentially due to the higher values of resistance, since both the number of channels for single GNR and the total number of GNRs in the bundle are lower than in CNT realization [6]. Compared to copper realization, the GNR ones provide a higher voltage drop for low values of J_0, but for higher values the behavior is much better. As for the thermal performance, the behavior of GNR PDNs is always better than that of copper one. The CNT cases 6 and 7 outperform GNR only up to a certain level of J_0.

In conclusion, for the given PDN, CNTs always outperform Cu, both in electrical and thermal performance, whereas GNRs ones are better than Cu only in thermal performance. In CNT cases the influence of contact resistance is essential to determine not only the levels of voltage drop and temperature rise, but also the range of admissible feeding current J_0.

References

[1] International Technology Roadmap for Semiconductors, 2013, http://public.itrs.net

[2] H. Li, C. Xu, N. Srivastava, and K. Banerjee, "Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects," IEEE Trans. Electron Dev., vol.56, no.9, pp.1799-1821, 2009.

[3] P.J. Burke, "An RF circuit model for carbon nanotubes," *IEEE Trans. on Nanotechnology*, Vol.2, N. 1, pp.55-58, 2003.

[4] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron. Devices Lett.*, vol. 27, no. 5, pp. 338–340, May 2006.

[5] A. G. Chiariello, A. Maffucci, G. Miano, "Electrical Modeling of Carbon Nanotube Vias", *IEEE Trans. on Electromagnetic Compatibility*, Vol.54, No.1, pp.158-166, Feb. 2012.

[6] A. G. Chiariello, A. Maffucci, G. Miano, "Circuit Models of Carbon-based Interconnects for Nanopackaging, *IEEE Trans. on Components, Packaging and Manufacturing*, Vol.3, No.11, pp.1926-1937, Nov. 2013.

[7] A. Todri-Sanial, J. Dijon and A. Maffucci, "Carbon Nanotube Interconnects: Process, Design, and Applications". Springer, ISBN: 978-3-319-29744-6, 2016.

[8] X. Chen, D. Akinwande, K.-J. Lee, G. F. Close, S. Yasuda, B. C. Paul, S. Fujita, J. Kong and H.-S.P. Wong, "Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics," *IEEE Trans. Electr. Devices*, Vol.57, no.11, pp.3137-3143, Nov. 2010.

[9] N. Srivastava, R.V. Joshi, and K. Banerjee, "Carbon Nanotube Interconnects: Implications for Performance, Power Dissipation and Thermal Management,"*Proc. of IEEE Inter. Electron Devices Meeting, IEDM*, pp. 249-252, Washington, DC, USA, Dec.2005.

[10] A. Naeemi and J. D. Meindl, "Performance Modeling for Single- and Multiwall Carbon Nanotubes as Signal and Power Interconnects in Gigascale Systems," *IEEE Trans. on Electron Devices*, Vol. 55, N.10, pp. 2574-2582, Oct. 2008.

[11] A. Magnani, M. de Magistris, A. Maffucci, A. Todri-Sanial, "Electrothermal Analysis of Carbon Nanotube Power Delivery Networks for Nanoscale Integrated Circuits,", IEEE Trans. on Nanotechnology, Vol. 15, N.3, pp.380-388, May 2016.

[12] K. Fukahori and P. R. Gray, "Computer simulation of integrated circuits in the presence of electrothermal interaction," *IEEE J. Solid-State Circuits*, Vol. SC-11, no. 6, pp. 834–846, Dec. 1976.

[13] A. Magnani, M. de Magistris, A. Maffucci, A. Todri-Sanial, "A node clustering reduction scheme for power grids electrothermal analysis," *Proc. of IEEE Work. on Signal and Power Integrity, SPI 2015*, pp.74-77, Berlin, Germany, May 2015.

[14] A. Maffucci, F. Micciulla, A. E. Cataldo, G. Miano and S. Bellucci, "Modeling, Fabrication and Characterization of Large Carbon Nanotube Interconnects with Negative Temperature Coefficient of the Resistance," to appear in *IEEE Trans. on Components, Packaging and Manufacturing Technology*, DOI: 10.1109/TCPMT.2016.2643007, available in preview.